High Voltage MOSFET Compact Modeling

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ABSTRACT

This article presents state-of-the-art high-voltage (HV) transistor compact models and new developments. After a short look into the laterally diffused metal-oxide semiconductor (LDMOS) transistor physics, an overview of the main HV transistor compact models is given. HV transistor modeling with BSIM sub-circuits as well as analytical models like EKV HV and HiSIM_HV is discussed in detail.

Keywords: Compact modeling, LDMOS, LDMOS Sub-circuit, EKV-HV, HiSIM_HV, parasitic modeling, 1/f noise modeling.

1 INTRODUCTION

Compact models are defined as models for circuit elements which are sufficiently accurate and simple to incorporate into circuit simulators. Hence, the outcome is useful to circuit design. Careful benchmarking of the available models need to be done in order to fulfill the special design requirements on one hand side and do not overshoot simulation time and parameter extractions effort on the other side.

In many new applications such as communication and automotive electronics, the use of integrated HV MOS transistors (LDMOS and double-diffused MOS (DMOS)) requires highly accurate compact models which need to take into account the drastic differences in the electrical behavior.

An example for a typical HV LDMOS transistor structure is shown in Fig. 1. Increased junction breakdown voltage (BV) of the drain diffusion is achieved by using a deep drain well [1]. Light well doping and large radii of the cylindrical and spherical junctions at the border increase the BV. Small on-resistance and high BV are contrary effects. The optimization of the tradeoff between both quantities is of major interest. The gate length is extended beyond the body-drain well junction, which increases the junction BV. The gate acts as a field plate to bends the electric field. As a result the critical field strength occurs at increased drain source voltages, commonly known as reduced surface field (RESURF) effect [2]. As there are high voltages at the drain, the electric field at the end corner of the gate electrode becomes quite large due to the small radius. Therefore, field oxide or shallow trench isolation (STI) is used to separate the critical gate region and the drain region. Furthermore, a so-called quasi-saturation is found for short-channel devices at high gate and drain bias. One reason for this is the Kirk effect in the drift region. Detailed explanations are presented in [4].

For reliable compact models, the following physical effects must be taken into account:

- Quasi-saturation.
- Self-heating.
- Channel geometry scaling
- Geometry-related.
- Graded channel.
- Bulk current.
- Impact ionization in the drift region.
- High-side switch.
- Parasitic bipolar junction transistor (BJT).

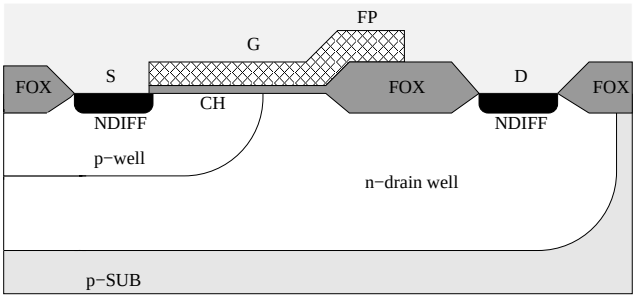

Fig. 1: Body-Isolated N-channel HV MOSFET

Figures of merit for LDMOS devices are mainly the on-resistance (Ron), gate-to-drain capacitance (Cgd), and BV. For radio frequency (RF) applications, the parameters transit frequency (FT) and maximum oscillation frequency (Fmax) are added to the list. These requirements must be taken into account for the selected compact model and their capabilities.

An additional challenge is LDMOS modeling for analog and RF circuit design. The integration of complex analog and RF functions such as RF power amplifiers in state-of-the-art wireless circuits requires accurate compact models in the high-frequency range. The compact model must account for the additional LDMOS effects in digital circuit (DC), analog circuit (AC) and RF large-signal regimes. The integration of these devices is done in RF complimentary MOS (CMOS), bipolar CMOS (BiCMOS) and bipolar CMOS and DMOS (BCD) technologies.

2 HV TRANSISTOR SUB-CIRCUIT MODELING

The lack of HV compact models has driven the development of sub-circuits. In the 1990s, foundries first offered HV LDMOS devices and SPICE realizations that were able to consider the special HV LDMOS effects. A sub-circuit of a device is a network composed of different active and linear or non-linear passive components. These components are connected in a specific way such that the device characteristics are reproduced most accurately. Furthermore, sub-circuits allow high flexibility. They can be easily adapted by adding or removing components in the net list. There is a well-defined node interface between the sub-circuit box and the external circuit where the sub-circuit appears to be a single device. The major disadvantage is increased simulation time due to a larger effective number of circuit nodes and components. Furthermore, special attention needs to be paid to the convergence in the circuit simulator.

In recent years, numerous sub-circuit solutions have been published, and sub-circuits for RF LDMOS modeling introduced. Inductors and capacitors are included to model the RF behavior, and a junction field-effect transistor (JFET) is used to improve the DC modeling. This JFET approach is applied in many circuits, where improved capacitance modeling has been achieved by adding voltage-controlled, gate-bulk and gate-drain capacitors or positive channel FET (PFET) devices to a negative channel FET (nFET) LDMOS structure. An example using the JFET approach in combination with an advanced core FET model (e.g., Berkeley Short-Channel Insulated-Gate FET (IGFET) (BSIM) Model or Enz-Krummenacher-Vittoz (EKV) Model) [5] for an unsymmetrical LDMOS traisistor is presented in Figure 2. Comparisons of DC measurements and simulations (IdVd) are Figure 3.

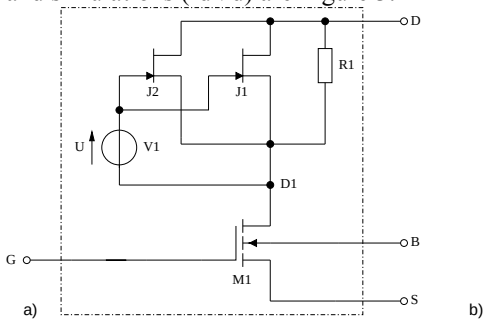

Fig. 2: JFET Approach with an Advanced Core FET Model

3 EKV HV COMPACT MODEL

The EKV HV compact model for vertical and lateral DMOS has been developed by the Swiss Federal Institute of Technology [6],[7]. It relies on the core of the charge-based EKV 2.6 MOSFET model for the intrinsic MOSFET, while the drift region is modeled with a bias-dependent resistance.

The EKV MOSFET model has the advantage of being physical and continuous in all regions of operation. The model is formulated on an inversion-charge description, where the voltage versus surface potential equation is transformed into an approximate equation of node charge versus node voltage drop. Similarly, the current versus surface potential equation can also be transformed into an approximate current versus node charge equation. Thus, the node charges become the independent variables. The single expression formulation ensures continuity of first and higher order derivatives with respect to any terminal voltage in the entire operating range.

The following physical effects are included in the EKV MOSFET model:

- Basic geometrical and process-related aspects such as oxide thickness, junction depth, effective channel length and width.
- Effects of doping profiles, substrate effect.
- Modeling of weak, moderate and strong inversion behavior.
- Modeling of mobility effects due to vertical and lateral fields and velocity saturation.
- Short-channel effects such as channel-length modulation (CLM), source and drain charge-sharing (included for narrow channel widths) and reverse short-channel effect (RSCE).
- Modeling of substrate current due to impact ionization.
- Quasi-static, charge-based dynamic model.
- Thermal and flicker noise modeling.
- A first-order non-quasi static model for trans-admittances.
- Short-distance geometry and bias-dependent device matching.

4 HISIM_HV MOSFET MODEL

In 2008, the Compact Modeling Council (CMC) selected the Hiroshima University STARC IGFET Model (HiSIM_HV) as the first standard HV MOSFET model [8]. HiSIM_HV was developed as an extension of the advanced low-voltage MOSFET model (HiSIM2). The model concept is based on the drift diffusion theory using charge sheet approximation of the inversion layer with zero thickness including gradual channel approximation. Unlike other surface potential-based models that use simplified analytical equations, the HiSIM2 model solves the Poisson equation iteratively. Less smoothing functions are needed due to smooth model equations, which result in fewer iteration steps. The applied iteration procedure ensures no run time penalty. The surface potentials at the source, the pinch-off point, the channel/drain junction and the drain contact are determined, and, at the same time, are implicit functions of the applied terminal voltages referenced to the source node. Thus, model-internal iteration procedures are required only for calculating the surface potential.

The device physics-based approach makes the model easily adaptable to special MOSFET devices such as LDMOS. HiSIM_HV solves the Poisson equation along the MOSFET channel iteratively, including the resistance effect in the drift region. The complete surface potential-based compact model offers a unified description of device characteristics for all bias regions. Model options can be selected by more than 20 model flags, offering high flexibility. HiSIM_HV scales with the gate width, the gate length, the number of gate fingers and the drift region length. In addition, HiSIM_HV is capable of modeling symmetric and asymmetric HV devices. Figure 3 shows a LDMOS output characteristic comparing measurements and the HiSIM_HV model.

The following effects are also included:

- Depletion effect of the gate polycrystalline silicon (poly-Si).
- Quantum mechanical.
- CLM.
- Narrow channel.
- STI.
- Leakage currents (gate, substrate and gate-induced drain leakage (GIDL) currents).
- Source/bulk and drain/bulk diode models.
- Noise models (1/f, thermal noise, induced gate noise, coupling noise).
- Non-quasi static (NQS) model.

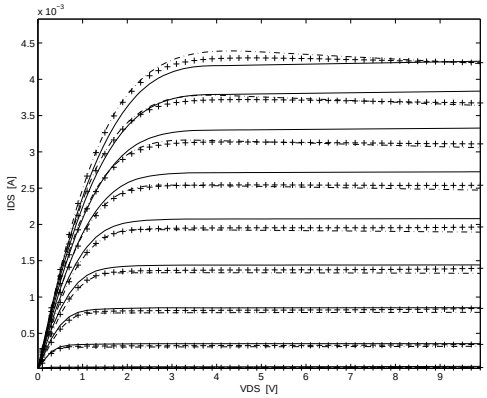

Fig. 3: HV CMOS Transistor Output Characteristic. Dashed line HiSIM_HV model, full line BSIM3v3 sub circuit (-) v. measurements (+).

5 1/F NOISE MODELING FOR HV TRANSISTORS

In this chapter we compare the 1/f noise model capability of HiSIM_HV and the BSIM3v3 sub-circuit described in chapter 2. The origin of flicker noise in HV transistors, mobility fluctuations as well as charge carrier fluctuations is still unchanged.

Mainly two parameters are used for modeling the 1/f noise in HiSIM_HV: NFALP which is applied for the mobility fluctuation phenomenon and NFTRP which is applied for the ratio of trapped density to attenuation coefficient. Additionally a third parameter can play a role: CIT, a capacitance parameter applied for interface-trapped carriers. Normally it is fixed to zero.

The same is valid for the BSIM3v3 sub-circuit approach to model HV devices: The flicker noise formulation is kept untouched to the low voltage description of BSIM3v3. Nevertheless there are two fundamental differences to HiSIM_HV:

1.) The BSIM3v3 approach has a different formulation for operating regions vg > vth + 0.1V and vg < vth + 0.1V; Therefore a discontinuous flicker noise model may occur in comparison to HiSIM_HV which uses one common formulation for strong and weak inversion operating regions (see the strong kinks in the pictures below especially for HV NMOS).

2.) The DC modeling approach is of course different and therefore the thermal noise description will also differ. Generally, thermal noise measurements in general are very difficult to perform at low frequencies. Another approach to check is the input referred noise. For accurate gm modeling also the input referred noise is simulated with higher accuracy. If the gm does not differ much from both HV model approaches then the noise models it can be compared (see Fig. 4 and Fig. 5).

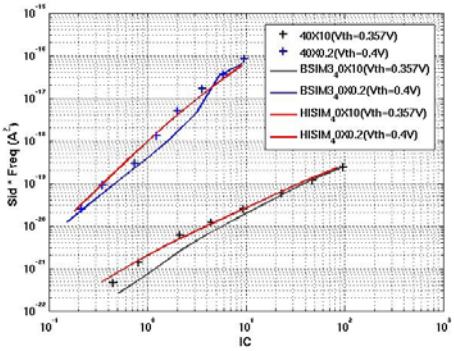

Fig. 4: HV NMOS, drain current noise Sid*Freq @ Vds=3V versus inversion coefficient IC for a short channel (upper curves) and a long channel device (lower curves) measurements: black crosses, HiSIM_HV: red lines, BSIM3v3: dark lines

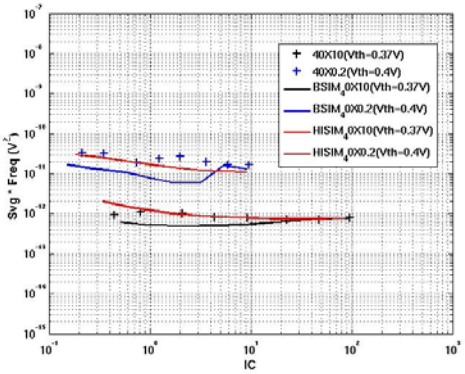

Fig. 5: HV NMOS, input referred noise Svg*Freq @ Vds= 3V versus inversion coefficient IC for a short channel (upper curves) and a long channel device (lower curves) measurements: black crosses, HiSIM_HV: red lines, BSIM3v3: dark lines

As shown in the Fig. 4 and Fig. 5 the HiSIM_HV flicker noise model approach shows a much better agreement with measurement data in comparison to a BSIM3v3 sub-circuit approach. The simulated gm data from both models is quite same.

6 MODELING OF PARASITICS FOR HV TRANSISTORS

The complexity of a HV LDMOS transistor structure introduces parasitic junctions which can significantly influence device performance. Depending on the architecture of various ICs, the relevance of the different parasitic effects varies. Three main parasitic effects can be identified: leakage currents, forward-biased bipolar transistors and capacitive.

Leakage currents flow through different wells down to the substrate. These currents are always present. They are strongly temperature-dependent. Low-power applications are most sensitive to such currents, but due to their relevance for stand-by power consumption, leakage currents are of interest to all applications.

Possible forward bipolar action also provides a current path down to the substrate. To prevent this action, switched devices must be treated with great care. Applications such as DC-DC converters or H-bridges can be mentioned here. There are two types of parasitic capacitances — the MOS overlap and the junction depletion. The first one (gate-to-drain or gate-to-source) can couple a signal from one terminal to the other, causing large problems regarding signal distortion and speed loss. The second one (well-to-well or well-to-substrate) can result in circuit speed reduction. The design approach generally used to simulate parasitic effects after parasitic extract can fail. A more advanced strategy in parasitic modeling is to provide a solution during the circuit design phase. Therefore, all parasitic effects should be covered by the device models. For the covering of substrate currents, no possibility for implementation is given so far. The lack of compact models including parasitic effects implies the usage of sub-circuit solutions. Fig. 6 shows a cross section of a LDMOS transistor where the parasitic devices are demonstrated.

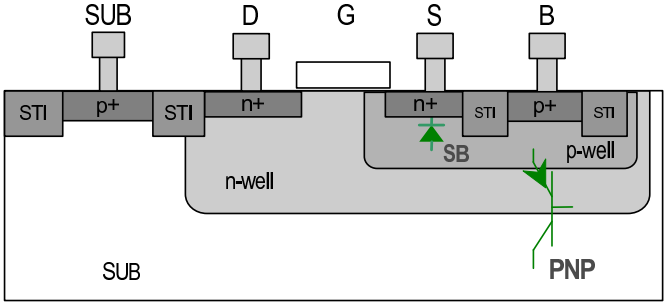

Fig. 6: Cross-section of an Isolated N-MOS Transistor

7 FURTHER DEVELOPMENTS

Hiroshima University is working on the next generation of the HiSIM_HV model. Inputs for further model requirements are given from the industrial partners of the CMC.

In the actual version HiSIM_HV ver.1.2.1 and former versions, the drift-resistance is modeled as a voltage controlled resistance with numerous empirical parameters, in order to describe the gate, drain and bulk voltage dependences. However, this drift-resistance description is rather complicated and has a large number of parameters to be extracted and adjusted. Another drawback is that this semi-empirical model has inherently the risk of non-physical behavior on the simulation result. This was the major motivation to develop a physical drift-resistance model.

In HiSIM_HV 2.0.0, which is currently under development, in addition to the old analytical-empirical model a new physical drift-resistance model will be introduced.

The drift-current in the drift region is described as:

$$I_{ddp} = W_{eff} \cdot X_{OV} \cdot q \cdot N_{drift} \cdot \mu_{drift} \cdot f\left(V_{ddp}, L_{drift}\right)$$

Where W_{eff} is the effective width, X_{ov} stands for the effective depth of the drift region, which is modulated by the surface potential and the drift/substrate junction. N_{drift} is the doping density in the drift region, μdrift is the mobility in the drift-region. The latter three are again a function of the voltage drop across the drift region (V_{ddp}) and of the drift length L_{drift}. This new concept should especially improve the drift-length scalability.

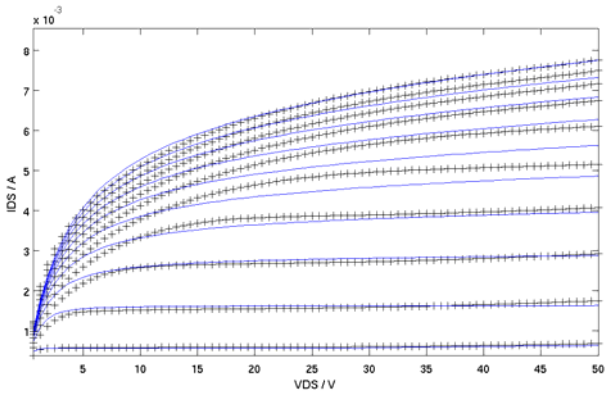

Fig. 7 Output characteristics of a short channel 50V thin oxide n-type LDMOS. The lines are the model results and the crosses are the measurements. Vb=0V and Vg is from 0.9 – 3.6V.

From Fig. 7, an excellent fitting is shown for both the gate and the drain voltage dependences which show the

good model quality although this new version is still under development.

The improvements/enhancements include also:

- Improved impact ionization model in the drift region.
- Improved capacitance model
- Asymmetrical bulk diodes
- Punch-through model

Another very interesting HV transistor development activity is ongoing in the EU FP7 People project and the Compact Modeling Network (COMON)). Several leading European companies such as Infineon and austriamicrosystems are cooperating with small and medium enterprises (SMEs) such as ADMOS and Dolphin and several universities (Swiss Federal Institute of Technology in Lausanne (EPFL) and Technical University of Crete (TUC)) in the development of advanced HV transistor models. The modeling activities are concentrated on a new approach and rely on the core of the charge-based EKV3.0 model.

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