

Generic Compact Model Development of Double-Gate MOSFETs with Inclusion of Different Operation Modes and Channels from Heavily Doped to Intrinsic Case

Xingye Zhou¹, Jian Zhang¹, Lining Zhang¹, Chenyue Ma¹,
Jin He^{1,2}, and Mansun Chan²

¹ Key Laboratory of Integrated Microsystems, Shenzhen Graduate School of Peking University, Shenzhen 518055, China

²Department of ECE, Hong Kong University of Science & Technology, Kowloon, Hong Kong

Tel: 86-0755-26032104 Fax: 86-0755-26035377 Email: xyzhoufly@163.com

Abstract - In this paper, the Double-Gate MOSFET's operation modes such as symmetric, asymmetric and independent-gate-operation are discussed and an idea for the generic compact model development is proposed. It is shown that the presented generic model predicts different DG MOSEET operation modes and the characteristics, which are well verified by the 2-D numerical simulator in different cases. We also analyze the model limitation and further improved direction.

I. INTRODUCTION

With the intensive downscaling of CMOS VLSI integrated circuits, traditional bulk device structure is approaching the practical limit imposed by gate tunneling and severe short channel effects (SCEs). In order to extend CMOS to next generation VLSI ICs, various alternative novelty device structures and process integration technology have been widely studied [1]. Among the proposed non-classical device structures, Double-Gate (DG) MOSFETs with very thin film body are strong contenders to replace the bulk MOSFETs due to superior short-channel-effect immunity, near-ideal sub-threshold slope, and low parasitic resistance and capacitance.

To predict the performance characteristics of DG MOSFETs, an accurate compact model is required to benchmark or simulate future generation circuit performance in future. Much research work has been devoted to developing compact models for DG MOSFETs. For example, some models applicable for symmetric DG MOSFETs have been developed in [2-7]. Some useful asymmetric and independent-gate MOSFETs models have also been proposed [8-12]. A generic core model for double-gate

MOSFETs, valid for symmetric, asymmetric and independent-gate-operation modes, has been reported in [13]. However this model is only applicable for undoped DG MOSFETs. To our knowledge, a generic compact model for both doped and undoped DG MOSFETs, valid for all symmetric, asymmetric and independent-gate-operation modes, is not available up to now.

In this paper, we discuss the DG MOSFET's operation modes. And then, a generic potential-based compact model for both highly doped and lightly undoped DG MOSFETs, applicable for all symmetric, asymmetric and independent-gate-operation modes, is described and further compared with the 2-D numerical simulation.

II. OPERATION MODES OF DG MOSFET AND PROPOSED MODEL

Due to the inherent complexity of solving Poisson equation with ionized dopant and free carrier charge terms, a generic compact model for both doped and nearly intrinsic DG MOSFETs applicable for all gate-operation modes has not been reported. While from the perspective of circuit designers, such a model to analyze and predict the performance of DG MOSFETs is highly desirable for different design consideration.

Fig.1 shows the structure and coordinate system of a generic N-type DG MOSFET. As we all know, depending on the structure parameters and gate biases, DG MOSFETs can operate in different modes: symmetric, asymmetric and

independent-gate-operation modes. A) A symmetric DG MOSFET has symmetric structure parameters (such as identical work function and oxide thickness for front gate and back gate) and the same input voltages for two gates. B) An asymmetric DG MOSFET is with asymmetric structure parameters (such as different work-function and different gate oxide thickness) but the same input voltages for two gates. C) DG MOSFETs with one of its gates biased to a constant voltage while the input signal enters the other gate, can be referred to as Independent-gate-operation mode.

With the physical analysis, no matter which operation mode the DG MOSFET is in, the channel potential profile along the direction vertical to the drain current direction can generally be classified into three categories as shown in Fig.2. For simplicity, the Fermi energy level and gate voltage are not shown. T_{si} , T_{oxf} and T_{oxb} are the thickness of silicon film, front gate insulator and back gate insulator separately and L is the channel length.

(I) The first category named as “bulk-like” in this report is that the channel is partially depleted, and DG MOSFET can be referred to as two bulk MOSFETs.

(II) The second category is that the channel is fully depleted and the position (x_0) where the electric field equals zero is inside the silicon film, which is named as “DG-like”.

(III) The third category named as “SOI-like” represents that the channel is fully depleted, but there is no the position where the electric field equals zero inside the silicon film.

The channel potential profile transits from one category to another as the gate voltage varies, and DG MOSFETs can only work in one of these three categories under a given operation point.

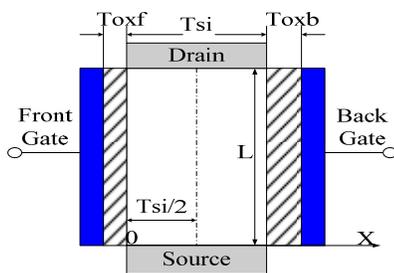


Fig.1 Cross section and the coordinate system of a generic N-type DG MOSFET with silicon channel.

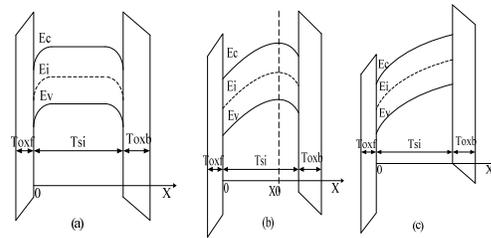


Fig.2 Simple corresponding energy band diagrams for the three categories mentioned above: (a) bulk-like; (b) DG-like; (c) SOI-like.

According to the three categories mentioned above, the proposed model is divided into three core parts. Depending on an approach that we used, this generic model selects one of the core parts to model the surface potential at the gate oxide/silicon film interface and the drain current for the corresponding category under the given operation point.

III. RESULTS AND DISCUSSION

The proposed generic model is verified by comparison with a 2-D self-consistent numerical solver, ULTRAS-DG [25]. A long-channel DG MOSFET with constant carrier mobility of $400 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ is chosen. The length and width of the channel are both 1 μm , and metal gate with mid-gap work function ($4.6eV$) is used. T_{oxf} and T_{oxb} unless specified. V_{gf} , V_{gb} and V_{ds} are the voltage for front gate, back gate and drain terminal separately. V_{fb} represents the flat band voltage. The work function difference of front gate and back gate is defined as $\Delta\Phi_f$ and $\Delta\Phi_b$ separately. N_a denotes the doping concentration of the channel.

Fig.3 is the model-predicted I_{ds} versus effective gate voltage curves of DG MOSFET for different levels of doping concentration in symmetric mode, compared with 2-D numerical simulation results. Lines represent the proposed model and symbols denote the numerical results. Apparently, the drain current from the generic model extensively agrees with the numerical simulation, from weak inversion to strong inversion and from lightly doped channels to highly doped channels.

Fig.4 illustrates the drain current I_{ds} versus V_{gs} curves of DG MOSFET for different doping concentrations in independent-gate-operation mode, $V_{gb}=0$, given by the proposed model and the numerical results. Agreement between the

model and numerical results for different doping levels are observed with acceptable error in the strong inversion region.

Fig.5 and Fig.6 demonstrate the transfer characteristics of DG MOSFET with different work function for two gates in asymmetric mode. Fig.5 indicates the impact of different levels of doping concentration on the $I_{ds}-V_{gs}$ curves, and Fig.6 gives the $I_{ds}-V_{gs}$ curves of an asymmetric DG MOSFET considering the impact of work function difference. Both Fig.5 and Fig.6 show that the current calculated from the model and the numerical simulation results agree with each other well.

The output characteristics of a DG MOSFET in asymmetric mode together with the numerical results are shown in Fig.7, which displays that the DG MOSFET characteristics obtained from the proposed model also have a good agreement with the numerical simulation.

Fig.8 shows the $I_{ds}-V_{gs}$ curves of a DG MOSFET with a larger work function difference for two gates in asymmetric mode, including the currents calculated from the proposed model and numerical simulation results. It is found that the deviation between both is very small as a DG MOSFET operation transits from the weak inversion region into the strong inversion region, or from a SOI-like operation into a DG-like operation mode. Thus, the combined SOI-like and DG-like mode gives accurate curves with the numerical simulation.

Again, Fig.9 demonstrates the $I_{ds}-V_{gs}$ curves of a DG MOSFET with different oxide thickness for two gates in asymmetric mode, given by the model and 2-D numerical simulation. Fig.9 indicates that the drain current of a DG MOSFET predicted by the model agrees with the 2-D numerical simulation well in different doping level and in a large gate bias region, for different front and back gate oxide thickness. This results demonstrate the validity of the proposed model..

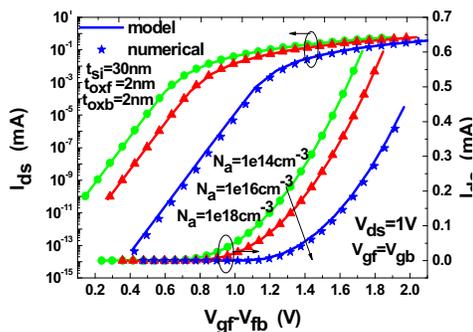


Fig.3 Model-predicted I_{ds} versus effective gate voltage of a DG MOSFET in symmetric operation mode with different doping concentrations, compared with the numerical simulation results.

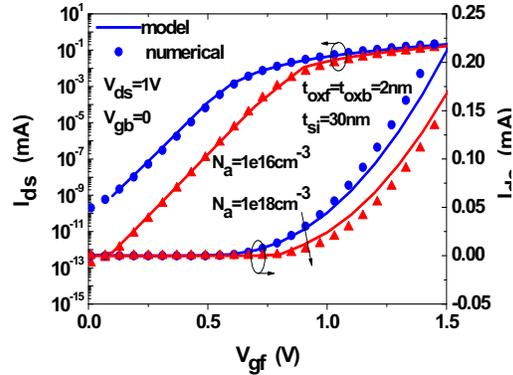


Fig.4 Comparison of transfer curves of a DG MOSFET in independent-gate-operation mode, from the generic model and numerical simulation.

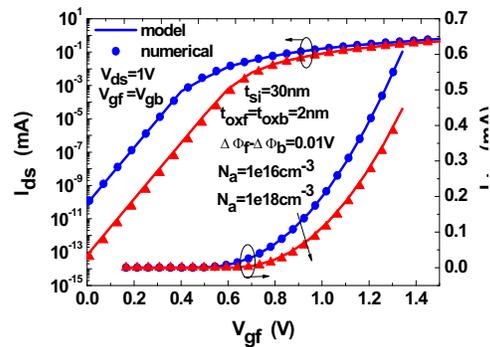


Fig.5 Transfer characteristics of a DG MOSFET with different work function in asymmetric operation mode with different doping levels, obtained from the model and numerical results.

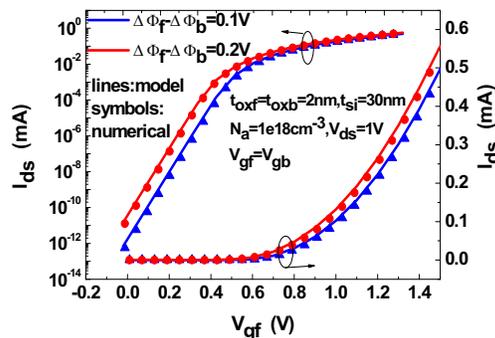


Fig.6 $I_{ds}-V_{gs}$ curves of a DG MOSFET with larger work function difference in asymmetric operation mode.

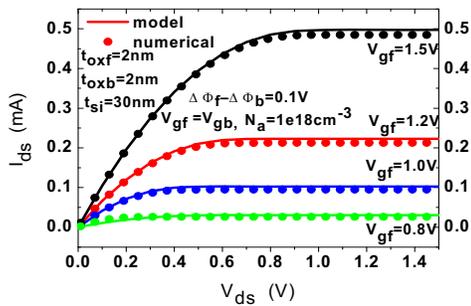


Fig.7 Distinct output characteristics of a DG MOSFET together with the numerical results in asymmetric mode with different work function.

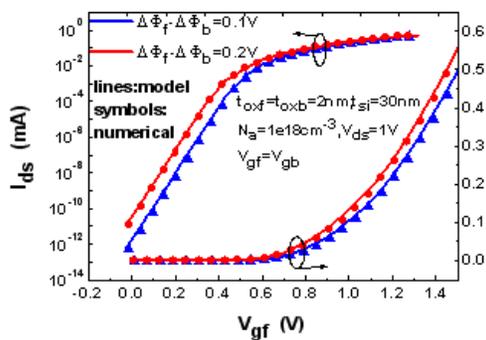


Fig.8 Illustration of the drain current of a DG MOSFET given by the model with different work function for two gates in asymmetric mode, compared with 2-D numerical simulation.

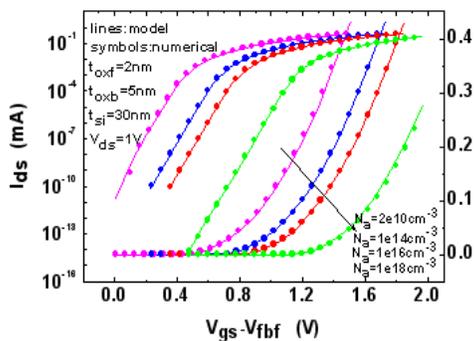


Fig.9 Plot of I_{ds} - V_{gs} curves of a DG MOSFET with different oxide thickness in asymmetric mode in comparison with numerical results.

VI. CONCLUSION

In summary, a generic compact model for both doped and nearly intrinsic DG MOSFETs has been developed, applicable for symmetric, asymmetric and independent-gate-operation is proposed. The proposed model consists of three core parts for the corresponding categories mentioned in section III. The validity of the proposed model has also been verified by the 2-D numerical simulation.

ACKNOWLEDGEMENT

This work is supported by the Natural Science Funds of China (60876027), and the special funds for major state basic research project.

REFERENCES

- [1] ITRS, International Technology Roadmap for Semiconductors 2006.
- [2] Y. Taur, ET al., *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 107–109, 2004.
- [3] A. Ortiz-Conde, et al., *Solid State Electronics*, vol. 49, no. 4, pp. 640-647, 2005.
- [4] Jean-Michel Sallese, et al., *Solid-State Electronics*, vol.49, no. 3, pp. 485-489, 2005.
- [5] F. Prégaldiny, et al., *WCM, 2006*; 3:386, ISBN0-9767985-8-1.
- [6] B. Diagne, et al., *Solid-State Electronics*, vol. 52, pp. 99-106, 2008
- [7] J. He, et al., *Semicond. Sci. Technol.*, vol. 23, no. 4, 045003, 2008.
- [8] G. Pei, et al., *IEEE Trans. Electron Devices*, vol. 50, no. 10, pp. 2135–2143, Oct. 2003.
- [9] M. Reyboz, et al., *Solid-State Electron.*, vol. 50, no. 1, pp. 1276–1282, Jan.2006.
- [10] A. S. Roy, et al., *Solid-State Electron.*, vol. 50, no. 4, pp. 687–693, Apr. 2006.
- [11] A. Ortiz-Conde et al., *Solid-State Electron.*, vol. 50, no. 11/12, pp. 1796–1800, Nov./Dec. 2006.
- [12] A. Ortiz-Conde, et al., *Proc.8th Int.Conf. Solid-State Integr.-Circuit Technol.*, Shanghai, China, pp. 1239–1242, Oct. 2006.
- [13] Xingyue Zhou, et al., “Multiple-gate MOSFETs: structure, operation modes, and generic compact model development.”. *6th IWCM, Yokohama, January 19, 2009.* .