Compact Model HiSIM-DG both for Symmetrical and Asymmetrical DG-MOSFET Structures

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ABSTRACT

We have developed the DG-MOSFET model HiSIM-DG based on the complete surface-potential-based description valid both for the symmetrical and the asymmetrical structures. HiSIM-DG including the short-channel effect model is verified to reproduce 2D-device simulation results for any applied bias conditions.

Keywords: dg-mosfet, symmetry, asymmetry, short-channel effect, subthreshold swing

1 INTRODUCTION

Advanced bulk-MOSFETs are facing serious problems such as increased off-current and diminished saturating characteristics of on-current due to enhanced short-channel effects. Thus Double-Gate MOSFETs are considered to be a promising candidate as the next generation MOSFET structure [1]. A big advantage of such structure with a very thin substrate silicon layer thickness is a suppression of the short-channel effect even down to 10nm channel length [2], [3]. To exploit the advantage for circuit applications, accurate compact models applicable for any device structures is inevitable.

Recently the asymmetrical structure has been demonstrated to provide better device performance enabling enhanced subthreshold characteristics [4]. Thus a compact model valid for the asymmetrical structure applicable for any bias conditions is highly requested. We have developed the DG-MOSFET model by solving the Poisson equation explicitly. The model is valid for any device structures with any bias conditions.

2 CORE PART OF HISIM-DG

Fig. 1 shows the studied DG-MOSFET as a symmetrical structure and its device parameter values. The complete surface-potential-based compact model HiSIM-DG has been developed by solving the Poisson equation iteratively [5], [6]. Thus HiSIM-DG solves the potential distribution along the silicon layer thickness explicitly as shown in Fig. 2a [7].The accuracy of the calculated potential values are compared with 2D-device simulation results for symmetrical structures in Figs. 2b and c. To capture the volume inversion effect, the charge distribution within the silicon layer along depth direction is considered in the Poisson equation explicitly. Good agreements have been proven for wide ranges of operation in condition.

The model solves the Poisson equation including the bulk charge. Thus the influence of the bulk impurity concentration can be verified. The dependence of circuit performances on the impurity concentration have been investigated with the model as shown in Fig. 3. It is demonstrated that the inclusion of the impurity concentration is important beyond $N_{sub}=1\times10^{16}cm^{-3}$.

Next we consider DG-MOSFETs of an asymmetrical structures and its band diagram under applied biases as shown in Fig. 4a and b, respectively. The extended HiSIM-DG for the asymmetrical structures is modeled by considering the independent charges $Q_{g1}$and Q_{g2} in the Poisson equation. These charges are combined with the Gauss Law. The extended HiSIM-DG valid both for the symmetrical and the asymmetrical structure treats the gate electric field explicitly, thus switching between the symmetrical structure and the asymmetrical structure is done automatically in a smooth way.

The extended HiSIM-DG for the asymmetrical structures have been verified its validity for the device structure and its device parameter values shown in Fig. 4a. Calculated potential values for various conditions are compared with 2D-device simulation results in Fig. 5. It is seen that the sub-gate bias V_{g2} controls the inversion condition of the main gate V_{g1} surface potential, enabling the threshold voltage shift [4]. These features of the asymmetrical DG-MOSFET structures are well captures by HiSIM-DG.

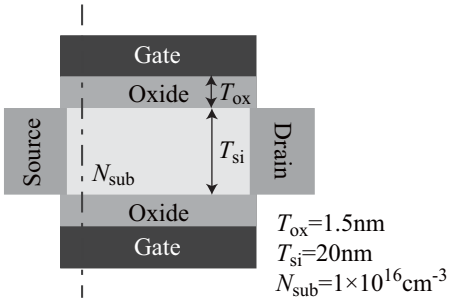


Fig. 1: Symmetrical DG-MOSFET and its device parameter values.

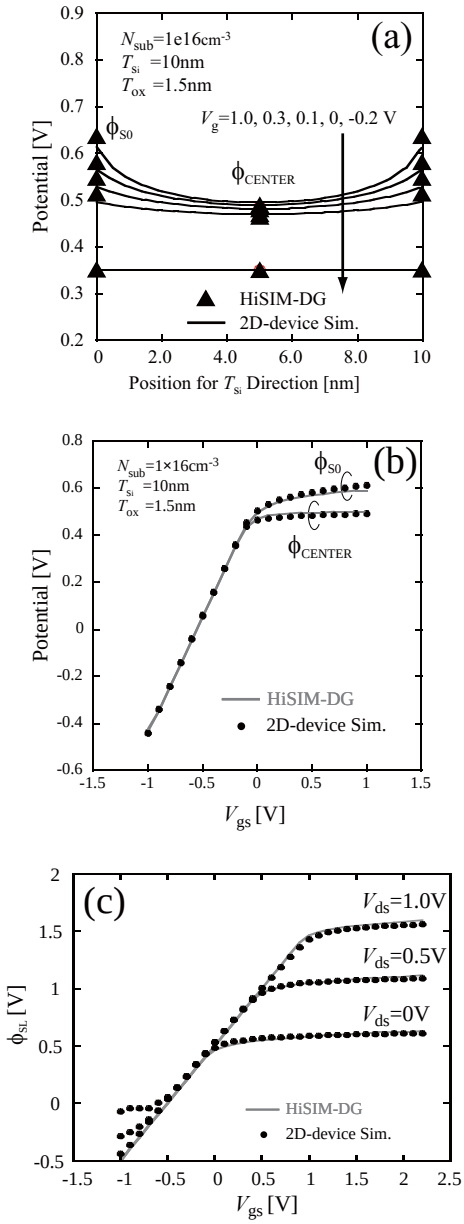
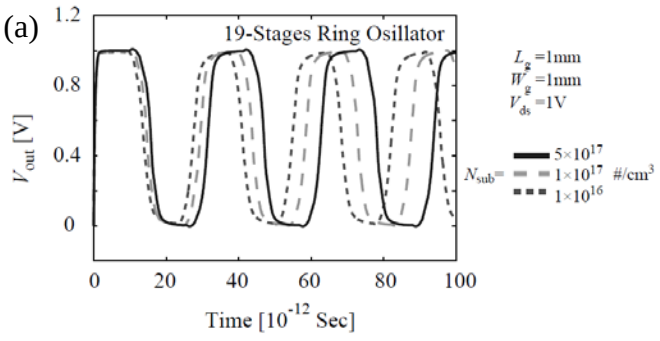


Fig. 2: Calculated potential values; (a) potential distribution in the silicon layer, (b) potential values at the surface and the middle of the silicon layer, (c) potential value at the drain side.



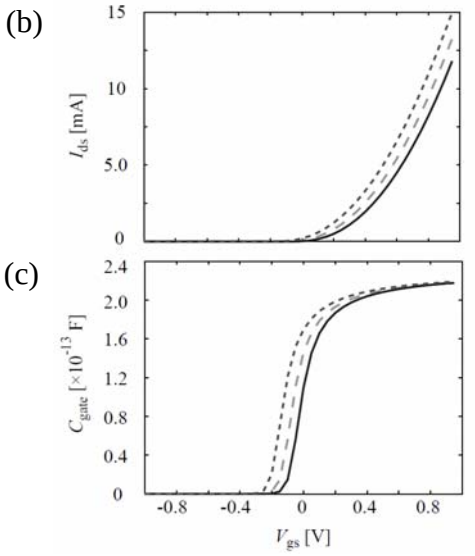
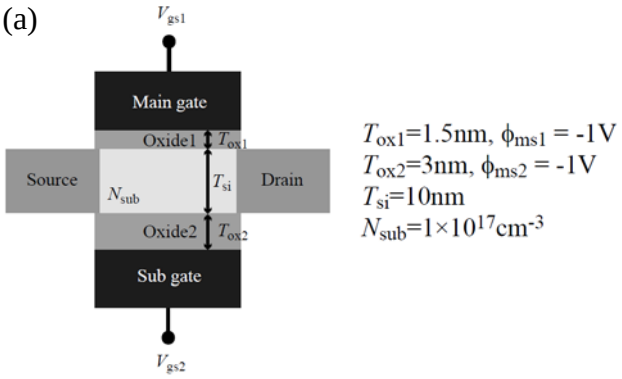


Fig. 3: (a)Waveform for different substrate impurity concentration; (b) the drain current as a function of the fate voltage; (c) the gate capacitance as a function of the gate voltage.



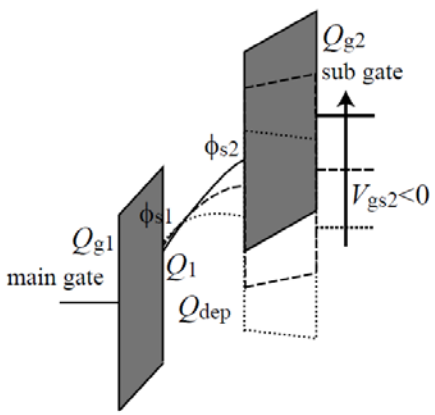


Fig. 4: (a) Asymmetrical DG-MOSFET and its device parameter values, (b) band diagram change by applied biases.

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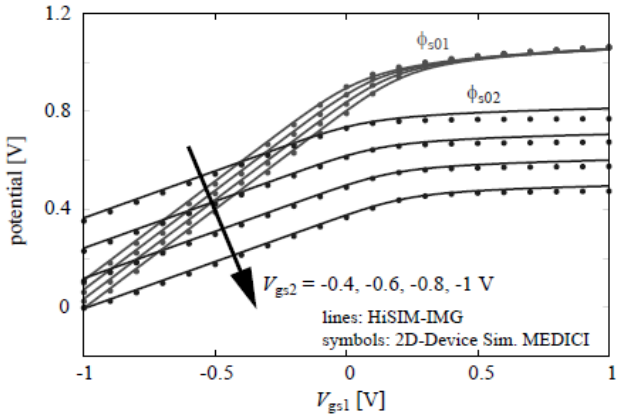

Fig. 5: Calculated surface potential values at the main V_{g1} and sub gate V_{g2} with HiSIM-DG in comparison to 2D-device simulation results.

3 MODELING THE SHORT CHANNEL EFFECT

The short-channel effect modeling is very important for the real application of DG-MOSFETs. It has been modeled on the basis of the threshold voltage. The threshold voltage modeling including the volume inversion effect is already discussed [8], and we focus here to develop a compact short-channel model for the subthreshold degradation, where the most feature of the DG-MOSFET is observable [9]. This is inevitable for real application of the DG-MOSFET. The modeling is done as the effective gate voltage shift ΔV_{gs} from the ideal case as schematically shown in Fig. 6. We start with the two dimensional Poisson equation describing the relationship between the potential ϕ and the total charge density ρ

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=-\frac{\rho(x,y)}{\varepsilon_{si}} \tag{2}$$

By approximating that the lateral electric field is constant to the x direction, we can simplify the Poisson equation as

$$E_x(x,y)+W_d\frac{\partial E_y'(y)}{\partial y}=\frac{1}{\varepsilon_{si}}\int_0^{W_d}\rho(x,y)dx \tag{3}$$

where W_d is the depletion width, and $E_y'(y)$ is the lateral electric field constant to the x direction.
After the integration with a triangle carrier distribution to the x direction the effective gate voltage shift ΔV_{gs} caused by the lateral electric field is written [10]

$$\Delta V_{gs}=-\frac{\varepsilon_{si}}{C_{ox}}W_d\frac{\partial^2\phi_s(y)}{\partial y^2}$$
$$=\frac{\varepsilon_{si}}{C_{ox}}W_d\{-A(V_{gs}-V_{fb})+\frac{qN_{sub}}{\varepsilon_{si}}+2AV_{bi}\}\exp\{-\sqrt{A}(L_g-y)\} \tag{4}$$

where $(L_g$-$y)$ is the distance from drain edge along the channel.
The final effective gate voltage shift ΔV_{gs} is written with some model parameters to compensate the approximations applied for deriving an analytical equation as

$$\Delta V_{gs}=\frac{\varepsilon_{si}}{C_{ox}}W_d\{-A(\mathbf{SW3}V_{gs}-V_{fb})+\frac{qN_{sub}}{\varepsilon_{si}}+2AV_{bi}\} \tag{5}$$
$$\times\exp\left[-\sqrt{A}L_g\left\langle 1-(\mathbf{SW1}+\mathbf{SW2}\{1+\log(V_{ds})\})\right\rangle\right]-\mathbf{SW4}$$

The model parameters **SW2**, **SW3** and **SW4** adjust the V_{ds} dependence of short-channel effects, the V_{gs} dependence, and the threshold voltage shift, respectively.

The calculated I_{ds}-V_{gs} subthreshold characteristics with use of the developed model are compared with 2D-device simulation results in Fig. 7 for various L_gs. It is seen that the developed model can reproduce 2D-device simulation results for different V_{ds} values. Fig. 8 compares calculated I_{ds}-V_{ds} characteristics and their derivatives with 2D-device simulation results under the on-current condition. It is seen that the agreement of HiSIM-DG calculation results with 2D-device simulation results is satisfactory for any bias conditions, even for the saturation condition. The short-channel effect was modeled on the basis of the subthreshold condition here. However, it is seen that ΔV_{gs} gives influence on the potential calculation even under the strong inversion condition as well, resulting good agreement of the calculated channel conductance g_{ds}.

Though DG-MOSFET preserves relatively good features down to L_g=40nm, clear degradation of g_{ds} at higher V_{gs} is observed. This is obvious even for L_g=100nm. This is attributed to the fact that the gate control of each side of the gate is weakened in comparison to the bulk MOSFET.

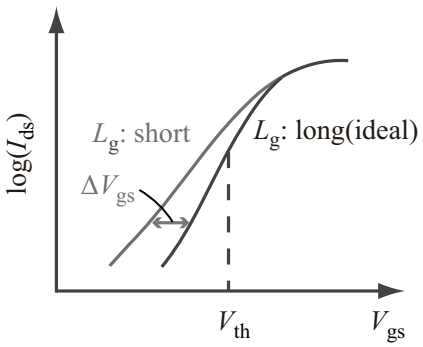

Fig. 6: Degradation of subthreshold swing with reduced gate length.

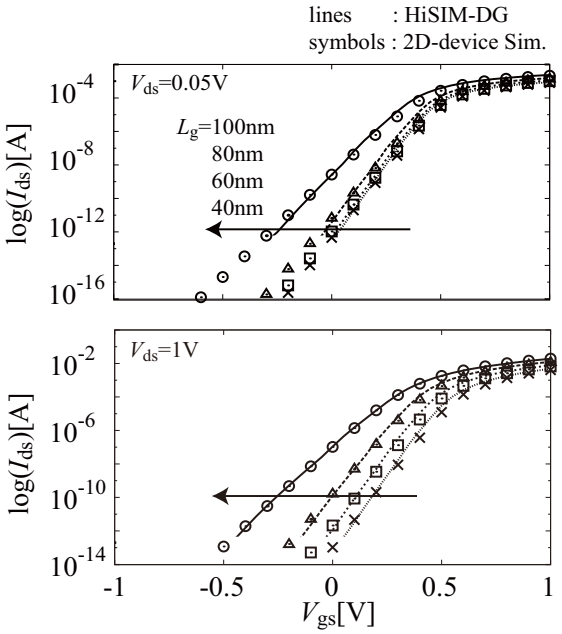

Fig. 7: Comparison of calculated I_{ds}-V_{gs} subthreshold characteristics with 2D-device simulation results with MEDICI.

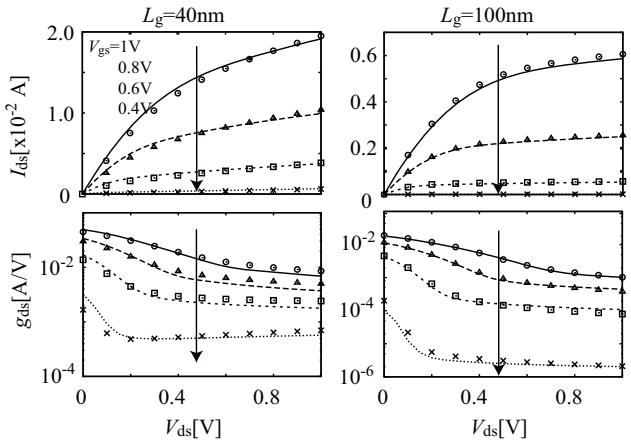

Fig. 8: Comparison of calculated I_{ds}-V_{ds} characteristics and their derivatives with 2D-device simulation results with MEDICI.

4 CONCLUSION

We have developed the DG-MOSFET model HiSIM-DG based on the complete surface-potential-based description valid both for symmetry and the asymmetrical structures.

Additionally we have developed a compact model describing the short-channel effect in DG-MOSFETs. HiSIM-DG including the developed model was verified to reproduce 2D-device simulation results for any applied bias conditions.

REFERENCES

[1] D. Hisamoto, et al., W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Boker, and C. Hu, "FinFET-A Self-Aligned Double Gate MOSFET Scalable to 20nm", IEEE TED, 47, 2320, 2000.

[2] B. Yu, L. Chang, S. Ahmed, H. wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Bokor, C. Hu, M.-R. Lin, D. Kyser, "FinFET Scaling to 10nm Gate Length", IEDM Tech. Dig., 251, 2002.

[3] E. Suzuki, K. Ishii, S. Kanemaru, T. Maeda, T. Tsutsumi, T. Sekigawa, K. Nagai, H. Hiroshima, "Highly Suppressed Short-Channel Effects in Ultrathin SOI n-MOSFET's", IEEE Transactions on Electron Devices, 47, 354, 2000.

[4] S. O'uchi, T. Nakagawa, Y. X. Liu, T. Sekigawa, E. Suzuki, K. Sakamoto, H. Koike and M. Masahara, "Calibration for Independent-DG MOSFET Compact Model Using Measured and Simulated I-V Characteristics", Proc. IWCM, 35, 2008.

[5] M. Miura-Mattausch, N. Sadachika, D. Navarro, G. Suzuki, Y. Takeda, M. Miyake, T. Warabino, Y. Mizukane, R. Inagaki, T. Ezaki, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "HiSIM2: Advanced MOSFET Model Valid for RF Circuit Simulation", IEEE Transactions on Electron Devices, 53, 1994, 2006.

[6] N. Sadachika, T. Murakami, H. Oka, R. Tanabe, H. J. Mattausch, and M. Miura-Mattausch, "Compact Double-Gate Metal-Oxide-Semiconductor Field Effect Transistor Model for Device/Circuit Optimization", IEICE Trans. Electron, E91-C, 2008.

[7] N. Sadachika, H. Oka, R. Tanabe, T. Murakami, H. J. Mattausch, and M. Miura-Mattausch, Proc. SISPAD, 289, 2007.

[8] H. Oka, R. Tanabe, N. Sadachika, A. Yumisaki, and M. Miura-Mattausch, "Suppressed Short-Channel Effect of Double-Gate Metal Oxide Semiconductor Field-Effect Transistor and Its Modeling", Jpn. J. Appl. Phys, 46, 2096, 2007.

[9] K. Ishimura, N. Sadachika and M. Miura-Mattausch, "Modeling of Subthreshold Swing and Analysis of Short-Channel Effects in Double-Gate MOSFETs", JJAP, 48, 2009.

[10] M. Miura-Mattausch, H. Jurgen Mattausch, and T. Ezaki, "The Physics and Modeling of MOSFETs Surface-Potential Model HiSIM", World scientific, 2008.