Modeling of Floating-Body Devices Based on Complete Potential Description

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ABSTRACT

Advanced MOSFETs exploit the carrier confinement to suppress the short-channel effect, which is realized by reducing the bulk layer thickness. The ongoing developments of the multi-gate MOSFET as well as the fully-depleted SOI-MOSFET with ultra thin silicon layer are proved to be applicable beyond the 50nm technology node. However, these advanced devices suffer from the floating-body effect caused by an unfixed body node, which plays an important role for the device performances. Here we present a modeling approach, based on a consistent potential description, for simplifying and solving the Poisson equation with a floating-body node.

Keywords: floating body, HiSIM, compact model, surface potential, circuit simulation

1 INTRODUCTION

The MOSFET is the most widely applied device for integrated circuits, intensively scaled down to improve the circuit performances. However, the conventional bulk MOSFET structure hits the limitation of scaling due to the inevitable short channel effect. To overcome this limitation, possible future variations such as silicon on insulator (SOI) MOSFET and double-gate (DG) MOSFET technologies have been intensively investigated and researched [1,2]. One specific feature of these devices is that they have a thin silicon layer region sandwiched by insulating oxides and that there is no electrode to tie the potential of this silicon body directly to a certain potential in order to maintain the carrier confinement.

Accurate modeling of the thin-layer MOSFETs for circuit simulation is still under development with different approaches to enable accurate circuit design with these devices [3,4,5,6]. An important aspect for the modeling is to fulfill the charge conservation, otherwise suffer from convergence problems in circuit simulations. Due to the unfixed potential value at the back side of the silicon layer, potential-based modeling, solving the potential distribution vertical to the device surface, is the best solution for the floating body devices, securing the charge conservation in a consistent way.

Consequently, we have developed compact models for the SOI-MOSFET and the DG-MOSFET by focusing on the floating-body potential distribution, based on the HiSIM (Hiroshima university STARC IGFET Model) frame work [7,8]. These models are called HiSIM-SOI and HiSIM-DG, respectively.

2 FEATURES OF THIN LAYER MOSFETS

Figure 1a-c compares the structures and band diagrams of bulk MOSFET, SOI-MOSFET and DG-MOSFET, respectively. The potential values on both sides of the oxide are determined explicitly by the applied voltages in the bulk MOSFET. Therefore the surface potential can be calculated explicitly from the boundary conditions. The SOI-MOSFET structure includes two nodes at the front side and the back-side of the thin silicon layer. The backside node can be considered as a "floating node", which is affected by the applied biases V_g and $V_{substrate}$. In DG-MOSFETs, 2 gates control the potential distribution of the silicon layer. The silicon layer thickness is usually less than the sum of two depletion layer thicknesses. Therefore the central potential cannot be determined explicitly and can be considered as a floating node.

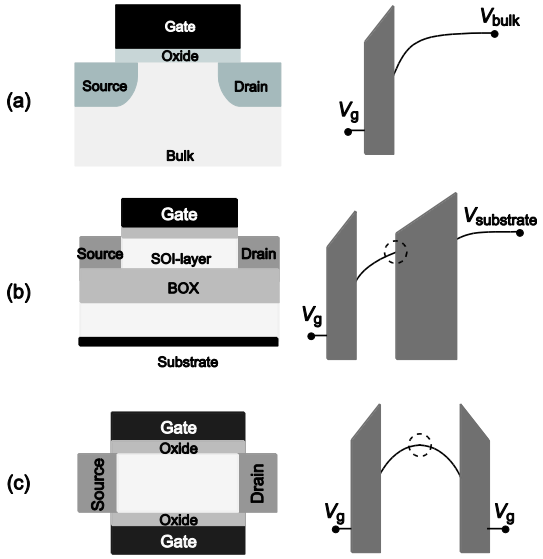

Figure 1: Schematics of structure and band diagram of (a) bulk MOSFET, (b) SOI-MOSFET and (c) DG-MOSFET. Potential values shown with ● are tied by electrodes and dashed circles show floating regions in the SOI-MOSFET and DG-MOSFET.

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3 BASIC CONCEPT OF THE SURFACE POTENTIAL BASED MODEL

HiSIM is a compact circuit simulation model based on the complete surface-potential description, which is obtained from the Poisson equation solved iteratively at the source and drain end, as shown in figure 2. The calculated potential values determine all device characteristics consistently.

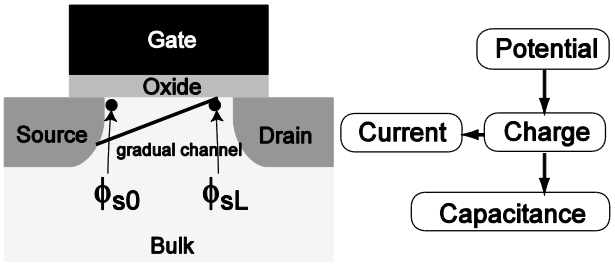


Figure 2: Basic concept of HiSIM

We demonstrate the extension of HiSIM to devices possessing a floating node within the device.

4 MODELING OF THE SOI MOSFET

To extend the frame work of HiSIM to the SOI MOSFET, and to include all device features accurately, HiSIM-SOI determines not only the surface-potential at the channel surface, but also at the 2 surfaces of the BOX (Buried Oxide) self-consistently [9,10]. The total iterative potential calculation for the 3 surfaces requires only about twice as much calculation time as in the bulk-MOSFET case solving just at the channel-surface. Figure 3 demonstrates the accuracy of the three calculated surface potentials in comparison to the results with a 2D-device simulation. Good agreement has been obtained and the floating potential at the bottom of the silicon layer is modeled accurately.

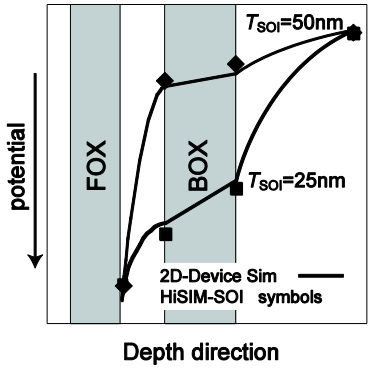


Figure 3: Calculated potential values along the depth (vertical to the channel) direction for the SOI region thickness (T_{SOI}) of 25nm and 50nm.

In the SOI-MOSFET, electron and hole pairs are generated by the impact ionization and holes accumulate in the body region, causing unexpected device behavior, which is known as the floating body effect (see figure 4). This effect greatly affects device characteristics and is modeled in HiSIM-SOI by adding the accumulated holes to the Poisson equation consistently within the iterative calculation. The accumulated holes are proportional to the impact ionization current I_{sub} [11]. Calculation results of the hole concentration are plotted in figure 5 as a function of the drain voltage in comparison with 2D-device simulation results. The acquired potential distribution along the depth direction at the source end is shown in figure 6. Due to the accumulated holes, the potential in the silicon layer is enhanced especially for high drain bias conditions where the impact ionization becomes strong.

Calculated drain currents, using the potential distributions with the accumulated holes in the SOI region (see figure 6), are shown in figure 7. Accurate determination of accumulated holes in the silicon body and consistent solution of the Poisson equation are very important to capture the floating body effect in SOI MOSFETs.

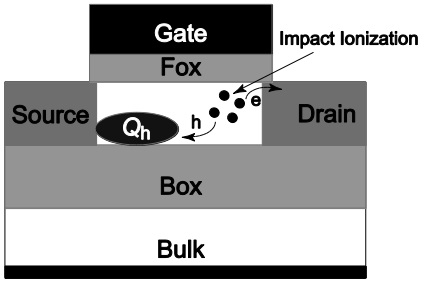


Figure 4: Schematic of the SOI MOSFET with accumulated holes due to impact ionization.

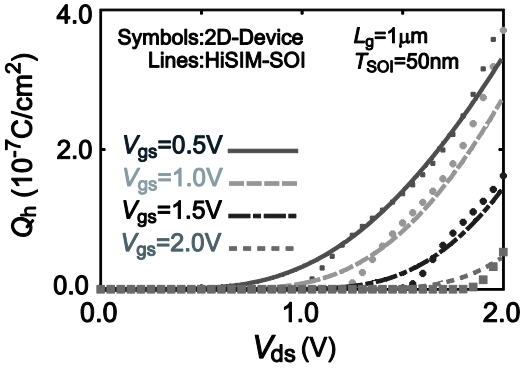


Figure 5: Comparison of the accumulated hole concentration as a function of the drain voltage as calculated by HiSIM-SOI and 2D-Device simulation for different gate voltages.

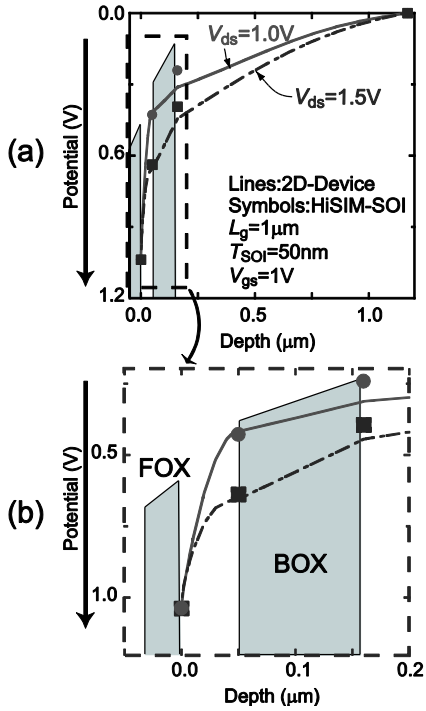


Figure 6: (a) Calculation result of the potential distribution along the depth direction considering the floating body effect for different drain biases and (b) its close up of the SOI region.

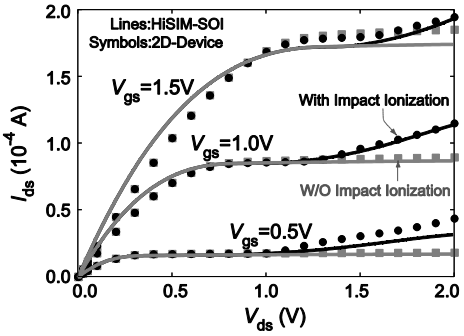


Figure 7: Calculated drain current characteristics of HiSIM SOI including the accumulated holes in the SOI region as compared with 2D-Device simulation results for L_g=1um. Calculation result without considering the impact ionization is also plotted for comparison

5 MODELING OF THE DG MOSFETS

The DG-MOSFET has a thin silicon body with another gate electrode, which enables improved channel control and results in ideal short channel effect immunity. Similar to SOI-MOSFETs, the potential value in the middle of the silicon layer is not fixed by any electrodes, as shown in figure 8 by 2D-device simulation, which makes the modeling of the device difficult. In our approach, to overcome this difficulty, the potential calculation process is divided into 2 parts. First, we solve the potential value at the center of the channel. After that, with the obtained fixed value for a "quasi" body potential, a surface potential calculation can be performed by solving the Poisson equation iteratively. In this solution example the symmetric DG MOSFET is considered, with the same thickness of the 2 gate oxides and the same voltage applied to the 2 gates.

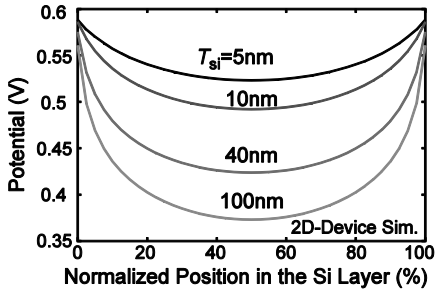


Figure 8: Potential distribution along the normalized vertical direction to the channel calculated by a 2D-device simulator. Increase of the floating node potential at the center of the channel is observed as T_{si} reduces.

Figure 9 shows the calculation result of the floating-body potential at the center, as compared with 2D-device simulation results, for different silicon layer thicknesses from 100nm to 5nm. Good agreements are achieved for this wide range of silicon layer thicknesses. Once the floating potential value is fixed, then the surface potential can be evaluated at both gates. The results are shown in figure 10 a-b as a function of gate voltage. The resulting drain currents are plotted in figure 11. Good accuracy of the potentials is of course the requirement for accurate circuit simulation.

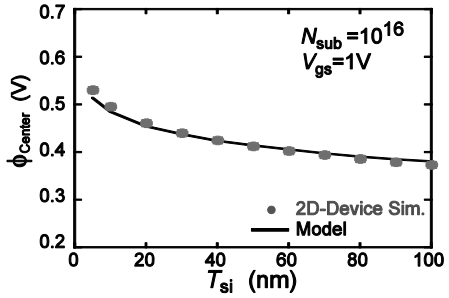
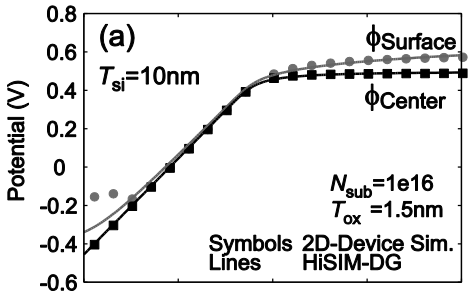


Figure 9: Comparison of the calculated floating potential value at the center of the silicon layer for different silicon layer thicknesses by the developed model and 2D-device simulation.



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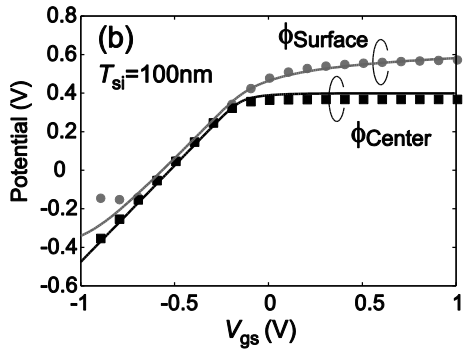

Figure 10: Comparison of potential value at the center of the silicon layer and at source-end surface in the channel as a function of the applied gate voltages by the developed model and 2D-device simulation for (a) T_{si}=10nm and (b) 100nm.

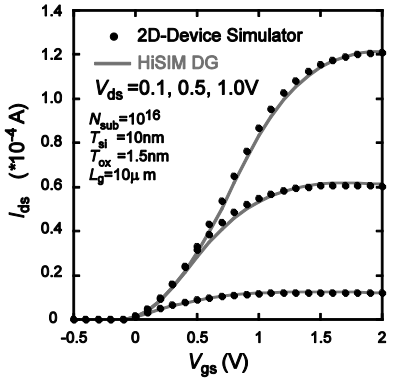

Figure 11: Comparison of calculated current voltage characteristics by HiSIM-DG and 2D-device simulation for channel impurity concentration of 10^{16} cm^{-3} and T_{si}=10nm, T_{ox}=1.5nm and L_g=10μm.

CONCLUSION

Modeling approaches for floating body devices are presented based on complete and consistent potential descriptions, and are applied to the SOI MOSFET and the double gate MOSFET. An accurate modeling of the floating potential is the key and the basis for the whole device model, because it critically affects all device characteristics.

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