Interface-trap Charges on Recombination DC Current-Voltage Characteristics in MOS Transistors

Zuhui Chen*, Bin B Jie** and Chih-Tang Sah***

*School of EEE, Nanyang Technological University, Singapore, zhchen@ntu.edu.sg
**IME, Peking University, China, bb_jie@msn.com
***University of Florida, USA, tom_sah@msn.com

Abstract

Steady-state Shockley-Read-Hall kinetics is employed to study the interface-trap charges at the SiO_2/Si interface on the electron-hole recombination direct-current current-voltage (R-DCIV) properties in MOS field-effect transistors. The analysis includes device parameter variations of neutral interface-trap density, dopant impurity concentration, oxide thickness, and forward source/drain junction bias. It shows that the R-DCIV curve is increasingly distorted as the increasing of interface-trap charges. The result suggests that the lineshape distortion observed in the past experiments, previously attributed to spatial variation of surface dopant impurity concentration, can also arise from interface-trap charges along the surface channel region.

Keywords: interface traps, interface-trap charges, MOS transistors, recombination DCIV

1. Introduction

Electron and hole generation, recombination and trapping at the SiO_2/Si interfacial electronic traps create additional currents and limit device performance characteristics, such as low stand-by dissipation-power, long operating-lifetime, low-noise amplification, and long-endurance memory. Due to the technical importance, extensive researches have been undertaken to study interfacial electronic traps at the SiO_2/Si interface in order to delineate their microscopic origins [1-3]. The generation of interface traps degrades the usable applied voltage and therefore limits device performance, and shortens the device lifetime at a given condition. Device reliability degradation may be exacerbated by strong electric field, high temperature and age since interface traps increase with time. The increasing of interface traps and interface-trap charges would eventually cause the transistor to cease functioning within the designed parameters. Thus, interface-trap charges are directly related to a transistor's reliability and critical to the proper performance of transistors.

The recombination DCIV electrical methodology was proposed as a simple and powerful tool to diagnose the operation reliability and extract submicron MOS transistor parameters with nanometer spatial resolutions [4-5]. The principle of the R-DCIV method is the use of a surface-potential-controlling gate terminal voltage to modulate the base-terminal DC current from electron-hole recombination at the SiO_2/Si interface traps to give the device and material properties. In this paper, we will explore the effect of interface-trap charges on the MOS transistor characteristics using the R-DCIV methodology. Since interface-trap density increases with the increasing of transistor write-erase cycles, investigations will focus on the effect of interface-trap charges at high interface-trap density on device characteristics, especially important for the floating-gate MOS memory transistors, which are basic units in the chips of the flash memory stick, cell phones and other portable electronics equipments. As proposed and explained by Sah [6-8], the random variations of Si-O and Si-Si bond angles and lengths along the SiO_2/Si interface generate localized perturbations which would then simultaneously create the neural interface traps with 0 or -1 charge state for neutral electron traps and 0 or +1 charge state for neutral hole traps. Thus, a paired-linear distribution of neutral interface traps with a linear energy distribution of neutral electron traps and a linear energy distribution of neutral hole traps will be theoretically studied in order to show interface-trap charge effect on transistor characteristics.

2. Theory of the R-DCIV Method

The steady-state areal rate of electron-hole recombination, R_{SS}, at a discrete energy level of interface traps with an areal density N_{IT} (trap/cm^2), is given by the Shockley-Read-Hall (SRH) formula [4-5]:

$$R_{SS} = \frac{c_{ns}c_{ps}N_S P_S - e_{ns}e_{ps}}{c_{ns}N_S + e_{ns} + c_{ps}P_S + e_{ps}} N_{IT} \qquad (1)$$

Here, c_{ns}, c_{ps}, e_{ns} and e_{ps} are the electron-hole capture-emission rate coefficients at the interface traps. N_S and P_S are respectively the surface electron and hole concentrations. The basewell-terminal recombination current I_B is obtained by integrating the SRH steady-state electron-hole recombination rate at interface traps, R_{SS}, over the channel area dydz [4-5]

$$I_B(V_{GB}) = q\iint R_{SS}(V_{GB}, y)\,dydz$$

$$= \frac{q(c_{ns}c_{ps})^{1/2} n_i W}{2} \int \frac{\{\exp[U_{PN}(y)] - 1\} N_{IT}(y)\,dy}{\exp[U_{PN}(y)/2]\cosh[U_S^*(y)] + \cosh(U_{TI}^*)} \qquad (2)$$

U_S^* is effective surface potential and U_{TI}^* is effective interface-trap energy level. $U_{PN}=V_{PN}/(kT/q)$ is the normalized forward bias applied the p/n junctions.

For a top-emitter bias configuration with $V_{DS}=0$, the gate voltage equation is given by:

$$V_{GB} = V_S + V_{FB} - Q_{IT}/C_{OX} + \varepsilon_S \times E_S / C_{OX} \quad (3)$$

Here, C_{OX} is the oxide capacitance per unit area and E_S is the electric field on the semiconductor side of the SiO_2/Si interface. The charge neutrality condition with the interface-trap charges is expressed by:

$$\rho = q \times [P - N - P_{IM} + Q_{IT}/q] = 0 \quad (4)$$

The Mass Action Law with voltage bias applied at the source and drain junctions is given by $P \times N = n_i^2 \exp(U_{PN})$. Thus, the surface electron and hole concentrations can be solved with:

$$N_S = n_i \exp(U_S - U_N)$$
$$= n_i \{[(\frac{P_{IM} - Q_{IT}/q}{2n_i})^2 + \exp(U_{PN})]^{1/2} - (\frac{P_{IM} - Q_{IT}/q}{2n_i})\} \exp(U_S) \quad (5a)$$
$$P_S = n_i \exp(U_P - U_S)$$
$$= n_i \{[(\frac{P_{IM} - Q_{IT}/q}{2n_i})^2 + \exp(U_{PN})]^{1/2} + (\frac{P_{IM} - Q_{IT}/q}{2n_i})\} \exp(-U_S) \quad (5b)$$

The electron and hole quasi-Fermi potentials, U_N and U_P, are a function of the dopant impurity ion concentration P_{IM} and the voltage U_{PN} applied to the drain, source or basewell p/n junctions in MOS transistors.

The neutral interface traps are defined as an electrically neutral trapping potential that can bind only one electron or hole. The charge formulae of the neutral electron trap Q_{ET} and neutral hole traps Q_{PT} are respectively given by [9]

$$Q_{ET} = \frac{-qN_{ET} \times (c_{ns} N_S + e_{ps})}{c_{ns} N_S + e_{ns} + c_{ps} P_S + e_{ps}} \quad (6a)$$

$$Q_{PT} = \frac{qN_{PT} \times (c_{ps} P_S + e_{ns})}{c_{ns} N_S + e_{ns} + c_{ps} P_S + e_{ps}} \quad (6b)$$

N_{ET} and N_{PT} are respectively neutral electron-trap and hole-trap concentrations. The total charge Q_{IT} is the sum of Q_{ET} and Q_{PT}, i.e., $Q_{IT}=Q_{ET}+Q_{PT}$. Poisson equation is changed to include the interface-trap charges Q_{IT} given by:

$$\varepsilon_S \nabla E = q \times [P - N - P_{IM} + Q_{IT}/q] \quad (7)$$

Then, we obtain the semiconductor surface electric field E_S:

$$E_S = \sqrt{\frac{2kTn_i}{\varepsilon_S}} \{[e^{-U_S} + U_S - 1]e^{U_P} + [e^{U_S} - U_S - 1]e^{-U_N} - \frac{Q_{IT}}{qn_i}\} \quad (8)$$

The E_S is extended to include the minority carriers from the forward bias applied p/n junctions.

The contribution of interface-trap charges is very small by comparing with P_{IM} and can be ignored even if there is one-species trap and all the traps are occupied by either electrons or holes for doped devices, which can be anticipated by in (4) and (7). However, for un-doped devices such as pure double-gate transistors, the interface-trap charges would play a very important role in charge neutrality condition and Poisson equation since interface-trap density is comparable to that of intrinsic carriers. A detailed report on interface traps in un-doped devices will be presented in a future article.

3. R-DCIV Lineshape Analysis

In the following discussion, we assume a paired-linear interface traps which includes a linear energy distribution of neutral electron traps N_{ET} with a decreasing of trap density from the conduction band edge to the valence band edge, and a linear energy distribution of neutral hole traps N_{PT} with a increasing of trap density from the conduction band edge to the valence band edge. 55 energy levels with an energy step of 20emV are used to simulate a linear energy distribution of interface traps in the silicon energy gap. For three dimension bulk model, the ratio of neutral electron traps and neutral hole traps is given by [10]:

$$R = \frac{D_{ET0}}{D_{PT0}} = \frac{1.09412}{0.5228205} = 2.095526 \quad (9)$$

D_{ET0} and D_{PT0} are the density of state respectively at conduction band edge and valence band edge. The densities of N_{ET} and N_{PT} can be respectively obtained with:

$$N_{ET} = \int D_{ET0} \times E \times dE = \frac{D_{ET0}}{2} \times E_{ET}^2 \quad (10a)$$

$$N_{PT} = \int D_{PT0} \times E \times dE = \frac{D_{PT0}}{2} \times (1 - E_{PT})^2 \quad (10b)$$

E_{ET} and E_{PT} are respectively for the energy levels of the electron and hole traps. The total interface trap density N_{IT} is the sum of N_{ET} and N_{EP}, i.e., $N_{IT}=N_{ET}+N_{PT}$. D_{ET0} is determined by the given total electron-trap density N_{ET} in (10a), while D_{PT0} is solved by (9) and the hole-trap density N_{PT} can be obtained from (10b). We assume that electron and hole capture rates are equal with $c_{ns}=c_{ps}=10^{-8}cm^{-3}/s$ and transistor temperature T is 296.57K at which the intrinsic carrier concentration is $n_i = 10^{10}cm^{-3}$. A metal gate is also assumed, and the other parameters are listed on the figures.

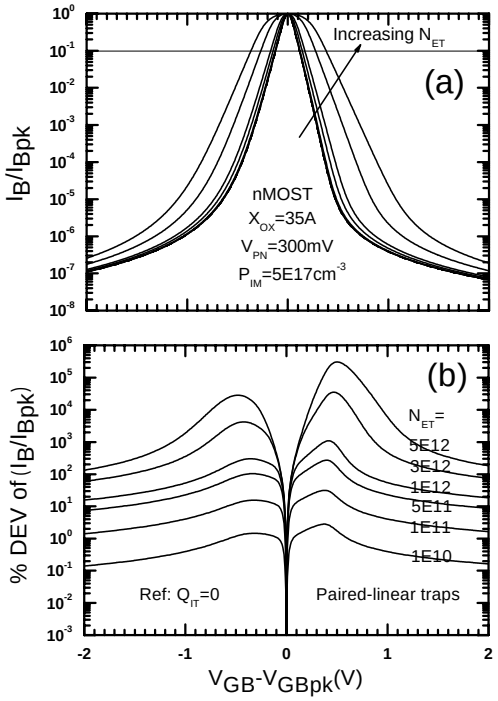

Fig. 1 Interface-trap charges on R-DCIV lineshape as a function of interface-trap density: (a) Normalized I_B vs. V_{GB} and (b) Percentage deviation. $N_{ET}=1.0\times10^{10}$, 1.0×10^{11}, 5.0×10^{11}, 1.0×10^{12}, 3.0×10^{12} and $5.0\times10^{12}cm^{-2}$.

NSTI-Nanotech 2008, www.nsti.org, ISBN 978-1-4200-8505-1 Vol. 3

The R-DCIV lineshape is primarily determined by the dopant impurity concentration P_{IM} and oxide thickness X_{OX}, and their spatial profiles at the SiO_2/Si interface [7]. However, these results were based on assumption that the energy level of interface trap is at the midgap, i.e., E_{TI}=0eV, and the interface-trap charge is zero, i.e. Q_{IT}=0. The quantitative proofs have not been reported on the effect of interface-trap charges on the R-DCIV curves. Fig. 1 shows interface-trap charges on R-DCIV lineshape as a function of interface-trap density. The neutral electron-trap density N_{ET} varies from 1.0×10^{10} to 5.0×10^{12}cm^{-2} along surface channel region and the neutral hole-trap density varies from 0.477×10^{8} to 2.386×10^{12}cm^{-2} since R= N_{ET}/N_{PT}=2.095526 for 3-D bulk model in (9). The normalized R-DCIV lineshape broadens as the increasing of N_{ET} as shown Fig. 1(a). Fig. 1(b) shows the percentage deviation of I_B/I_{Bpk} using the reference curve with Q_{IT}=0. The 90% base current range, defined by $I_B/I_{B\text{-}peak}$ = 0.1 to 1.0 shown by the horizontal line in Fig. 1(a), is covered by a gate voltage range from −0.1V to +0.1V at low N_{ET}, such as $N_{ET}=1.0\times10^{10}$cm^{-2}, and from −0.3V to +0.3V at high N_{ET}, such as $N_{ET}=5.0\times10^{12}$cm^{-2}. The percentage deviation is over 200 for $N_{ET}=1.0\times10^{12}$cm^{-2} when comparing the I_B-V_{GB} curves using the range from I_B/I_{Bpk}=0.1 to 1.0. The normalized R-DCIV curves and percentage deviations show that R-DCIV lineshape is significantly affected by the trap-density dependence of the trap charge Q_{IT}.

The recombination DCIV dependences of interface-trap charges on two most important MOS transistor parameters, dopant impurity concentration P_{IM} and gate oxide thickness X_{OX}, are shown in Fig. 2 and Fig. 3. P_{IM} varies from 1×10^{15} to 1×10^{18} cm^{-3} and X_{OX} varies from 12A to 100A with $N_{ET}=1.0\times10^{12}$cm^{-2}. Such a high interface-trap concentration is generated during repeated program-erase cycling of non-volatile floating-gate and SNONS memory transistors, recently reported by Victor Kuo of Taiwan Power Semiconductor Corporation [11]. The solid-line curves are for the device with interface-trap charge Q_{IT} while the dash-line curves correspond to the transistor without Q_{IT}, i.e., Q_{IT}=0. The percentage deviation from curves with Q_{IT}=0 is used to evaluate the interface-trap charges on device characteristics. Both figures show large deviations from curves without Q_{IT} when comparing the I_B-V_{GB} curves using the range from I_B/I_{Bpk}=0.1 to 1.0. For dopant impurity concentration $P_{IM}=5.0\times10^{17}$cm^{-3}, which is in practical range, the % deviation is over 200%. These percentage deviations indicate that the effect of interface-trap charges is not negligible when using R-DCIV method to extract device and materials parameters.

Figure 4 illustrates the interface-trap charges on the R-DCIV lineshape as a function of the forward bias (1mV to 600mV) or the injected minority carrier concentration. For small injected minority carrier concentration, the 90% base current range of R-DCIV curves covers a gate voltage range from −0.2V to +0.2V for injection V_{PN}=600mV as shown in Fig. 4(a). Figure 4(b) shows that the % deviation of interface-trap charges from zero interface-trap charge is

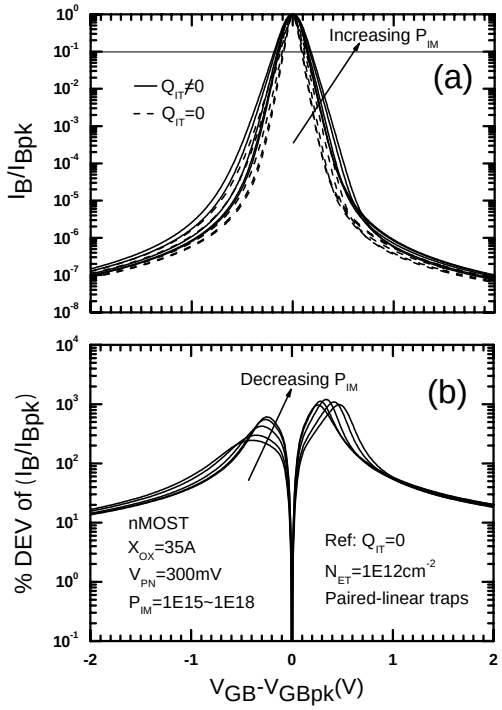

Fig. 2 Interface-trap charges on R-DCIV lineshape as a function of dopant concentration P_{IM}: (a) Normalized I_B vs. V_{GB} and (b) Percentage deviation. $P_{IM}=1.0\times10^{15}$, 1.0×10^{16}, 1.0×10^{17}, 5.0×10^{17} and 1.0×10^{18} cm^{-3}.

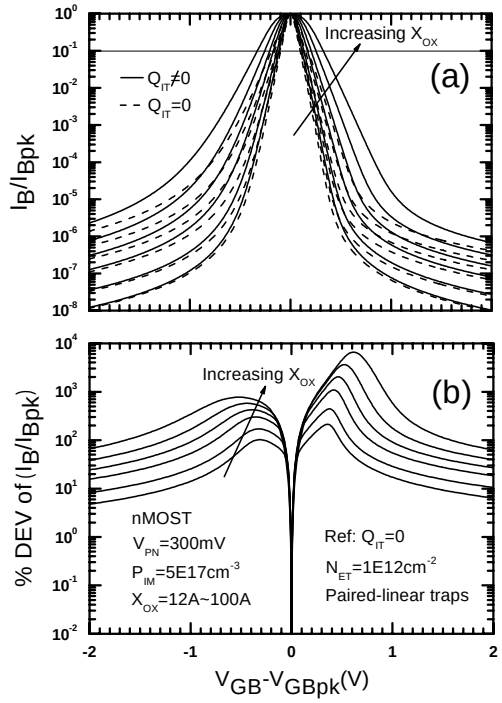

Fig. 3 Interface-trap charges on R-DCIV lineshape as a function of gate oxide thickness X_{OX}: (a) Normalized I_B vs. V_{GB} and (b) Percentage deviation. X_{OX}=12, 20, 35, 50, 70 and 100A.

over 50% for very small forward bias such as V_{PN}=1mV while % deviation is over 500% for V_{PN}=600mV when matching 90% base current range of the R-DCIV curves. The value of % deviation suggests that interface-trap charge has significant effect on the R-DCIV lineshape when forward bias V_{PN} is in practical range ($V_{PN} \leq$ ~600mV).

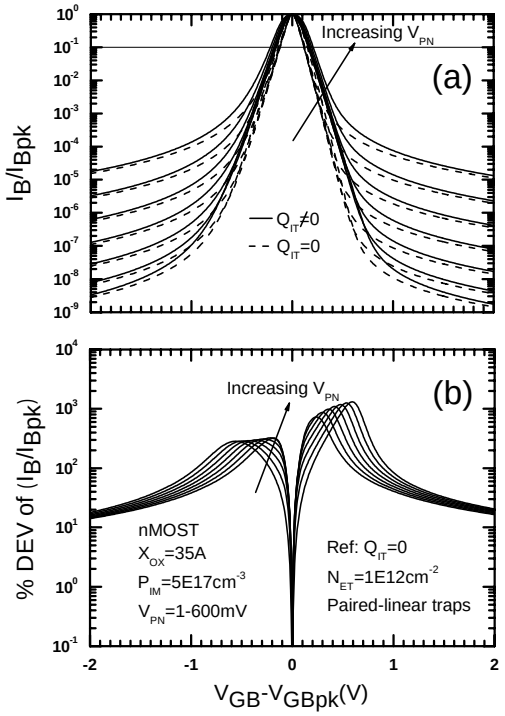

Fig. 4 Interface-trap charges on R-DCIV lineshape as a function of forward bias V_{PN}: (a) Normalized I_B vs. V_{GB} and (b) Percentage deviation. V_{PN}=1, 100, 200, 300, 400, 500 and 600mV.

The preceding analysis shows that interface-trap charges has significantly impact the R-DCIV lineshape at room temperature. Thus, the use of gate voltage formula without including interface-trap charges would cause a large loss of accuracy when extracting the parameters, especially for the mid-life devices with high interface-trap density from the R-DCIV experimental data. The fundamental reason is that the interface charge Q_{IT}, which is proportional to the interface-trap density N_{IT}, plays important role in the gate voltage equation as indicated in (3). The larger Q_{IT} would lead to greater lineshape distortion. Only for the transistors with low Q_{IT}, the R-DCIV lineshape distortion is negligible to characterize the fundamental device properties at the SiO_2/Si interface.

4. Conclusion

This paper presents a study of the effect of interface-trap charges in MOS transistors on the R-DCIV lineshape (Recombination DC- Current-Voltage) curves using the Schockley-Read-Hall thermal recombination kinetics at room temperature. Four device and material parameters over the practical range are computed to illustrate the effects on R-DCIV lineshape. Based on the theoretical analysis, we conclude that interface-trap charges significantly impact MOS transistor characteristics. The broadened R-DCIV lineshape observed in experiments can be accounted for partially by the density and profile of interface-trap charges along surface channel region, not just by the spatial variation of surface dopant impurity concentration. Thus, the gate voltage formula should include the term of interface-trap charges when using recombination DCIV methodology to extract the parameters of stressed transistors.

References

[1] O. Leistiko, A. S. Grove and C.-T. Sah, "Redistribution of Acceptor and Donor Impurities during Thermal Oxidation of Silicon," J. Applied Physics, vol. 35, pp.2695-2701, Sep. 1964.

[2] B. E. Deal, A. S. Grove, E. H. Snow, and C.-T. Sah, "Observation of Impurity Redistribution During Thermal Oxidation of Silicon Using the MOS Structure," J. Electrochem. Soc., vol. 112, pp.308-314, March 1965.

[3] Chih-Tang Sah, "Evolution of the MOS Transistor-From Conception to VLSI," Proc. IEEE, vol. 76, no. 10, pp 1280-1326, Oct. 1988.

[4] Chih-Tang Sah, "DCIV Diagnosis for Submicron MOS Transistor Design, Process, Reliability and Manufacturing," in Proceedings of the 6th International Conference on Solid-state and Integrated Circuit Technology (ICSICT), 1 (2001).

[5] Yih Wang and Chih-Tang Sah, "Lateral profiling of impurity surface concentration in submicron metal-oxide-silicon transistors," J. Appl. Phys. Vol. 90, No. 7, Oct. 2001.

[6] Chih-Tang Sah, "Insulating layers on silicon substrate," in Properties of Silicon, p. 497 (INSPEC, IEE, 1988).

[7] Chih-Tang Sah, Fundamentals of Solid-State Electronics-Solution Manual, Section 912, p. 107-108, World Scientific-Singapore, 1996.

[8] Zuhui Chen, Bin B. Jie and Chih-Tang Sah, "Effects of Energy Distribution of Interface Traps on Recombination DC Current-Voltage Lineshape," J. Appl. Phys. 100, 114511(2006).

[9] Chih-Tang Sah, "Equivalent Circuit Models in Semiconductor Transport for Thermal, Optical, Auger-Impact, and Tunneling Recombination-Generation – Trapping Processes," Phys. Stat. Sol. (a) 7, 541-549 (1971).

[10] Chih-Tang Sah, private communication by email to Zuhui Chen on April 25, 2007. This Sah model was based on the perturbation from random change of bond angle and bond length at the SiO_2/Si interface, to be published.

[11] Victor Chao-Wei Kuo, et al, "Detailed comparison of program, erase and data retention characteristics between p+poly and n+poly SONOS NAND flash memory," Proc. MTDT Conference, Aug. 2006, Taipei.