Multi-Bit/Cell SONOS Flash Memory with Recessed Channel Structure

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ABSTRACT

A novel device structure formed in recess region was presented and characterized for 4-bit/cell NOR-type nonvolatile memory (NVM) technology. The memory cells were designed to have common control gate and source line in a cell so that memory density is high. The proposed memory cell has a nitride layer formed on the surface of the recessed channel region for a charge storage node. Using channel hot electron (CHE) injection, we observed successfully ΔV_{th} and V_{th} margin of 2.8 V and 2.34 V, respectively, in 2-bit/cell operation mode without programming disturbance by adjacent storage node. The recess depth (x_{rw}) and width (x_{rd}) are 200 nm and 60 nm, respectively. By controlling doping profiles of the localized p-type channel doping in the recessed channel region, we could obtain the V_{th} margin of 1.7 V. Especially the cell size could be shrunk to $1.25F^2$/bit in a 4-bit/cell.

Keywords: multi-bit/cell, SONOS, nonvolatile, flash memory, recessed channel, localized charge trap, hot electron injection

1 INTRODUCTION

Low cost, low power, high density, and high reliability are main issues in Flash memory market. The concept of device scaling has been applied over many technology generations, resulting in consistent improvement in both device density and performance. Localized charge trapping device based on SONOS flash structures has been considered as a very promising candidate for future NVM beyond the floating gate technology, due to its various advantages. Especially, the capability of 2-bit/cell operation from the physically separated storage node is very attractive for ultra-high density memory application. The 2-bit/cell or 4-bit/cell SONOS type NVMs such as NROM™ [1], twin MONOS [2], mirror-bit [3], side wall type (or spacer) [4-5] and double SONOS [6-7] can operate as a multi-bit memory. The spacer-type and split-gate structure made possible physical isolation of bits [2-5], but were not scalable to sub-80 nm due to the difficulties in geometry controllability and performance degradation. To shrink gate length down to sub-100 nm and remove the interference between storage nodes by charge redistribution [8-9], we have proposed compact 2-bit/cell SONOS device with recessed channel structure [10-11]. However, research for higher bit-density than 2-bit/cell has not been performed.

In this paper, we propose an advanced cell concept for 4-bit/cell (or 2-Tr/cell) SONOS memory by adopting recess structure. We investigate the device characteristics of the proposed cell with an L_g of 60 nm using technology computer aided design (TCAD) device simulator [12] and show successful 4-bit/cell operation without having any interference between bits in a cell.

2 DEVICE STRUCTURE

Figure 1 shows schematic of 3-dimensional (3-D) 3×3 array view of proposed flash memory device with recess region. We tried to show key parts (source line, isolated poly gate, recessed channel region, and STI) of the device structure. The recess region is formed on the thin silicon body having wall-type shape. We can achieve high-density 4-bit/cell by sharing one control gate and one common source. The common source line located near the recessed region enables the biasing for bit programming /erasing and operates as a global bit line. The O/N/O gate stack is formed on the surface of the recessed region.

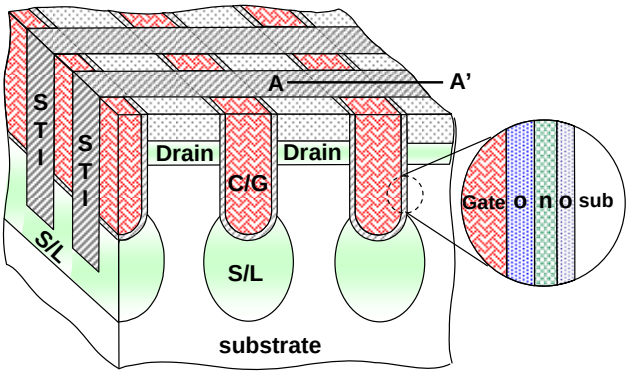


Figure 1: Schematic 3-D 3×3 array view of proposed flash memory device with recessed channel region. Each cell has 2 transistors and 4 storage nodes.

Figure 2 show 3×3 array layout of key layers (a) and schematic cell arrays (b) of our proposed flash memory cells as an example. In figure 2 (b), a cell is consisted of 2 devices which share the gate and the source, and each device in a cell can be operated independently. The bit lines and the common source lines run together vertically, and the word lines run horizontally in this figure. A cell of proposed scheme is controlled by three independent addressing lines like those of conventional 2-bit/cell

scheme. However, the memory density can be ~2 times due to the sharing. It is estimated that the cell size is ~5F^2 or a 1.25 F^2/bit in a cell. Even if we consider peripheral circuit complexity for 4-bit/cell operation, we can implement ~3 times higher bit density compared to conventional 60 nm 1-bit/cell NOR flash technology.

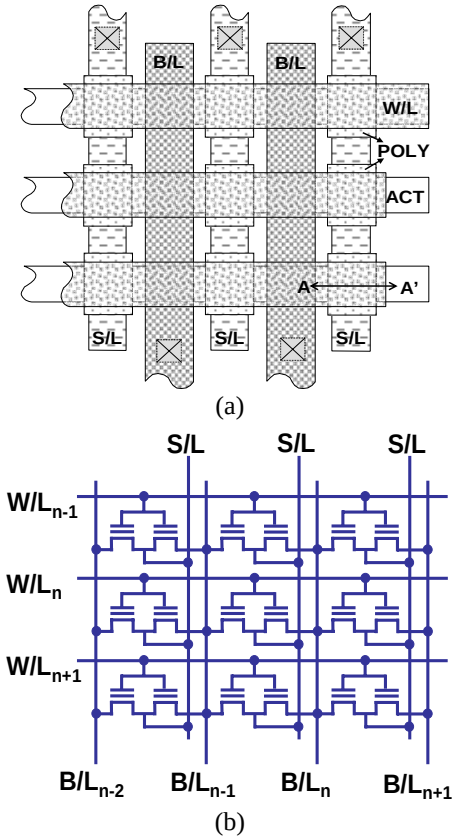


Figure 2: An example of a layout of 3×3 arrays consisted of proposed NOR-type cells (a) and its schematic cell arrays (b). The proposed unit cell has two transistors (2-Tr/cell) which shares one control gate and one source.

Figure 3 shows schematic cross-sectional view of cut along A-A' direction in Fig. 2(a). Our previous flash memory cell has recessed channel structure and floated counter doping near the bottom of the recessed region to achieve excellent 2-bit/cell (1-Tr/cell) operation. By changing the floating counter doping region to the common source region, we can achieve two 2-bit/cell devices without increasing cell area. Therefore, there are 4 storage sites (4-bit/cell) in a cell as shown in figure 3. The width (x_{rw}) and depth (x_{rd}) of the recess region are 60 nm and 200 nm, respectively. The x_{rd} is an important parameter in determining channel length. Long channel length can be possible without increasing x_{rw}, resulting in reasonable bit separation between the source and the drain sides. Thus we can achieve high density and high performance. The ONO layers have corresponding thicknesses of 4 nm (tunnel oxide), 5 nm (nitride), and 6 nm (block oxide), which is equivalent to an oxide thickness of nearly 12 nm. The local channel dopings by boron (p-type, $N_{A,peak}$=1×10^{18} cm^{-3}) are localized nearby metallurgical source and drain junctions for V_{th} control, DIBL suppression, and efficient hot carrier generation.

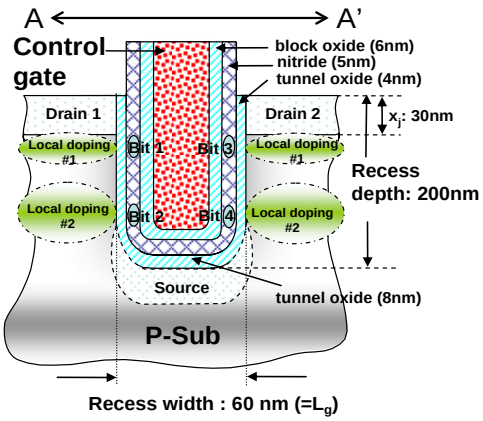


Figure 3: Schematic cross-sectional view of the proposed device structure of cut along A-A' direction. The channel length (L_g) represents the open width (x_{rw}) of the recess region. The x_{rd} and x_{rw} represent recess depth and recess width, respectively.

3 DEVICE SIMULATION AND RESULTS

Figure 4 shows simulated doping profile from the drain to the source as a parameter of ΔR_p (5 and 15 nm) of the source/drain doping profile. Uniform substrate doping is 1×10^{16} cm^{-3} and a peak concentration of a localized channel doping is 1×10^{18} cm^{-3}. ΔR_ps of the localized doping profiles near the drain and source junctions are 20 and 50 nm, respectively, by controlling ion implantation energy.

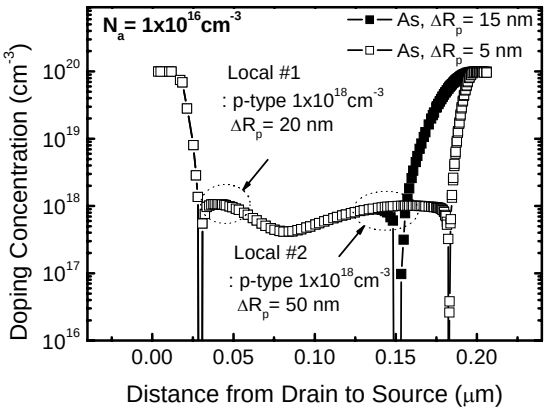


Figure 4: Simulated doping profiles along a vertical channel. Uniform substrate doping concentration is 1×10^{16} cm^{-3}. Two peak channel dopings are located near the drain and the source.

NSTI-Nanotech 2008, www.nsti.org, ISBN 978-1-4200-8505-1 Vol. 3

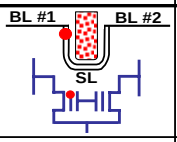
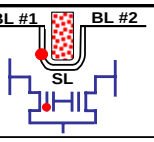
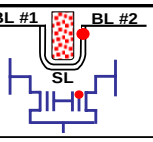
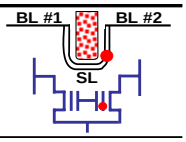
	Bit 1	Bit 2	Bit 3	Bit 4
Schematic				
PGM bias (V)	V_G= 5, V_{SL}= 0 V_{BL1}= 3.5 V_{BL2}= F*	V_G= 5, V_{SL}= 3.5 V_{BL1}= 0 V_{BL2}= F	V_G= 5, V_{SL}= 0 V_{BL1}= F V_{BL2}= 3.5	V_G= 5, V_{SL}= 3.5 V_{BL1}= F V_{BL2}= 0
ERS bias (V)	V_G= -6, V_{SL}= 0 V_{BL1}= 3.5 V_{BL2}= F	V_G= -6, V_{SL}= 3.5 V_{BL1}= 0 V_{BL2}= F	V_G= -6, V_{SL}= 0 V_{BL1}= F V_{BL2}= 3.5	V_G= -6, V_{SL}= 3.5 V_{BL1}= F V_{BL2}= 0
Forward/Reverse read (V)	V_G= sw, V_{SL}= 0/1.5 V_{BL1}= 1.5/0 V_{BL2}= F	V_G= sw, V_{SL}= 1.5/0 V_{BL1}= 0/1.5 V_{BL2}= F	V_G= sw, V_{SL}= 0/1.5 V_{BL1}= F V_{BL2}= 1.5/0	V_G= sw, V_{SL}= 1.5/0 V_{BL1}= F V_{BL2}= 0/1.5

Table 1: Summary of a schematic for a bit and bias condition for programming, erasing and forward/reverse read operation. Here 'F' and 'sw' mean floating and sweep, respectively.

It needs to be noted that a sharp peak of the channel doping near the source and drain junctions is very important to increase V_{th} margin for 2-bit/Tr.

The concept of 4-bit/cell operation of proposed device is summarized in Table 1. It shows bias conditions for programming (PGM), erasing (ERS), and forward/reverse read operation for each bit. Here 'F' and 'sw' mean floating and sweep, respectively.

To show internal physics regarding the bit programming, simulated electric field profiles from the drain to source are shown in figure 5 at programming times (t_{PGM}) of 1 ns (before) and 1 μs (after). After programming with V_D=3.5 V and V_G=5 V, V_{th} near the drain increases due to localized charge trapping, which is verified by high peak of the electric field profile near the drain.

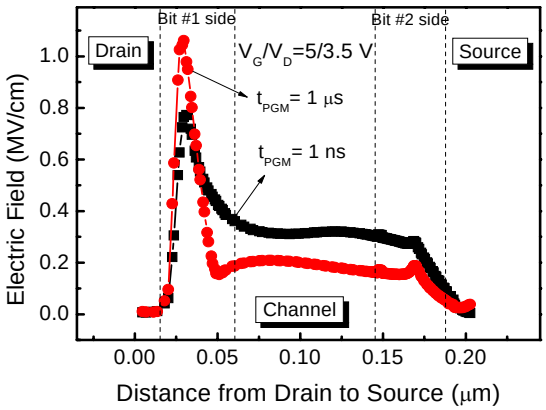


Figure 5: Simulated electric field profiles from the drain to the source before (t_{PGM} of 1 ns) and after (1 μs) programming.

To see interference between two transistors in a cell, we checked programming status of bit #3 when bit #2 is programmed. Figure 6 shows injected charges density on each storage node during bit #2 programming. Here, common gate bias is 5 V, and common source bias is 3.5 V. For the programming of bit #2, the drain2 shown in figure 3 is floated and the drain1 is grounded. Therefore, current flows from the common source to the drain1 and hot carriers are generated for programming bit #2 as a result. In figure 6, we can observe bit charges on only the bit #2. The interference between other storage nodes in a cell is impossible.

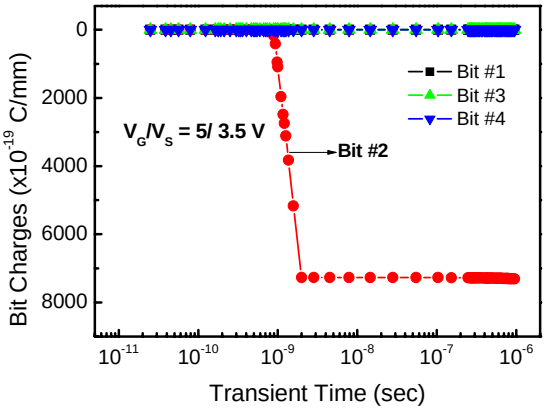


Figure 6: Injected charge density of each storage node for 1μs of bit programming. Applied V_G and V_S are 5 V and 3.5 V, respectively. The drain1 is grounded and the drain2 is floated. There is no bit charge on bit #3 during programming bit #2.

Figure 7 shows log I_D-V_G characteristics of before and after programming by injecting CHE for 1 μs at a fixed V_G of 5 V. In figure (a), V_D is 3.5 V and V_S=0 V. The bias condition in figures (b) and (c) is V_S=3.5 V and V_D=0 V. At V_D=0.1 or V_S=0.1 V after programming, the V_{th} shifts (ΔV_{th}) are about 2.8 V and 1.8 V for a bit #1 (a) and bit #2 (b), respectively. Reverse read and forward read (with V_D=1.5 V or V_S=1.5 V) are carried out immediately after each charge injection. We obtained the V_{th} margins are 2.34 V (a) and 1.4 V (b) which

is enough for 2-bit/Tr operation. By making the source doping profile more steep (ΔR_p: 15 nm → 5 nm), the V_{th} margin was improved form 1.4 V (b) to 1.7 V (c).

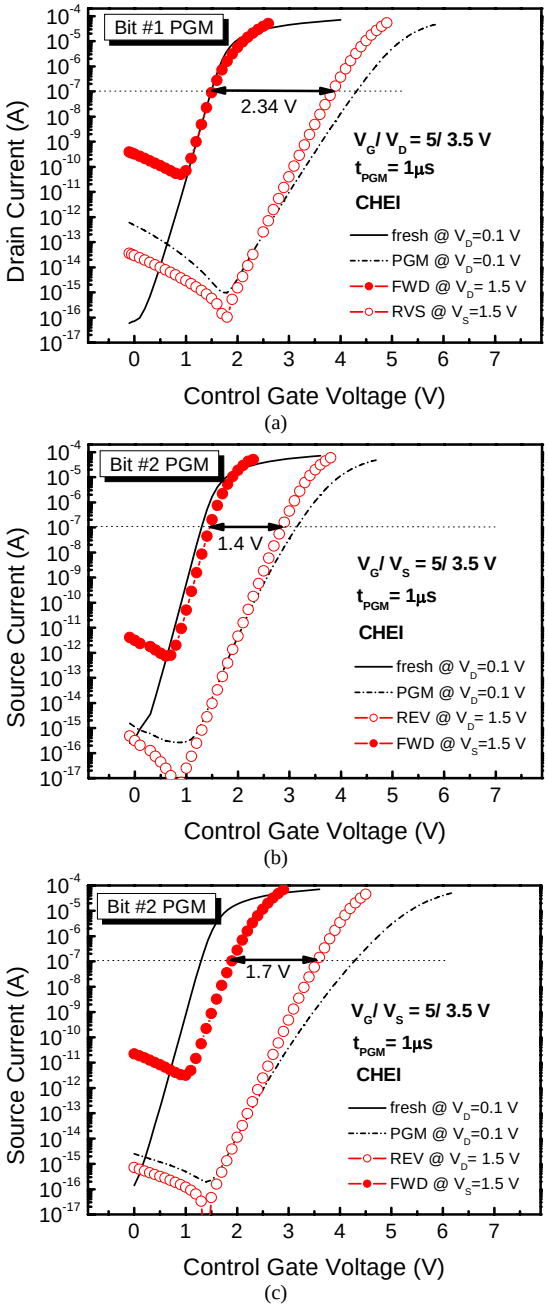


Figure 7: *I-V* characteristics before and after CHE programming of bit #1 (a) and bit #2 (b), (c). ΔR_ps of common source doping profile is 15 nm (b) and 5 nm (c).

The localized channel doping mentioned above also can help the V_{th} increase. However, the read disturbance can be happened from the by doping fluctuation. It needs to be noted that a sharp peak of the channel doping near the source and drain junctions is very important to increase V_{th} margin for 2-bit/Tr.

4 CONCLUSION

We have proposed compact 4-bit/cell SONOS flash memory device that has recessed channel structure. Since two transistors in a recessed region share the gate and the source, integration density could be very high (~3 times compared to conventional 60 nm NOR cell). Enough V_{th} margins (> 1.4 V) for 2-bit/Tr was obtained. We also have shown there is no interference between storage nodes in a cell. Our proposed device structure can be one of most promising candidates for multi-bit operation scaled NVM technology.

ACKNOWLEDGEMENT

This work was supported by "The National research program for the 0.1 Tb Non-volatile Memory Development sponsored by Korea Ministry of Science & Technology" in 2007.

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