N-channel Single Crystal Si Nanoparticle Schottky Barrier Transistor

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ABSTRACT

In this work, we report n-channel Si nanoparticle Schottky barrier transistors with a vertical current flow structure. A $YbSi_x$ Schottky barrier junction was used as a source/drain junction to make electrons majority carriers in nanoparticle transistor since the nanoparticles were intrinsic. Si nanoparticles were generated by a plasma aerosol method and directly deposited on source patterns. A layer of SiO_2 was initially used as the gate insulator. This was deposited by PECVD and annealed at 500°C in O_2 producing a final thickness of approximately 2.5nm. In subsequent lots, this layer was replaced by HfO_2 to suppress short channel effects. The physical thickness of the HfO_2 was 4.5nm. The channel length of all devices was 15nm using a Cr metal gate. The Schottky barrier height of the $YbSi_x$ junction was 0.68 eV to p-type Si. The effective electrical thickness of the HfO_2 gate oxide is 1.45nm with leakage current of $0.2A/cm^2$ at 2.0V. I_D-V_D characteristic of the initial lot show that majority carriers are electrons and that the channel carrier concentration is modulated by gate bias but it dose not saturated due to short channel effects and contact resistance.

Keywords: Nanoparticle, Schottky barrier transistor, Ytterbium silicide, Vertical transistor.

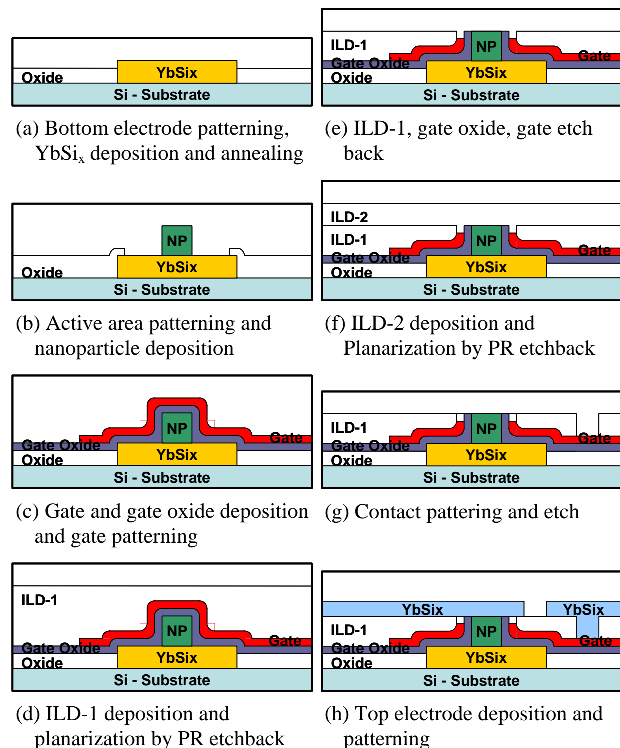
1 INTRODUCTION

Three-dimensional (3-D) integration is one of the promising novel processes to prolong Moore's Law. To achieve 3D integration, previous work has largely been based on thin film poly-crystalline transistors (TFT) [1]. However, as performance requirements in semiconductor devices increase, integration of crystalline devices over other devices, in a layer by layer manner, becomes more essential. However, it is difficult to make multi level crystalline layers on the same chip in Si based process because of thermal and process limitations.

One of new process hat has been proposed to solve this problem is the use of Si crystalline nanoparticles. A method was recently demonstrated by which single crystal silicon nanoparticles (NPs) can be deposited on any substrate without dependency on crystalline structure and substrate heating [2]. The silicon nanoparticles are intrinsic since they are undoped. These particles were then used to build discrete, single crystal transistors. In the reported device, the majority carrier is determined by the work function of the Schottky contact. Previous reports used $PtSi_x$ which has low barrier to p-type silicon, and so makes p-channel devices [3]. This paper reports n-channel single crystal silicon nanoparticle Schottky barrier transistor with 15nm channel length, Cr metal gate, SiO_2 or HfO_2 for the gate oxide and $YbSi_x$ for the source/drain junction. $YbSi_x$ shows a low barrier to n-type silicon yet retains a good ideality factor [4]. N-channel transistors were formed due to workfuction of source/drain Schottky junction. The carrier concentration was well modulated by the gate voltage.

2 DEVICE PROCESS

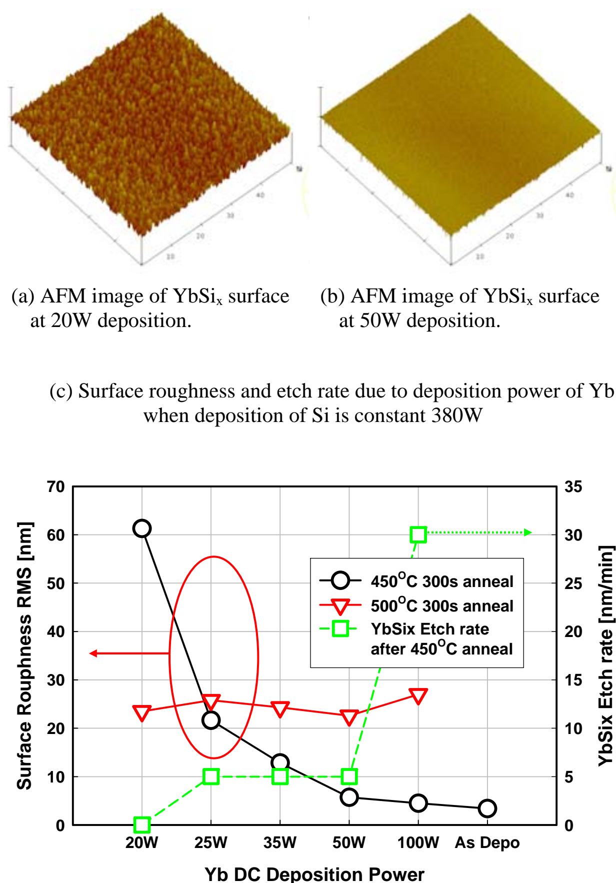
The process flow of the nanoparticle transistor is shown in Figure 1.



(a) Bottom electrode patterning, $YbSi_x$ deposition and annealing
(b) Active area patterning and nanoparticle deposition
(c) Gate and gate oxide deposition and gate patterning
(d) ILD-1 deposition and planarization by PR etchback
(e) ILD-1, gate oxide, gate etch back
(f) ILD-2 deposition and Planarization by PR etchback
(g) Contact pattering and etch
(h) Top electrode deposition and patterning

Figure 1: Process flow of silicon nanoparticle transistor.

To make the vertical transistor, the source layer was first patterned on a p-type Si substrate by co-sputtering a mixture of ytterbium and silicon. The film was annealed to from ytterbium silicide. Since the vertical structure transistor ultimately requires a three layer stack of gate oxide, gate electrode, and inter-layer dielectric (ILD) to be no thicker than the size of the nanoparticle (~35nm) [3], the surface roughness of the bottom $YbSi_x$ layer is extremely important. To obtain good surface morphology, surface roughness and electrical characteristics were examined as a function of the composition of Yb and Si in the initial film. Figure 2 shows surface roughness due to deposition power of Yb when that of Si is constant. The rf deposition power of Si was fixed at 380W because the deposition rate of Si was lower than that of Yb. The deposition power of Yb was found to be linearly correlated to deposition rate. As the Yb concentration was increased, the surface became smoother after annealing. For deposition powers less than ~100W, the unreacted concentration of Yb is high, so the $YbSi_x$ layer is easily removed by aqua regia etching after the anneal. Furthermore, a silicide did not form when the annealing temperature was below 400°C. The RMS surface roughness was found to be more that 20nm at any composition for temperatures over 500°C. An optimum annealing temperature was found to be 450°C for <5nm surface



(a) AFM image of $YbSi_x$ surface at 20W deposition.

(b) AFM image of $YbSi_x$ surface at 50W deposition.

(c) Surface roughness and etch rate due to deposition power of Yb when deposition of Si is constant 380W

Figure 2: Surface roughness and etch rate of $YbSi_x$ as a function of the Yb deposition power.

roughness when Yb and Si mixture was deposited by co-sputtering with an RF power of 380 W for the silicon and a dc power of 50W for ytterbium.

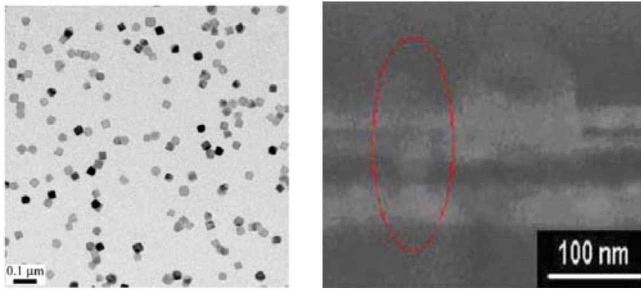
A 15nm thick oxide was deposited by PECVD at 340°C on top of this source pattern, and the active areas were defined by etching the oxide down to the silicide. After the etch was completed, cubic crystalline Si nanoparticles were deposited by non-thermal plasma CVD. The particles were 35nm size on average [3] as shown in Figure 3(a). The yield of the cubic Si nanoparticle was 90% and particle density on wafer was $1.0x10^8$ cm^{-2}. These nanoparticles were used as a transistor channels because of the large contact area and good electron mobility. And then, we etch oxide using 50:1 HF to removed nanoparticles on non-active area.

Next, the gate oxide was deposited. The first lot used the same PECVD oxide which was then annealed in O_2 at 500 °C to obtain a final thickness of about 2.5 nm. In the second batch a 4.5nm HfO_x was deposited by MOCVD at 450°C. In either case, a 15nm Cr was then deposited by evaporation to serve as the gate electrode. The thickness of the Cr acts essentially as the channel length of the transistor. The gate was then patterned and etched by CR-12 wet etchant to avoid etching damage of the gate dielectric.

The channel length and gate oxide thickness are closely related to on/off characteristics of the transistor. Generally, for a planar device, to obtain good on/off characteristics, the channel depth should be less than half of channel length [5]. For the nanoparticle transistor, the channel depth is defined by half of nanoparticle size. Since the particles are cubes, the channel length cannot be much longer than channel height. Of course, this geometry allows the gate to surround the channel on all four sides, however, control of short channel effects in this geometry is challenging. As a result, thin and reliable oxide materials are needed for good channel control. The optimum thickness of the gate oxide was determined by simulation. It was found that an equivalent oxide thickness of no more than 1.5nm is required to an inverse subthreshold slope less than 100mV/decade. These results prompted the change from SiO_2 to HfO_2.

To make top electrode and isolate the gate from the drain, a photoresist etch back process was applied to ILD planarization process. 500nm of silicon dioxide was deposited by PECVD at 340°C and coated with 1.3um of photoresist. All of the photoresist was then etched back along with 200nm of oxide. The dry etch process, which used CF_4, O_2 and CHF_3 gases, was established to have the same etch rate for the oxide and the photoresist. Next the etched back oxide was further etched by dry etch with CHF_3 and O_2 until top surface of particles were seen. This condition has high etch selectivity to Si. The gate electrode was isolated by etching with diluted CR-12 chromium etchant and the HfO_x was removed on top of Si nanoparticle by ion milling.

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061828 Vol. 1, 2007

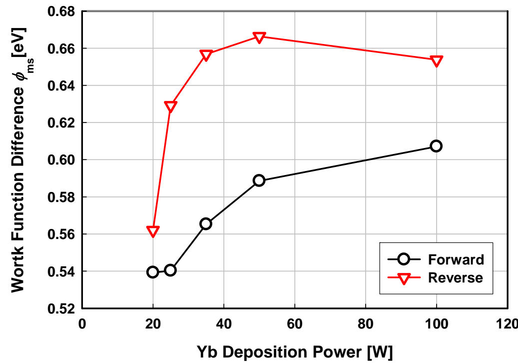


(a) TEM image of 35nm Si cube nanoparticles.

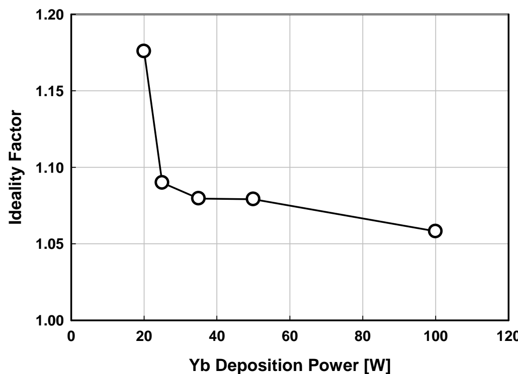
(b) SEM image of Si nanoparticles transistor.

Figure 3: TEM image of nanoparticle and SEM image of transistor.

After this, one more etch back process was done to isolate gate from the drain contact. Contact holes were then made by patterning and wet etch to connect to the gate and the top electrode. Finally $YbSi_x$ was deposited and patterned for top electrode (drain) to increase the drive current. The electrode was formed by lift off and annealing at 450°C. A cross sectional image of transistor is shown in Figure 3 (b).



(a) Schottky barrier height of $YbSi_x$ due to composition



(b) Ideality factor of $YbSi_x$ due to composition

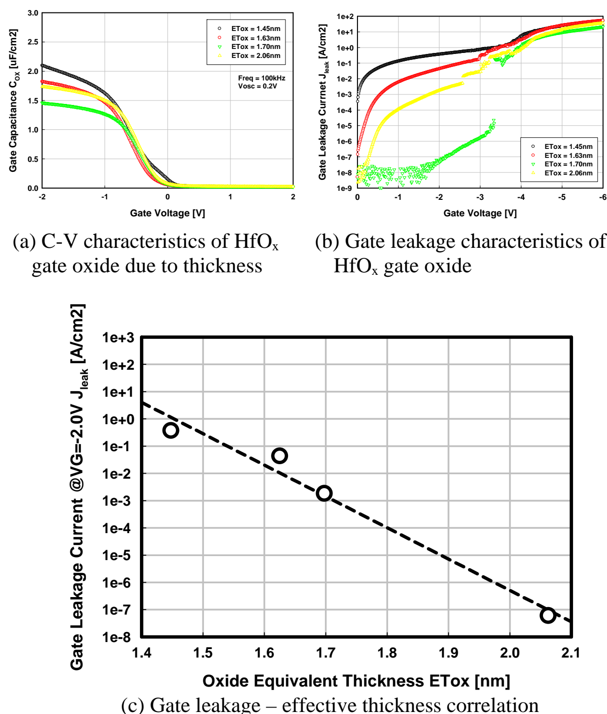
Figure 4: $YbSi_x$ junction characteristics on p-type Si.

3 RESULTS AND DISSCUSION

The electrical characteristics of $YbSi_x$ Schottky junction are shown in Figure 4. The Schottky barrier height for hole was extracted at both forward and reverse operation by temperature dependent current-voltage methods [6]. The Schottky barrier height is shown in Figure 4(a) as a function of Yb deposition power (which is proportional to the Yb deposition rate). The Schottky barrier height for holes was 0.65eV for reverse bias and 0.61eV for forward bias at 50W. This barrier lowering is due to the applied forward bias because this small applied bias reduces the barrier height, making hole injection easier. As a result, the Schottky barrier height is usually lower in forward bias [7]. In the reverse bias region, barrier height does not change much for deposition powers between 35W and 100W, however the barrier height decreases sharply for lower powers, reaching 0.56eV at 20W. Under forward bias however, the barrier height more gradually with changing powers between 25 and 100W, and dose not change below 25W. In the reverse bias region, the leakage current is influenced by surface traps at the interface between the wafer and the deposited film. The barrier height is extracted as added form of not only Schottky barrier height but also and activation energy of trap depending on trap density in current-temperature method [7]. The Schottky barrier height has a maximum with a good ideality (1.07) at 50W.

Ideality factor is shown in Figure 4 (b) by composition at 25°C. Ideality factor is extracted by linear fitting of log I_D-V_D in logarithmic region. The ideality factor decreases to 1.06 at 100W. This value is similar to previous reported results [4]. Ideality factor increases with decreasing ytterbium composition. Insufficient ytterbium can generate defects on the surface and this increased trap density may increase the ideality factor [8].

Figure 5 shows electrical characteristics of HfO_x gate oxide. The electrical characteristics on two terminal capacitor test patterns were examined on p type Si with a Cr gate. C-V characteristics are shown in Figure 5(a). The physical thickness of samples was varied from 4.5nm to 6.0nm, producing an equivalent oxide thickness from 1.45nm to 2.06nm, as extracted by the NCSU CVC model [9]. The gate leakage current characteristic is shown in Figure 5(b) in accumulation. As the gate oxide thickness decreases, the gate leakage current increases logarithmically. When the thickness is below 1.8nm, hard breakdown is not observed. The relationship between the equivalent oxide thickness and gate leakage current is shown in Figure 5(c). A 1.45nm HfO_x film was used for the Si nanoparticle transistor.



(a) C-V characteristics of HfO_x gate oxide due to thickness

(b) Gate leakage characteristics of HfO_x gate oxide

(c) Gate leakage – effective thickness correlation

Figure 5: HfO_x gate oxide characteristics on p-type Si.

Figure 6 shows I_D-V_D characteristic of n-type Si-nanoparticle transistor. As gate voltage increased, drain current is increase. This means that electrons which are supplied by source Schottky barrier junction flow from source to drain. The current is well modulated by the gate. As the drain bias increases at low gate voltage, the drain current does not saturate, indicating short channel behavior. In addition to the use of a thinner EOT high-k gate insulator, one might also want to consider the use of etching processes to selectively remove some of the nanoparticle width once the particles have been deposited on the substrate.

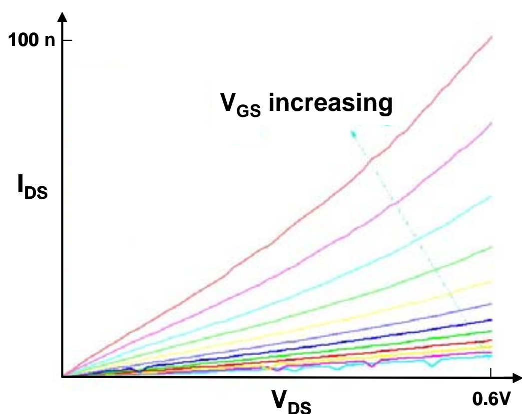


Figure 6: ID-VD characteristic of n-type Si nanoparticle transistor.

3 CONCLUSIONS

In this work, we have demonstrated n-channel single nanocrystal silicon Schottky barrier transistor with $YbSi_x$ for source/drain contact. $YbSi_x$ shows high Schottky barrier height to p-type silicon and ideal junction characteristics with ideality factor of 1.06 with 5nm RMS surface roughness. For good cutoff characteristics, HfOx was adopted for gate oxide and it shows good electrical characteristics such as leakage current of $0.2A/cm^2$ at -2.0V and breakdown voltage of -4.0V when thickness is 1.45nm. Although n-channel Si nanoparticle transistor dose not saturated well, Majority carrier of transistor was changed by workfunction of source and drain and supplied electrons are well modulated by gate.

This work shows that silicon nanoparticle transistors can be used to make complementary logic by controlling workfunction of source/drain metal contacts. This work was supported by NSF through NIRT grant DMI-0304211. Part of the work was done at the Minnesota Nanofabrication Center and the Characterization Center, both of which receive partial support from NSF through the NNIN program.

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