A Circuit Compatible Analytical Device Model for Nanowire FET Considering Ballistic and Drift-Diffusion Transport

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ABSTRACT

In this paper, we propose a quasi-analytical device model of nanowire FET (NWFET) for both ballistic and drift-diffusion current transport, which can be used in any conventional circuit simulator like SPICE. The closed form expressions for *I-V* and *C-V* characteristics are obtained by analytically solving device equations with appropriate approximations. The developed model was further verified with the measured *I-V* characteristics of a NWFET device. Results show a close match of the model with measured data.

1. INTRODUCTION

Continued scaling of transistor sizes into sub-50nm dimensions has made conventional bulk MOSFET devices vulnerable to severe short-channel effects (SCE) such as very high leakage current, poor gate control etc [1, 2]. Various device structures such as double gate fully depleted SOI (DGFDSOI), trigate and all around gate structures hence, are being extensively studied to restrict short-channel effects within a limit while achieving the primary advantages of scaling [2 - 4]. Among these devices nanowire (NW) FETs (a realistic implementation of all-around-gate structure) have recently drawn wide research interest due to their excellent short channel effect immunity compared to other contemporary device structures [5]. The superior *I-V* characteristics of NWFETs over other devices have been successfully demonstrated both theoretically and experimentally [6-8]. Subsequently, a circuit friendly compact model of these devices will further facilitate the study on their prospect in high performance circuit applications. Though several physical device models are proposed to understand and optimize the characteristics of these devices [6, 9], they are however, not quite efficient for large circuit simulations due to the complexity in solutions, which are mostly numerical. Further, most attempts on nanowire modeling assumed ballistic transport [6, 9] and neglect the more realistic drift-diffusion current conduction. It has been predicted that even in transistors of this kind with channel length below 10nm, expecting ballistic transport is quite unrealistic. A drift-diffusion model of NWFET has recently been reported, where the transistor channel is represented by a number of cascaded ballistic transistors [10]. However, the model requires that all ballistic transistors are operated in the linear region, which is not the case in reality.

In this paper, we propose a simplified circuit compatible analytical device model of NWFET for both ballistic and drift-diffusion transport, which can be efficiently used in any conventional circuit simulator like SPICE. The closed form expressions for *I-V* and *C-V* characteristics are obtained by analytically solving the device equation with appropriate approximation. We also compare the developed model with measured *I-V* characteristics of a Ge-NWFET.

The rest of the paper is organized as follows. In section 2, the developed compact model of nanowire FET is described considering both ballistic and drift-diffusion current transport. Section 3 presents the experimental verification of the above model with the measured *I-V* characteristics of a fabricated nanowire PFET followed by a conclusion in Section 4.

2. COMPACT MODEL OF NWFET

Conceptually in an NWFET, the nanowire channel is connected between the source and drain contacts, which are in thermodynamic equilibrium. Hence, the electrostatics at source and drain contacts can be described by their individual Fermi level. Since the nanowire channel is isolated from any other source of mobile carrier, source and drain are the sole source of carriers inside the nanowire channel. In such an electrostatic system, the carrier density at any sub-band (*n*th) of a nanowire channel can be expressed as [9],

$$n_p = \sum_{\upsilon} g_{\upsilon} \int_{E_{c,n}}^{\infty} \frac{D_{\upsilon}^{n}(E)}{2} \left[f(E-\mu_s) + f(E-\mu_d) \right] dE \qquad (1)$$

where $\mu_{s(d)}$ is the source (drain) Fermi level, $E_{c,n}$ be the conduction band minimum for the *n*th sub-band, $f(E)$ is the probability that a state with energy E is occupied. $D(E)$ is the density-of-states and g_{υ} is the valley degeneracy. We assume that the tunneling of carrier from gate to the channel is negligible. Due to unique geometry of NWFET, a relatively large gate insulator thickness can be used while maintaining an excellent gate control and hence, the above assumption is reasonable. Normalizing all energies and voltages by β ($k_B T/q$) and introducing one-dimensional density of states [9], the total charge in the nanowire channel can be written as

$$Q_{NW} = N_0 \sum_{\upsilon} \sum_{n} g_{\upsilon} \sqrt{m_d^{\upsilon}} \left\{ \int_0^{\infty} \frac{\varepsilon^{-1/2} d\varepsilon}{1 + e^{[\varepsilon + \varepsilon_{\upsilon}^{n} - \varphi_s]}} + \int_0^{\infty} \frac{\varepsilon^{-1/2} d\varepsilon}{1 + e^{[\varepsilon + \varepsilon_{\upsilon}^{n} - (\varphi_s - v_{ds})]}} \right\} \qquad (2)$$

where $N_0 = q\beta\sqrt{2k_B T}/(2\pi\hbar)$ and m_d^{υ} is the density of states effective mass, while $\varepsilon_{\upsilon}^{n}$ and φ_s (ψ_s/β) are the normalized conduction band minima of nth subband and surface potential, respectively. We consider the source potential as the

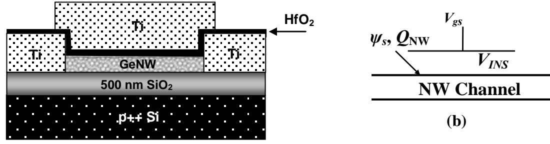

Fig. 1: (a) Schematic of a nanowire FET; (b) Schematic of potential drop across the device. The applied gate voltage (V_{gs}) partly drops across the insulator (V_{INS}) and partly across the nanowire channel.

reference potential and v_{ds} (V_{ds}/β) is the normalized drain potential with respect to source. Note that the Fermi integrals (of order -1/2) in the above equation are not solvable analytically and hence, a closed form expression for charge (Q_{NW}) can not be obtained directly. An approximate closed form solution is therefore, obtained by decoupling surface potential from the Fermi integral. It is done by dividing the operating region into two; (1) sub-threshold ($|\Psi_s|\leq|\Psi_T|$, when $\varepsilon + \varepsilon_\upsilon^n - \varphi_s >> 0$) and (2) super-threshold ($|\Psi_s|>|\Psi_T|$), and subsequently using series expansion, an analytical expression for channel charge is achieved as [11],

$$Q_{NW} = \alpha e^{\psi_s/\beta} \qquad |\Psi_s|\leq|\Psi_T| \qquad (3)$$

$$\approx \lambda_0 + \rho_1\lambda_1(\psi_s - \psi_T) + \rho_2\lambda_2(\psi_s - \psi_T)^2 \qquad |\Psi_s|>|\Psi_T|$$

where $\psi_T = E_\upsilon^n/q - 2\beta$ is the surface potential at the threshold point. α and λs are analytically obtained using the device parameters as well as considering V_{ds}, while constants ρ_1 and ρ_2 are obtained empirically. A detailed decription about the derivation of Eq. (3) can be found in [11] and hence, is omitted here.

Fig. 2 shows Q_{NW} verses Ψ_s of nanowre NFETs with different wire diameters and materials (Si and Ge) obtained from physics model and the above analytical model. Physical model represents the numerical solution of Eq. (2) and the analytical solution is obtained using Eqs. (3). It can be seen that the analytical model closely matches with physics model for all devices.

A. Ballistic Transport

Q_{NW} can further be related to gate voltage, V_g through the following voltage divider equation [see Fig. 1(b)].

$$\psi_s = V_{gs} - \phi_{ms} - V_{INS} = V_{gs} - \phi_{ms} - \frac{Q_{NW}}{C_{INS}} \qquad (4)$$

where C_{INS} is the insulator capacitance and Φ_{ms} is the work function difference. Substituting Q_{NW} in (4) an analytical closed form expression for V_{gs}- Ψ_s then can be obtained as Eq. (5), where V_T is the gate voltage (threshold voltage) corresponding to Ψ_T. Knowing Ψ_s in terms of the terminal voltages, the drain current, I_{ds} and gate input capacitance, C_G (Fig. 1) can now be obtained following Landauer approach [9] as Eq. (6).

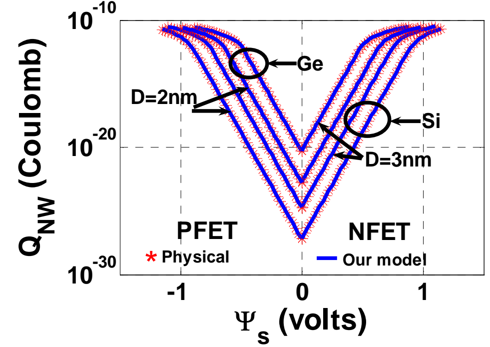

Fig. 2: Q_{NW} vs. Ψ_s of nanowire NFETs with different wire diameters and materials. Physical model represents numerical solution.

Figs. 3 and 4 show *I-V* (I_d-V_g and I_d-V_d) characteristics of a ballistic NWFET with different materials (Si and Ge). An 8nm thick HfO_2 is used as insulator and a work-function difference of 0.45eV is used for all devices. It can be observed that the above model closely matches with the physical model.

B. Drift-Diffusion Transport

Though the ballistic transport provides much higher drive current, achieving this in real devices is quite illusive. Demonstrated nanowire devices show much lower drive currents than are expected considering ballistic transport. It is hence, imperative to develop a more realistic device model considering drift-diffusion transport. Solving Eqs. (3) and (4), an analytical V_{gs}-Q_{NW} relation can also be obtained as

$$Q_{NW} = \beta C_{INS} \cdot lambertw\left[\frac{\alpha}{\beta \cdot C_{INS}} e^{(V_{gs}-\phi_{ms})/\beta}\right] \text{ for } V_{gs} \leq V_T \qquad (7)$$

$$Q_{NW} = C_{INS}\left[V_{gs} - \phi_{ms} - \psi_T + \frac{(\rho_1\lambda_1 + C_{INS})}{2\rho_2\lambda_2}\right] - C_{INS}\frac{\left[(\rho_1\lambda_1 + C_{INS})^2 - 4\rho_2\lambda_2[\lambda_0 - C_{INS}(V_{gs} - \phi_{ms} - \psi_T)]\right]^{1/2}}{2\rho_2\lambda_2} \text{ for } V_{gs} > V_T$$

The drift-diffusion current then can be obtained by

$$\psi_s = V_{gs} - \phi_{ms} - \beta \cdot lambertw\left[\frac{\alpha}{\beta \cdot C_{INS}} e^{[(V_{gs}-\phi_{ms})/\beta]}\right] \qquad \text{for } V_{gs} \leq V_T$$

$$= \psi_T + \frac{-(\rho_1\lambda_1 + C_{INS}) + \left[(\rho_1\lambda_1 + C_{INS})^2 - 4\rho_2\lambda_2[\lambda_0 - C_{INS}(V_{gs} - \phi_{ms} - \psi_T)]\right]^{1/2}}{2\rho_2\lambda_2} \qquad \text{for } V_{gs} > V_T \qquad (5)$$

$$I_{ds} = \frac{2qk_BT}{h}\sum_n\sum_\upsilon g_\upsilon\left[\ln(1 + e^{(q\psi_s - E_\upsilon^n)/k_BT}) - \ln(1 + e^{(q\psi_s - E_\upsilon^n - V_{ds})/k_BT})\right], \text{ and } C_G = \partial Q_{NW}/\partial V_{gs} \qquad (6)$$

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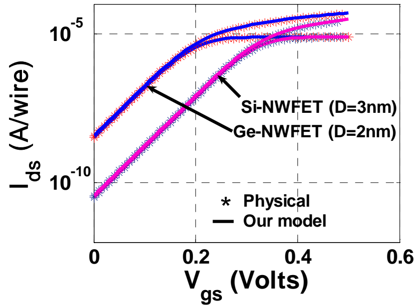
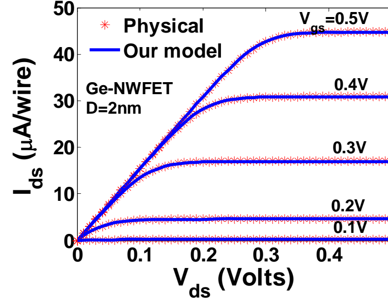


Fig. 3: I_{ds} vs. V_{gs} of nanowire NFET with different diameters and materials.



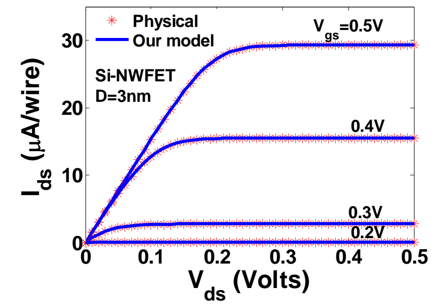


Fig. 4: I_{ds} vs. V_{ds} of nanowire NFET with materials (Ge (a) and Si (b)). HfO_2 (8nm thick) was used as insulator for all devices.

analytically integrating the following [12]:

$$I_{ds} = \frac{\mu}{L_{eff}} \int_0^{V_{ds}} Q_{NW}(V_{gs}, V_{ds}) dV \quad (8)$$

where, μ is the field dependent mobility given by

$$\mu = \mu_0 / \left[1 + \mu_0 V_{ds} / (v_{sat} L_{eff})\right] \quad (9)$$

Substituting Q_{NW} from Eq. (7), the integrations in Eq. (8) however, can not be performed in closed form and hence, further approximation on the V_{ds} dependence of Q_{NW} is required. It can be easily observed from Eqs. (1) and (2) that the channel charge with V_{ds}=0 will be twice that of for large V_{ds} (> a few kT/q) for all gate voltages. Q_{NW} dependence on V_{ds} within these two limiting values is seen to be approximately exponential in nature. While this exponential function in sub-threshold region is independent of V_{gs}, it however, depends on V_{gs} in the inversion region due to the strong correlation between the transverse and lateral electric field at the drain end. Hence, the modified charge expression with the above approximation on lateral field (V_{ds}) dependence can be re-written as

$$Q_{NW} = Q_{NW}^{*}\left(1 + e^{-V_{ds}/\beta}\right) \quad \text{for } V_{gs} \le V_T \quad (10)$$

$$Q_{NW} = Q_{NW}^{*}(> V_T)\left(1 + e^{-V_{ds}/\eta\beta}\right) \quad \text{for } V_{gs} > V_T$$

where Q_{NW}^{*} is the channel charge corresponding to large lateral field ($V_{ds} >> \beta$) and η can be expressed as

$$\eta = 1 + T \cdot (V_{gs} - V_{th})^{\gamma} \quad (11)$$

T and γ are found empirically for a nanowire structure. Fig. 5 shows the variation in channel charge of a Ge-NWFET with V_{ds} for different gate voltages. It can be seen that the above approximation closely predicts the lateral field (V_{ds}) dependency of charge. Substituting Q_{NW} now in Eq. (8) from Eq. (10) and integrating analytically, the drift-diffusion

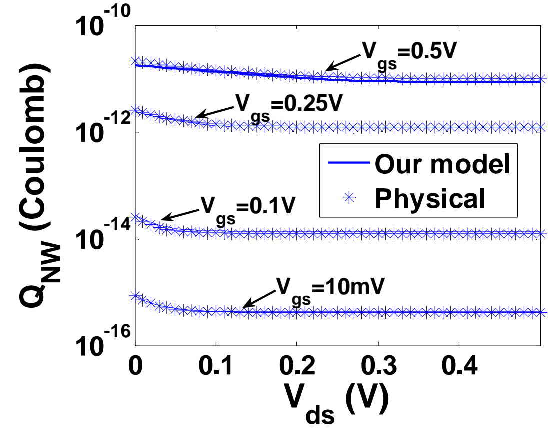


Fig. 5: Lateral field (V_{ds}) dependence of channel charge of a Ge nanowire NFET with 2nm diameter.

current can be obtained as Eq. (12).

Figs. 6 shows the *I-V* (I_{ds}-V_{gs} and I_{ds}-V_{ds}) characteristics of Si and Ge NWFETs considering drift-diffusion transport. All nanowires are considered <110> type for comparison purposes. An effective channel length (L_{eff}) of 250nm is used for all devices in the simulation. It can be observed that current considering drift-diffusion transport is considerably smaller than the ballistic current.

3. EXPERIMENTAL VERIFICATION

To further validate the above compact model the I-V characteristics of a fabricated nanowire PFET was compared. Fig. 7 shows the comparison of the above nanowire model with measured I-V characteristics. The PFET device was fabricated on a 500 nm thick SiO_2 substrate (Fig. 7a) with 250 nm long Ge- nanowire (<110>) channel (diameter = 12 nm). Schottky source drain electrodes were formed using Ti metal. An 8 nm thick HfO_2 gate dielectric was deposited

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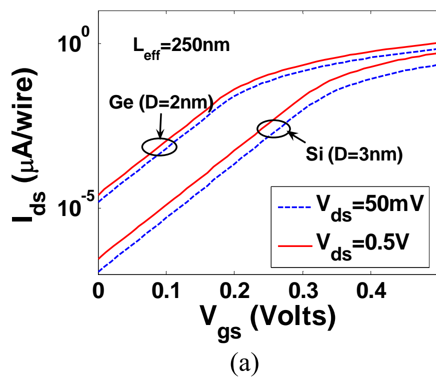
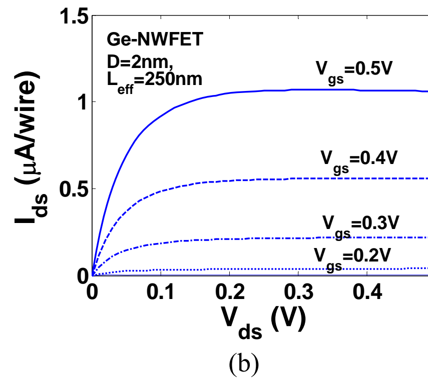
$$I_{ds} = \frac{\beta \mu C_{INS}}{L_{eff}} lambertw\left[\frac{\alpha^{*}}{\beta \cdot C_{INS}} e^{(V_{gs}-\phi_{ms})/\beta}\right]\left(V_{ds} + \beta\left[1 - e^{-V_{ds}/\beta}\right]\right) \quad \text{for } V_{gs} \le V_T \quad (12)$$

$$= \frac{\mu C_{INS}}{L_{eff}}\left(V_{ds} + \eta\beta\left[1 - e^{-\frac{V_{ds}}{\eta\beta}}\right]\right)\left[V_{gs} - \phi_{ms} - \psi_T + \frac{(\rho_1\lambda_1^{*} + C_{INS}) - \left[(\rho_1\lambda_1^{*} + C_{INS})^2 - 4\rho_2\lambda_2^{*}[\lambda_0^{*} - C_{INS}(V_{gs} - \phi_{ms} - \psi_T)]\right]^{1/2}}{2\rho_2\lambda_2^{*}}\right] \quad \text{for } V_{gs} > V_T$$



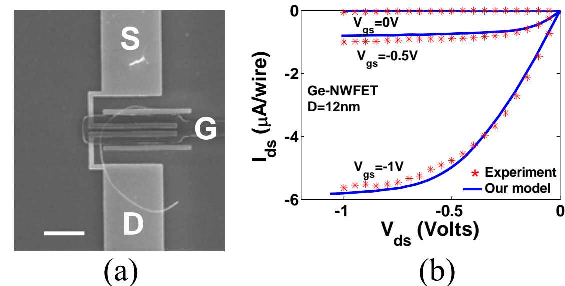
(a)



(b)

Fig. 6: (a) I_{ds} vs. V_{gs} of nanowire NFET (Si and Ge) considering drift-diffusion transport; (b) I_{ds} vs. V_{ds} of Ge-nanowire NFET considering drift-diffusion transport.

using atomic layer deposition (ALD) prior to evaporating the Ti metal gate electrode. It can be observed from Fig. 7b that the above model closely matches with the experimental results for a wide range of bias voltages. Note that we used a simple model for Schottky source/drain contact for comparison purposes because the fabricated device had Schottky contacts at both source and drain junctions. However, in reality these devices are expected to have ohmic contacts at both source and drain junctions and hence, a rigorous Schottky contact modeling may not be required.



(a) (b)

Fig. 7: (a) SEM image of a nanowire PFET. (b) Comparison of the developed drift-diffusion current model with experimental result.

4. CONCLUSIONS

In this paper, we provided an analytical compact model of NWFET for both ballistic and drift-diffusion current transport. Considering the fact that a direct closed from expression for the device characteristics can not be achieved, reasonable approximations were made to obtain an eventual analytical solution. The model is seen to be effective for a wide range of wire diameters and also showed a close agreement with experimental result. The model therefore, can be efficiently used in large circuit simulations using nanowire FETs.

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