

Discrete Dopant Fluctuated Nano Planar and FinFET Devices

Yiming Li*, Chih-Hong Hwang*, Shao-Ming Yu**, Hsuan-Ming Huang*, and Hung-Ming Chen***

* Department of Communication Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd, Hsinchu 300, Taiwan, ymli@faculty.nctu.edu.tw

** Department of Communication Engineering, National Chiao Tung University, 1001 Ta-Hsueh Rd., Hsinchu 300, Taiwan

*** Taiwan Semiconductor Manufacturing Company, No. 8, Li-Hsin Rd. 6, Hsinchu Science-Based Industrial Park, Hsinchu 300, Taiwan

ABSTRACT

In this paper, we simulate the random-dopant-induced electrical characteristics fluctuations in sub-32 nm planar MOSFET and bulk FinFET devices. A large-scale computational statistical approach is performed, in a sense of discrete atomic dopants, with a three-dimensional quantum mechanical transport device simulation. The validation of simulation technique is calibrated with silicon measured data. The fluctuation of device performance is dominated by the number and position of random dopants. Our result implies that even device has the same on-state current; the inhomogeneity of the potential that induced by the discreteness of the channel dopants strongly disturbs the carrier's conducting path at subthreshold region, and thus results in different off-state current. For the devices with the same threshold voltage, the 32-nm bulk FinFET possesses excellent immunity against the randomness of dopants due to improved gate controllability, compared with the planar device.

Keywords: MOSFET, bulk FinFET, Nanoscale VLSI devices, 3D modeling and simulation, Random dopant, Electrical characteristics, Fluctuation.

1 INTRODUCTION

As silicon technology scaling has approached the sub-100nm regime, the discreteness and randomness of dopant charges in the channel region start to introduce significant influences on device's electrical performance. The randomness nature of ion implantation and the thermal annealing processes are source of random fluctuation in nanodevices. Even in a lightly doped channel, the existence of unwanted impurity dopant will strongly influence the channel potential distribution and thus has significant impacts on device characteristics. Random dopant effect has recently been studied in several experimental and simulation studies [1-13]. These studies have shown that the fluctuations in MOSFET parameters are not purely a result of a variation in average doping density associated with a fluctuation in the number of dopants, but also the particular random distribution of dopants in the channel region [10]. Nanoscale bulk fin-typed field effect transistor

(FinFET) has recently been of great interests due to the better channel controllability over conventional planar devices [14-20].

In this paper, we numerically explore the random-dopant-induced electrical characteristics fluctuations in sub-32 nm planar MOSFET and bulk FinFET devices. A large-scale device simulation is performed, in a sense of discrete atomic dopants, by solving a three-dimensional quantum mechanical transport model. To explore the immunity and mechanism against random dopant effect, we investigate random-dopant-induced fluctuations of the two type devices, the 30nm-gate (effective gate length is 19nm) planar MOSFET and bulk FinFET, shown in Fig. 1. Effects due to the random fluctuation of the number and position of dopants in the channel region are estimated. Influence of the inhomogeneous channel potential induced by discrete dopants on the electrical characteristics is investigated. This paper is organized as follows. In Sec. 2, the simulation method is described. In Sec. 3, the fluctuation of characteristics is discussed. Finally, we draw conclusions.

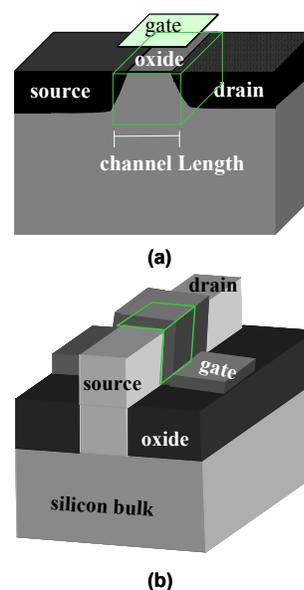


Figure 1: A schematic plot of (a) planar MOSFET and (b) bulk FinFET for the 3D simulation.

2 SIMULAITON TECHNIQUE

The simulation flowchart is shown in Fig. 2. To have the same device's operation point, the explored two devices' threshold voltage is calibrated. Both the devices' nominal channel doping concentration is $1.48e^{-18}cm^{-3}$, with the 30nm-gate length, and the gate oxide thickness is 1.2nm. The work function used in both devices is 4.4 eV. Outside the channel, the doping concentration of well and background are $5e^{19}cm^{-3}$ and $1e^{15}cm^{-3}$, respectively. Only dopant within the channel region is treated discretely.

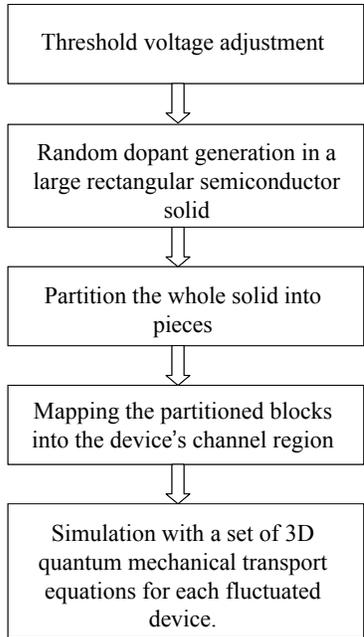


Figure 2: A flowchart of the developed simulation procedure for the random-dopant-induced electrical characteristics fluctuation.

Inside the discrete dopant region, to include the effect of random fluctuation of the number and location of discrete channel dopants, we first generate 5000 doping islands in a $150nm^3$ rectangular semiconductor solid, whose equivalent doping concentration is $1.48e^{-18}cm^{-3}$. Each doping island actually means a dopant particle and the doping concentration of each doping island is $1/V$, where V is the volume associated with a dopant. We then partition the large rectangular semiconductor solid into blocks with $30nm^3$. Each partitioned blocks are mapped into devices' channel region for the 3D device simulation with discrete dopant. The number and position of doping islands in a block are the number and position of dopants distributed in the device's channel. Then, the electrical characteristics of each discretely dopant fluctuated device are estimated by solving a set of 3D quantum mechanical transport equations. The quantum mechanical transport simulation is performed by solving a set of 3D density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations [14]. This approach computationally is

cost-effective and allows us to explore the fluctuations of electrical characteristics that induced by the randomness of dopant number and position in the channel region.

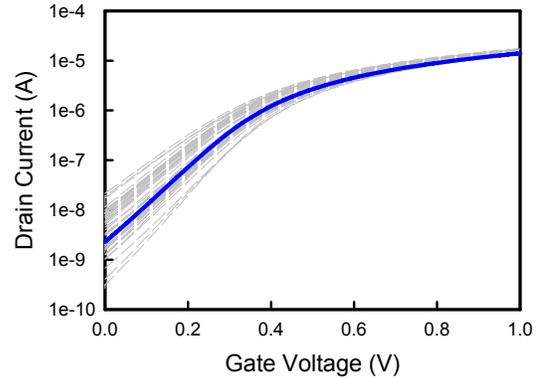


Figure 3: The I_d - V_G curves of the planar device, where the solid line is the result of continuously doped case and the dashed lines are the results of the discretely doped cases.

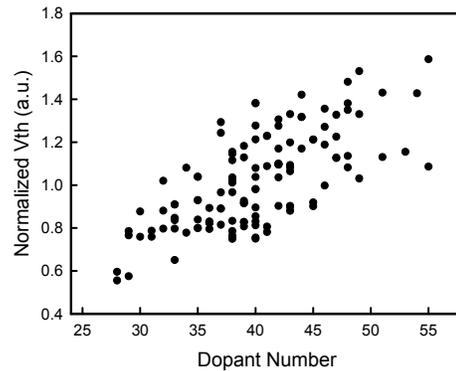


Figure 4: The plot of normalized threshold voltage of the 30nm-gate planar MOSFET with respect to dopant number.

3 RESULTS AND DISCUSSION

Figure 3 shows the I_d - V_G curves of the explored 30nm-gate planar device, where the drain voltage is 1V. The blue solid line shows the continuously doped case ($1.48e^{-18}cm^{-3}$), and the gray dashed lines are discretely doped cases. The spreading I_d - V_G curve shows the fluctuation of device's current-voltage characteristics that induced by discrete dopants. The normalized threshold voltage (V_{th}) is shown in Fig 4. The definition of threshold voltage in this paper is the smallest gate voltage as the current larger than $1e^{-7}A/\mu m$. From the random-dopant-number point of view, the equivalent channel doping concentration increases when the dopant number increases. Then, it substantially alters the threshold voltage and the on- and off-state currents. The random-dopant position induces very different fluctuations of characteristics in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases.

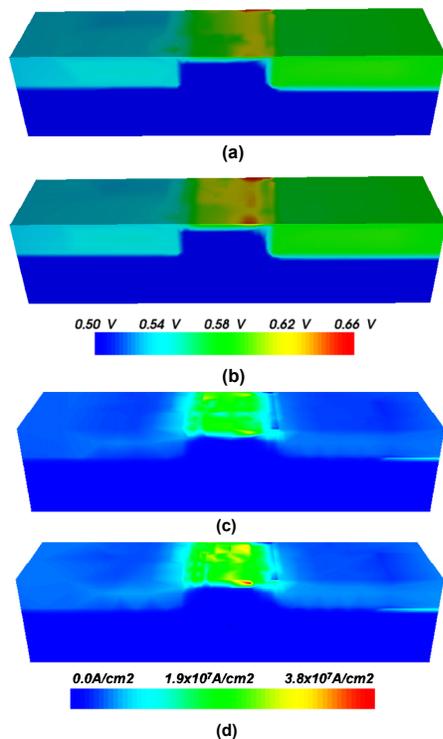


Figure 5: A 3D view of off-state potential and on-state current density of planar MOSFET devices. Plots of (a) and (c) show the results of continuously doped case and others show the results of a discretely doped case.

Figure 5 shows the 3D views of off-state potential ($V_g=1V$ and $V_d=0.05V$) and the 3D distributions of on-state current density ($V_g=1V$ and $V_d=1V$) of the 30nm-gate planar MOSFET. Figures 5(a) and 5(c) show the off-state potential and on-state current density of continuously doped case, respectively. Figures 5(b) and 5(d) are the discretely doped cases. The random-dopant-induced potential fluctuation not only influences the threshold voltage, but also the current density and current conducting path of planar MOSFET. The standard deviations of the on-state current (I_{on}), the off-state current (I_{off}), the threshold voltage, the drain-induced barrier height lowering (DIBL), and the subthreshold swing (SS) for the 30nm-gate planar MOSFET are summarized in Tab. I.

Table I: A list of estimated fluctuations for different characteristics for the explored 30nm-gate planar MOSFET.

I_{on}	I_{off}	V_{th}	DIBL	SS
$1.14 \times 10^{-6} A$	$4.62 \times 10^{-9} A$	45mV	31.4mV	14.60mV/A

Similarly, we also simulate the I_d-V_G characteristics for the 30nm-gate bulk-FinFET device, as shown in Fig. 6, where the drain voltage is 1V. Comparing the fluctuated I_d-V_G characteristics of planar MOSFET and bulk-FinFET, the spreading range of planar MOSFET is significantly larger than bulk-FinFET, which implies the worse

immunity against discrete dopant fluctuation of planar MOSFET. Also, the planar MOSFET shows significantly larger I_{off} fluctuations than bulk-FinFET. The off-state potential and on-state current density distributions of bulk-FinFET are introduced, in Fig. 7. For the devices with the same threshold voltage, the 30nm-gate length bulk FinFET possesses better immunity against the discreteness and randomness of dopants due to the improved gate controllability in bulk FinFET devices.

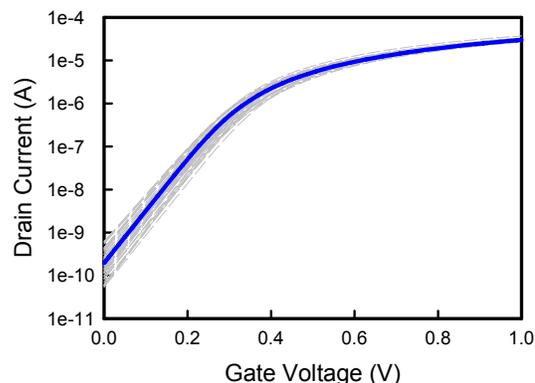


Figure 6: The I_d-V_g curves of the 30nm-gate bulk FinFET. The solid line shows the result of continuously doped case and the dashed lines are the result of discretely doped cases.

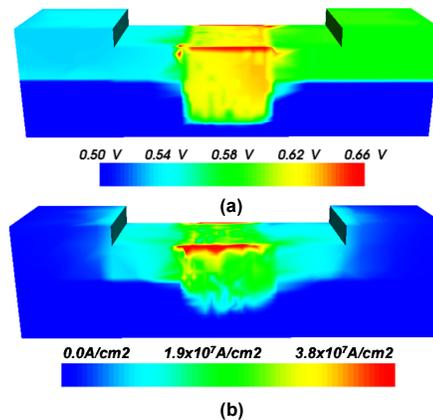


Figure 7: A 3D view of (a) off-state potential ($V_g=1V$ and $V_d=0.05V$) and (b) on-state current density ($V_g=1V$ and $V_d=1V$) for a discretely doped bulk FinFET.

4 CONCLUSIONS

In this paper, the fluctuation of electrical characteristics of nanoscale planar MOSFET and bulk FinFET have been numerically studied by a 3D “atomistic” simulation. The model includes the density-gradient equation coupling with Poisson equation as well as electron-hole current continuity equations. The fluctuations of threshold voltage, on- and off-state current, subthreshold swing, drain-induced barrier lowering, and fluctuated potential have been studied. Even

device has the same on-state current; the inhomogeneity of the potential that induced by the discreteness of the channel dopants disturbs conducting path at subthreshold region, and thus results in different off-state current. For the devices with the same threshold voltage, the preliminary result of 30-nm gate bulk FinFET shows that it possesses improved immunity against the discreteness and randomness of dopants, compared with the planar device.

ACKNOWLEDGEMENTS

This work was supported in part by Taiwan National Science Council (NSC) under Contract NSC-95-2221-E-009-336 and Contract NSC-95-2752-E-009-003-PAE, by MoEATU Program, Taiwan, under a 2006-2007 grant, and by the Taiwan Semiconductor Manufacturing Company under a 2006-2007 grant.

REFERENCES

- [1] C. Riddet, A. R. Brown, C. L. Alexander, J. R. Watling, S. Roy, and A. Asenov, "3-D Monte Carlo Simulation of the impact of quantum confinement scattering on the magnitude of current fluctuations in double gate MOSFETs," *IEEE Trans. Nanotech.*, 6, 48, 2007.
- [2] Y. Li and S.-M. Yu, "Comparison of random-dopant-induced threshold voltage fluctuation in nanoscale single-, double-, and surrounding-gate field-effect transistors," *Jpn. J. Appl. Phys.*, 45, 6860, 2006.
- [3] A. Asenov, "Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 μm MOSFETs: A 3-D "atomistic" simulation study," *IEEE Trans. Elec. Dev.*, 45, 2505, 1998.
- [4] A. Asenov, "Random dopant threshold voltage fluctuations in 50 nm epitaxial channel MOSFETs: A 3D 'atomistic' simulation study," *Solid-State Device Res. Conf.*, 45, 300, 1998.
- [5] A. Asenov, A.R. Brown, J.H. Davies and S. Saini, "Hierarchical approach to "atomistic" 3-D MOSFET simulation," *IEEE Trans. CAD*, 18, 1558, 1999.
- [6] A. Asenov, S. Kaya and A.R. Brown, "Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness," *IEEE Trans. Elec. Dev.*, 50, 1254, 2003.
- [7] B. Cheng, S. Roy, G. Roy, A. Brown, and A. Asenov, "Impact of Random Dopant Fluctuation on Bulk CMOS 6-T SRAM Scaling," *Solid-State Device Res. Conf.*, 258, 2006.
- [8] K. Samsudin, B. Cheng, A. R. Brown, S. Roy, and A. Asenov, "UTB SOI SRAM cell stability under the influence of intrinsic parameter fluctuation," *Solid-State Device Res. Conf.*, 553, 2005.
- [9] K. Samsudin, B. Cheng, A.R. Brown, S. Roy and A. Asenov, "Impact of random dopant induced

- fluctuations on sub-15nm UTB SOI 6T SRAM cells," *IEEE SOI Conf.*, 61, 2005.
- [10] M. Hane, T. Ikezawa, and T. Ezaki, "Coupled atomistic 3D process/device simulation considering both line-edge roughness and random-discrete-dopant effects," *IEEE Int. Conf. SISPAD*, 99, 2003.
- [11] H.-S. Wong and Y. Taur, "Three-dimensional "atomistic" simulation of discrete random dopant distribution effects in sub-0.1 μm MOSFETs," *IEDM*, 705, 1993.
- [12] D. J. Frank, Y. Taur, M. Jeong, and H.-S. Wong, "Monte Carlo modeling of threshold variation due to dopant fluctuations," *Symp. VLSI Circuits*, 171, 1999.
- [13] S. Toriyama, D. Hagishima, K. Matsuzawa, and N. Sano, "Device simulation of random dopant effects in ultra-small MOSFETs based on advanced physical models," *IEEE Int. Conf. SISPAD*, 111, 2006.
- [14] Y. Li, H.-M. Chou, and J.-W. Lee, "Investigation of electrical characteristics on surrounding-gate and omega-shaped-gate nanowire FinFETs," *IEEE Trans. Nanotech.*, 4, 510, 2005.
- [15] Y. Li and W.H. Chen, "Simulation of nanoscale round-top-gate bulk FinFETs with optimal geometry aspect ratio," *IEEE Conf. Nanotech.*, 2, 569, 2006.
- [16] E.J. Nowak, I. Aller, T. Ludwig, K. Kim, R.V. Joshi, C.-T. Chuang; K. Bernstein, and R. Puri, "Turning silicon on its edge [double gate CMOS/FinFET technology]" *IEEE Circuit and Device Magazine*, 20, 22, 2004.
- [17] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-C. Yeo, Y. Li, J.-W. Lee, and P. Chen, M.-S. Liang, and C. Hu, "5nm-gate nanowire FinFET," *Symp. VLSI Tech.*, 196, 2004.
- [18] A. Kranti and G. A. Armstrong, "Device design considerations for nanoscale double and triple gate FinFETs," *IEEE Int. SOI Conf.*, 96, 2005.
- [19] N. Collaert, S. Brus, A. De Keersgieter, A. Dixit, I. Ferain, M. Goodwin, A. Kottantharayil, R. Rooyackers, P. Verheyen, Y. Yim, P. Zimmerman, S. Beckx, B. Degroote, M. Demand, M. Kim, E. Kunnen, S. Locorotondo, G. Mannaert, F. Neuilly, D. Shamiryan, C. Baerts, M. Ercken, D. Laidler, F. Leys, R. Loo, J. Lisoni, J. Snow, R. Vos, W. Boullart, I. Pollentier, S. De Gendt, K. De Meyer, M. Jurczak, and S. Biesemans, "Integration challenges for multi-gate devices," *IEEE Integrated Circuit Design and Tech.*, 187, 2005.
- [20] D. Park, K. Kim, and B.-I. Ryu, "3-Dimensional nano-CMOS transistors to overcome scaling limits," *IEEE Conf. Solid-State and Integrated Circuits Tech.*, 1, 35, 2004.