Carbon Nanotube Transistor Compact Model

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ABSTRACT

In this paper, we describe the development of device models and tools for the design of the carbon nanotube FET (CNFET). Both HSPICE model and Verilog-A model for CNFET including typical device/circuit level non-idealities have been developed. They can be used for design of nanotube transistor circuits as well as to study performance benefits of the new transistor.

Keywords: Carbon nanotube transistor, CNFET, SPICE model, Compact model, HSPICE, Verilog-A

1 INTRODUCTION

The principal challenges for the semiconductor industry at the nanoscale are: (1) power and performance optimization, (2) device fabrication and control of variations at the nanoscale, and (3) integration of a diverse set of materials and devices on the same chip [1, 2].

Nanotechnology has been put forward as the key to meeting many of the challenges of the industry. New physical phenomenon and chemical/biological synthesis techniques are being explored. While there have been significant accomplishments in scientific discovery at the nanoscale, the engineering work that is required to harness the science into manufacturable technologies is just beginning.

In this paper, we focus on the use of the carbon nanotube transistor as a logic switch. While very promising experimental results have been published in the past few years, these results are mostly on a single-device level with a focus on scientific discovery. In order to develop a new transistor into a bona fide technology, an engineering approach needs to be adopted. We need to develop the necessary device models and design tools with the appropriate level of abstraction to enable the ***design*** of a useful system. This is distinct from the "science" phase of discovery and explanation of physical phenomena.

We will describe the development of both HSPICE compact model [3] and Verilog-A compact model of the carbon nanotube transistor. The model is physics-based and includes non-idealities such as carrier scattering, parasitic resistances and parasitic capacitances. Using this model, we perform circuit simulations to assess the effect of material parameter variation of the carbon nanotube on circuit performance. We obtain key information such as the delay variation as a function of the nanotube diameter and the source/drain doping level and thereby establish a realistic assessment of the expected performance of carbon nanotube transistors at the circuit level. This device model is compatible with both digital circuits design (as a logic switch) and analog circuits design (as a small signal amplifier). We illustrate the use of this model for small signal analysis through an application example [4]. The development of tools, such as the ones illustrated in this paper, will be necessary for any proposed new device to become a useful technology.

2 DEVICE MODEL TOPOLOGY

Typical layout of CMOS-like CNFET device is illustrated in Figure 1. One or multiple devices can be fabricated along a single CNT and multiple CNTs are allowed to be under the same gate in order to improve the drive current. The CNT channel region is undoped, and the other regions are heavily doped, acting as both the source/drain extension region and/or interconnects between two adjacent devices (un-contacted gate-drain / source-gate configurations). Due to the screening by the adjacent CNTs for the device with multiple CNTs, the nanotubes under the gate are grouped into (1) the two CNTs at the edges and (2) the other CNTs in the middle. All CNTs in each group are treated identically.

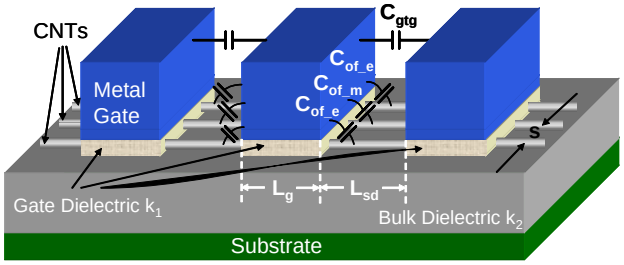

Figure 1. The 3-D structure of CNFETs with multiple channels and high-*k* gate dielectric material, and the related parasitic gate capacitances. Three CNFETs are fabricated along one single CNT. The channel region of CNTs is non-doped, and the other regions of CNTs are heavily doped.

This device model is implemented in hierarchy. The complete CNFET device model is implemented in three levels (Fig. 2). Device level non-idealities are included hierarchically at each level. Level 1, denoted as CNFET_L1, models the intrinsic behavior of CNFET. It is the core of the CNFET device model. This level corresponds to device-level models such as [5, 6]. The second level, denoted as CNFET_L2, includes the device non-idealities: the capacitance and resistance of the doped S/D CNT region, as well as the possible Schottky Barrier (SB) resistances of S/D contacts. The first two levels deal with only one CNT under

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the gate. The top level, denoted as CNFET_L3, models the interface between CNFET device and CNFET circuits. This level deals with multiple CNTs per device, and includes the parasitic gate capacitance and screening due to adjacent CNTs. Both nFET and pFET models are implemented for SPICE simulation.

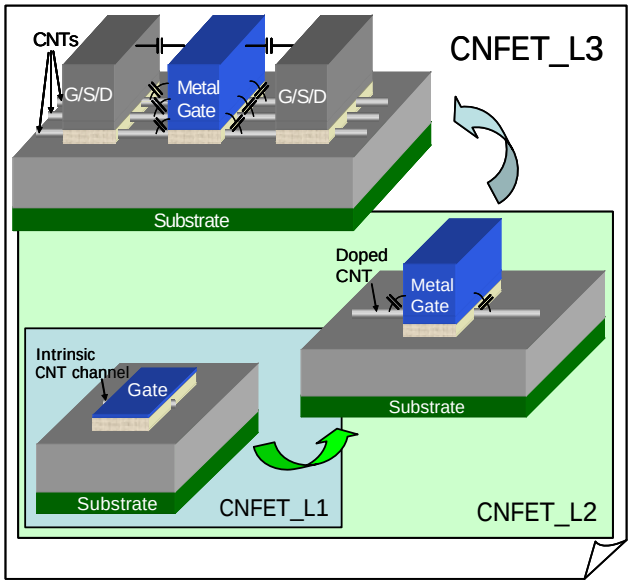

Figure 2. The device model is implemented in hierarchy. The complete CNFET device model is implemented in three levels.

For CNFET, the kinetic inductance becomes significant when signal frequency is higher than 800 GHz in the channel region and 5 TGHz in source/drain region, respectively, which are beyond our interested frequency range for most applications. Thus we ignore the inductance for CNFET device modeling.

3 HSPICE MODEL IMPLMENTATION

The first level models the intrinsic performance of CNFET with near-ballistic transport, and without any parasitic capacitance and parasitic resistance. The equivalent circuit model is shown in Figure 3. It consists of two major parts: the current sources and the trans-capacitance network to determine both dc and ac performance. C_{xy}/C_{yx} are the trans-capacitance pairs assuming the carrier distribution along the channel is uniform.

The single-walled carbon nanotube (SWCNT) is treated as quasi 1-D quantum wire in this work. We consider three current sources in CNFET model: (1) the thermomic current contributed by the semiconduting sub-bands (I_{semi}) with the classical band gap theory, (2) the current contributed by the metallic sub-bands (I_{metal}), and (3) the leakage current (I_{BTBT}) caused by the band to band tunneling mechanism through the semiconducting sub-bands.

For semiconducting sub-bands, we only consider the electron current for nFET because the hole current is usually negligible compared to the electron current due to the positive band gap.

For short channel device, with the Born-von Karman boundary condition, the total current contributed by all sub-states equals to the current flowing from drain to source (+k branch) minus the current flowing from source to drain (-k branch),

$$I_{semi}(V_{ch,DS},V_{ch,GS}) = 2\sum_{\substack{k_m \\ m=1}}^{M}\sum_{\substack{k_l \\ l=1}}^{L}\left[T_{LR}J_{m,l}(0,\Delta\Phi_B)\big|_{+k} - T_{RL}J_{m,l}(V_{ch,DS},\Delta\Phi_B)\big|_{-k}\right]$$

$$J_{m,l}(V_{xs},\Delta\Phi_B) = \frac{2e}{h}\frac{\sqrt{3}a\pi V_\pi}{L_g}\frac{k_l}{\sqrt{k_m^2+k_l^2}}\frac{1}{1+e^{(E_{m,l}+eV_{xs}-\Delta\Phi_B)/kT}}$$

where L_g is the channel length and $E_{m,l}$ is the carrier energy of the substate (m, l), the quantum numbers for the transverse and longitudinal direction, respectively. V is the source / drain chemical potential. $\Delta\Phi_B$ is the channel surface potential lowering due to gate/drain bias that is calculated with the equation solver in Fig. 3 automatically. The source input Fermi level is chosen as the reference point. V_π (~3.033eV) is the carbon π-π bond energy with tight bonding model, and 'a' is the carbon atom distance. The transmission probability T_{LR} and T_{RL} are calculated according to [3].

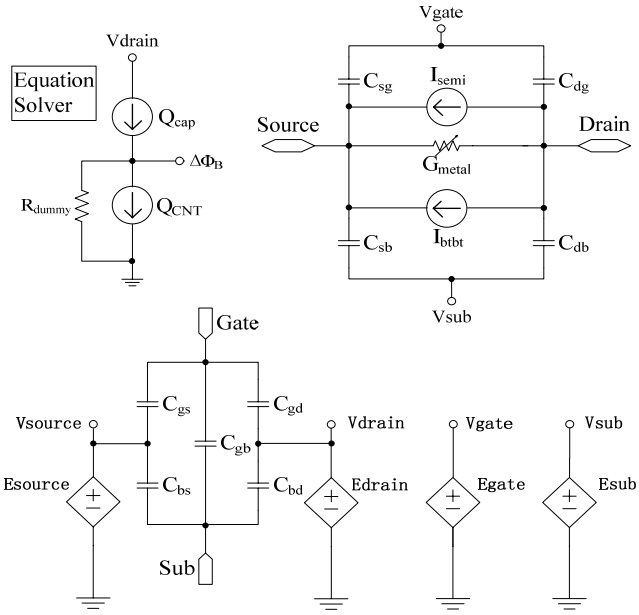

Figure 3. The 1st level equivalent circuit model CNFET_L1 for CNFET, assuming the carrier distribution along the channel is uniform. Exxx is the voltage controlled voltage source, and the potential of Vxxx equals to that of the controlling voltage source. R_{dummy} is a large value (>1E15) resistor in order to keep circuit stable.

For long channel devices (L_g >> 100nm), the wave number k_l can be represented as a continuous variable. One can either approximate the current with short device equation by setting L_g=100nm, or replacing the inner summation with integral function and assuming T_{LR}=T_{RL}=T_m, the equation can be simplified as,

$$I_{semi}(V_{ch,DS},V_{ch,GS}) \approx \frac{4e^2}{h}\sum_{\substack{k_m \\ m=1}}^{M} T_m \cdot \left[V_{ch,DS} + \frac{kT}{e}\ln\left(\frac{1+e^{(E_{m,0}-\Delta\Phi_B)/kT}}{1+e^{(E_{m,0}-\Delta\Phi_B+eV_{ch,DS})/kT}}\right)\right]$$

The metallic current of the metallic sub-band (which is only true for metallic nanotubes) is implemented as a controlled resistor (G_{metal}) with conductance $(4e^2/h)\cdot T_{metal}$ (Fig. 3). BTBT current I_{BTBT} is given by,

$$I_{btbt} = \frac{4e}{h}kT\cdot\sum_{\substack{k_m \\ m=1}}^{M}\left[T_{btbt}\ln\left(\frac{1+e^{(eV_{ch,DS}-E_{m,0}-E_f)/kT}}{1+e^{(E_{m,0}-E_f)/kT}}\right)\cdot\frac{\max(eV_{ch,DS}-2E_{m,0},0)}{eV_{ch,DS}-2E_{m,0}}\right]$$

$$T_{btbt} = \frac{\pi^2}{9}\exp\left(-\frac{\pi m^{*(1/2)}(\eta_m 2E_{m,0})^{3/2}}{2^{3/2}e\cdot\hbar\cdot\varepsilon}\right)$$

The second level device model includes the device level non-idealities, including the defect/impurity scattering in the channel region, the quantum/series resistance and the parasitic capacitance of the doped source/drain region, as well as the Schottky barrier (SB) resistance at the interface between the doped CNT and the source/drain metal contacts. The third level, i.e. the top level of the device modeling, allows multiple CNTs for each device. Assuming there are a number of N nanotubes under the gate, they are grouped into (1) a number of min(N,2) CNTs at the two edges and (2) the other N-min(N,2) CNTs in the middle. All CNTs in each group are treated identically, thus there are two components within one device. By specifying the parameter "s" (the inter tube pitch) for each device, the screening effect of parallel CNTs on both the current drive and the coupling capacitance are taken into account automatically by the device model. To be compatible with CMOS process, we assume CNFET circuits use the same interconnect technology (the feature size is defined by photolithography) as that for silicon technology.

4 VERILOG-A IMPLMENTATION

Due to limitations imposed by HSPICE, the resulting model is not fast enough to be used to simulate complex circuits. To improve the simulation speed of the carbon nanotube model, the HSPICE subcircuit model has been rewritten into Verilog-A. Traditionally, compact device model, such as the BSIM models, are written in C. Nevertheless, Verilog-A has been proposed as the standard language for compact device modeling in recent years due to its many advantages [7, 8]. In particular, Verilog-A enables models to be developed quickly and reliably by abstracting model developers from calculating error-probe partial derivative and complicated simulator interfaces. While most major commercial simulators support compact models written in Verilog-A, the model also has the advantage that it is portable to other simulators such as Spectre [9].

In order to verify the Verilog-A model, benchmark circuits which evaluate the static and transient performances of the model have been used. Table 1 shows simulation times required by the two models for some benchmark circuits. Compared with its HSPICE subcircuit counterpart, the implemented Verilog-A model runs approximately five and seven times faster for DC and transient simulations, respectively. This dramatic improvement in simulation speed enables us to simulate more complex circuit with more computational intensive analysis in a reasonable amount of time.

Circuit	HSPICE model	Verilog-A model	Speed Gain
1 (DC)	2.00s	0.35s	**5.71**
2 (DC)	2.10s	0.40s	**5.25**
3 (Transient)	20.5s	2.80s	**7.32**
4 (Transient)	20.7s	2.70s	**7.67**
5 (Transient)	41.0s	5.30s	**7.74**
6 (Transient)	60.9s	7.90s	**7.71**

Table 1: Comparison of HSPICE and Verilog-A models

SUMMARY

This paper describes the development of device models for CNFET including typical device/circuit level non-idealities. This device model is implemented in hierarchy. The complete CNFET device model is implemented in three levels. Device/circuit level non-idealities are included hierarchically at each level. Both HSPICE model and Verilog-A model have been implemented. Compared with HSPICE subcircuit counterpart, the Verilog-A model runs approximately five and seven times faster for DC and transient simulations, respectively. This large run-time improvement enables us to simulate more complex circuit with more computational intensive analysis in a reasonable amount of time.

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