Hybridization of CMOS with CNT-Based Complementary Nano Electro-Mechanical Switch for Low-Leakage and Robust Embedded Memory Design

Rajat Subhra Chakraborty, Seetharam Narasimhan, and Swarup Bhunia
Department of EECS, Case Western Reserve University
Cleveland, Ohio, USA
{rsc22, sxn124, skb21}@case.edu

ABSTRACT

In the nanometer era of VLSI technology, exponential increase in leakage power with technology scaling has become a major design concern. Embedded Static Random Access Memory (SRAM) is a major part of modern nanoelectronic systems. However, over the years, the integration density of SRAM has increased steadily along with associated increase in leakage power and decrease in robustness. The decrease in robustness often manifests itself as "failures" in basic memory operations like read, write and hold. Carbon nanotubes (CNTs), in recent times, have generated a lot of interest because of their exceptional electrical, mechanical and thermal properties, which have motivated investigations on building nano electro-mechanical system (NEMS) switches with them. In this paper, we propose integration of a specific CNT-based NEMS complementary switch with CMOS SRAM cells to achieve significant decrease in memory leakage power (~19X) and increase in robustness due to bitline leakage reduction (~55X).

Keywords: Leakage Reduction, Static Random Access Memory (SRAM), Carbon Nanotube (CNT), Nano Electro-Mechanical System (NEMS).

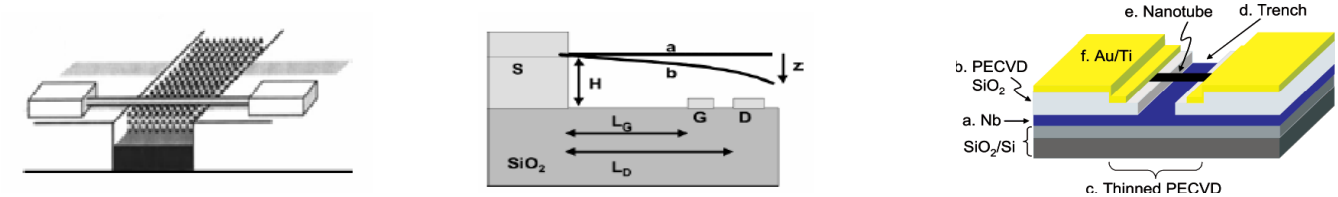
1 INTRODUCTION

One of the major challenges with aggressive technology scaling is the dramatic increase in the leakage power at each technology generation. At nanometer scale, CMOS devices suffer from severe "short-channel effects" [1], which combined with greater gate-oxide tunneling leakage, result in large device current in the "off" state. In fact, leakage power is predicted to constitute nearly 50% of chip power at sub-65nm CMOS technology nodes. This phenomenal increase in wasted power is clearly unacceptable, more importantly in mobile battery-operated systems. In memory circuits, the effect of leakage is also manifested as a decrease in robustness of read, write and hold operations, and it is aggravated by the large die-to-die and within-die process variations in the nanometer technology nodes [2].

Numerous leakage reduction techniques have been investigated for SRAM circuits. A very effective leakage saving technique for memory circuits that has been widely investigated is source biasing [3], which "gates" the supply and applies a positive bias voltage in the source of the NMOS transistors (of each memory cell), such that the rail-to-rail voltage is reduced resulting in leakage reduction. The technique selects a bias voltage in such a way that ensures data retention while minimizing cell leakage.

To address some of the issues with nano-scaled CMOS logic and memory, several new devices have been proposed as alternative to CMOS at the end of its roadmap [4]. They include carbon nanotube-based FET (CNTFET), molecular electronic switches, ferromagnetic logic devices, resonant tunneling devices, single electron transistors (SET) and quantum-dot cellular automata (QCA). Although some of these devices offer promising features in terms of device operation, integration density, power and performance, however, the potential of these devices in near future is limited by the following facts: a) fabrication of these devices typically involves prohibitive cost; b) the manufacturing defect rate as well as impact of parameter variations are predicted to be unacceptably high; and c) a rapid transition to a fundamentally new device and/or computational paradigm is less feasible. It would be beneficial to be able to use the vast resources of design and analysis tools available for traditional CMOS design.

In this paper, we propose a novel hybridization scheme which can extend the effectiveness of CMOS memory technology in nanometer regime using Nano Electro-Mechanical Systems (NEMS) switch as leakage control elements in static random access memory. A NEMS switch with specific characteristics referred as *"Complementary Nano Electro-Mechanical Switch" (CNEMS)*, having



(a) (b) (c)

Fig. 1: (a) Self-assembled switches based on electroactuated multi-walled nanotubes [6]; (b) Three-terminal carbon nanorelay of a CNT cantilever beam switch [7]; (c) Single-walled nanotubes (SWNTs) suspended over shallow trenches in SiO_2, with a Nb pull electrode [8].

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carbon nanotubes (CNTs) as switching elements is investigated as a structure to control leakage in CMOS memory array. We show that the proposed implementation can cause substantial decrease in cell leakage power. The hybridization can also effectively reduce the bitline leakage improving the read noise margin of the memory circuit. Thus the proposed technique allows the existing SRAM design techniques and design automation tools still applicable while addressing the leakage and robustness issues with CNEMS.

2 STRUCTURE OF CNEMS AND ITS WORKING PRINCIPLE

In this section, we briefly describe carbon nanotube based NEMS switches and then present the working principle, a possible hybridization approach, and equivalent electrical model of CNEMS.

2.1 Use of Carbon Nanotubes (CNTs) as NEMS Switch

The use of carbon nanotubes as an alternative technology for CMOS in electronic circuits is a concept which has emerged in the recent years, since this structure was reported in [5]. Along with CNT-based Field Effect Transistor (FET) that exploits the semiconductor property of CNT, design of NEMS using CNT has been intensively investigated. CNTs are observed to be particularly suitable for NEMS applications due to their well-characterized physical and chemical properties and their exceptional electrical and mechanical behavior. In recent years, many different NEMS switches based on carbon nanotubes have been proposed. Fig. 1(a-c) presents several recent CNT-NEMS devices, two of which can operate as cantilever structures [6-8]. In [6], a switch based on multi-walled CNT cantilever structure suspended over metallic trenches has been described. The switching behavior is observed by noting the current at the bottom electrode, which shows an abrupt increase beyond a certain "threshold" voltage difference between the nanotubes and the bottom electrode. However, the chief limitation of the device is the low ON-state current (~0.4nA) at a bias voltage of around 3V. In [7], a three-terminal multi-walled carbon nanorelay has

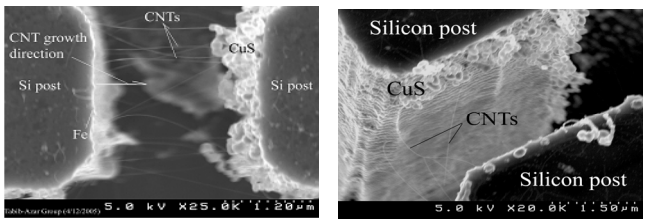

Fig. 2: CNTs we have grown using a metal-catalyzed (iron) chemical vapor deposition technique using C_2H_2 between two raised silicon posts (left). Self-aligned and welded CNTs can be grown into any layer that can withstand 500-800°C. CNTs grown into Cu layer that was subsequently sulfidized (right).

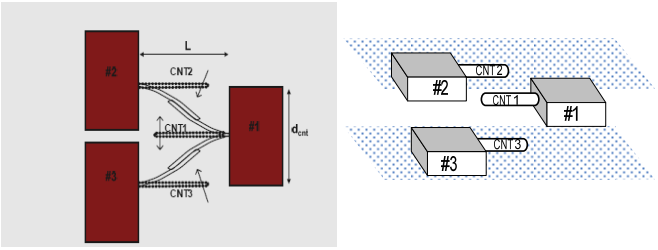

Fig. 3: CNEMS structure [9]: top view (left) and side view (right) of the switch. The central CNT (CNT1) is either touching the top (CNT2) or the bottom (CNT3) one.

been presented. The switch operates by the application of voltages between two electrodes, which the authors describe as "Source" and "Gate", and the current is measured at the "Drain" electrode. However, the device operates at comparatively high voltage (Vsg ~ 25V), and there is considerable fluctuation in its ON current. In [8], the authors report the operation of an electromechanical carbon nanotube switch. However, this structure also has comparatively low ON current (~250nA) and shows large random fluctuations in the ON-state current.

2.2 CNEMS Structure and Operating Principle

Compared to the CNT-NEMS switches described in the previous subsection, the complementary switch (CNEMS) proposed in [9, 12] has certain properties which make it suitable for hybridization with CMOS as a leakage reduction and data retention device. We have developed a metal-catalyzed chemical vapor deposition technique to grow self-aligned and welded CNTs suitable for this structure, as shown in Fig. 2. This growth process can be extended for fabrication of CNEMS and its subsequent hybridization with CMOS.

Fig. 3 shows the top and side views of the proposed switch. The operating principle of this structure has been described in details in [9]. The switch contains three co-planar CNTs of cantilever geometry, which are initially unconnected. The switch in this case acts like a mechanical relay rather than an electronic switch and can be toggled between two complementary configurations by the application of a voltage pulse between the central CNT and either of the two side CNTs. Once configured in a certain way, the switch remains in the same state until an opposite electric field is applied to reconfigure it. This is because of the van der Waals' interaction between the carbon nanotubes. Due to this latching mechanism, each switch works as a nonvolatile memory element. The critical physical parameters of the structure such as turn-on voltage and switching speed can be estimated from the system total energy considerations as described in [9]. The salient features of CNEMS are: a) low-voltage operation (~1V for CNT length ~20nm, diameter 3-5nm); b) high current-carrying capacity; and c) low energy (34eV) and time (<1ns) for transition. We have used the widely-accepted interconnect model [10] for carbon nanotubes to derive the

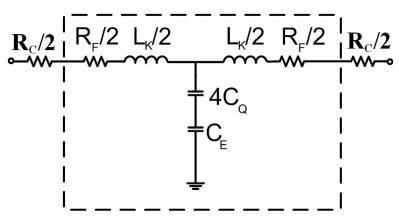

Fig. 4: Equivalent circuit model for CNEMS.

circuit-compatible model for CNEMS in our simulations. Fig. 4 shows the equivalent circuit model.

2.3 Hybridization of CMOS with CNEMS

The hybrid implementation can be achieved by extending the existing CMOS fabrication process. A possible integration solution, shown in Fig. 5, consists of separate layers for MOSFET and CNEMS, while an interconnect layer in between makes the required connections between CNEMS and MOSFET devices. Typically, CNTs require higher growth temperature compared to CMOS, which may cause adverse impact on transistors on silicon substrate when CNTs are grown after MOSFET fabrication. However, in recent past, CMOS-compatible growth technique of CNTs has been widely investigated and solutions have been proposed [11], which appear promising to make the proposed hybridization feasible.

3 APPLICATION OF CNEMS FOR LEAKAGE REDUCTION IN SRAM

The scheme for reducing standby leakage in memory with CNEMS switches is shown in Fig. 6. Unlike conventional source biasing scheme for leakage reduction in standby mode using sleep transistor, we exploit the unique structure of the CNEMS to connect the virtual ground terminal (VSSV) to the actual ground (VSS) in active mode (Fig. 6a) and to a bias voltage (VSB) in the standby mode (Fig. 6b). In the active mode, the low resistance of the CNEMS switch (or an array of them in parallel) and their high current carrying capacity allows normal operation with minimal penalty in Read/Write delay. In the sleep mode, the CNEMS switch terminal "B" at the virtual ground (VSSV) is connected to the terminal

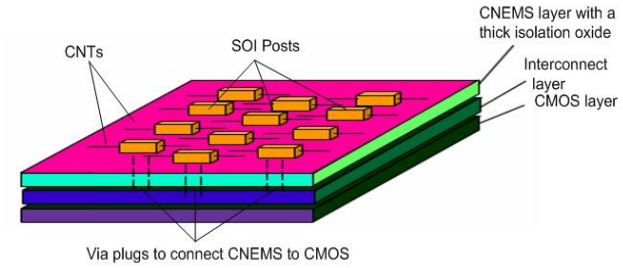

Fig. 5: A possible way to hybridize CNEMS Structure with CMOS.

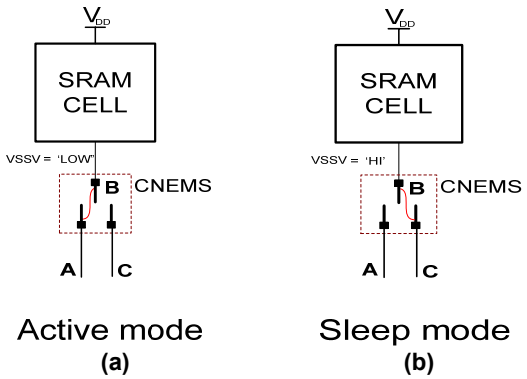

Fig. 6: The proposed leakage reduction scheme using CNEMS switches for source biasing: a) active mode; b) standby mode.

"C" which is at a positive potential. This voltage is chosen so that the sleep mode leakage is reduced; however, it is above the "Data Retention Voltage" (DRV) of the SRAM cell thereby ensuring that data is retained.

The bitline leakage reduction scheme using CNEMS is shown in Fig. 7. We propose to reduce the bitline leakage by "re-routing" it during active mode. When a bitline is charged high and connected to a SRAM cell storing zero, there is a leakage current through the access transistor from the bitline to the node storing zero. The worst-case bitline leakage occurs when only one cell stores '1' and all the other cells in the column store '0'. When the read operation of the cells storing '1' starts, the sense amplifier may perform a faulty read operation due to the large leakage current from BL. This is prevented by the scheme shown in Fig. 7. Here, in addition to the BL and BL′ lines, we incorporate a leakage re-routing path for each block of

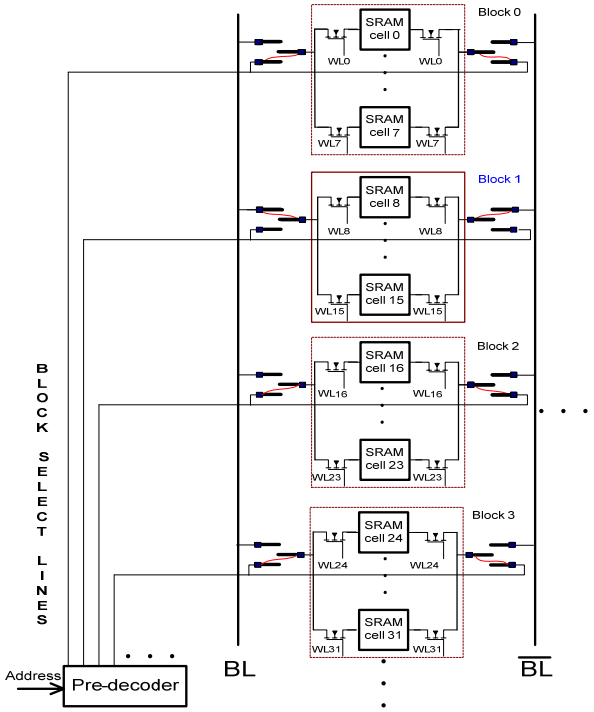

Fig. 7: Proposed scheme for bitline leakage reduction in an SRAM array.

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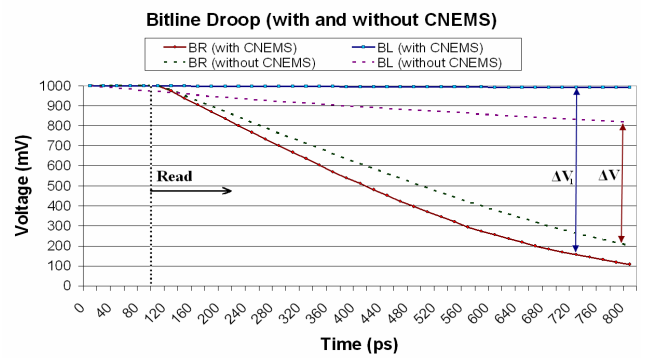

Fig. 8: Reduction in read noise margin due to bitline leakage (VDD=1V, T= 300°K, 256 rows).

SRAM cells using CNEMS. When a wordline is asserted for read operation, the access transistors of all the cells belonging to the block are connected to the BL and BL′ lines. The remaining blocks which are not being accessed are connected via CNEMS to the re-routing path, which prevents them from affecting the bitline charge. A pre-decoder (similar to [3]) controls the switching of CNEMS during read access. Since the leakage of non-accessed rows cannot affect the bitlines, the voltage droop due to bitline leakage in the BL (or BL′) effectively reduces to nearly zero, improving the read noise margins.

4 RESULTS

Table 1 contains the simulation results showing the reduction in standby leakage current for an SRAM cell for BPTM 45nm and BPTM 70nm models, compared to the source biasing scheme. We observe an improvement of ~19X for the 70nm process and an improvement of ~11X for the 45nm process. Table 2 shows the improvement in bitline noise margins due to the proposed scheme. The simulated BL and BL′ waveforms have been shown in Fig. 8 for the BPTM 45nm process. It can be observed that the leakage in the bitline reading a '1' causes a voltage droop of almost 200mV in just 800ps, reducing the read noise margin considerably. On the other hand, the proposed bitline leakage reduction scheme using CNEMS considerably mitigates this problem.

5 CONCLUSIONS

We have presented a unique hybridization of a new carbon nanotube NEMS structure called CNEMS with CMOS technology to decrease the leakage power in SRAM. We show that for memory circuits, the cell leakage can be reduced and undesired bitline droop due to bitline leakage can be mitigated by redirecting the bitline leakage using CNEMS. Based on our investigation, we can conclude that CNT-NEMS with special characteristics can be extremely effective for low-power and robust SRAM design using nanometer CMOS technologies.

Table 1. Comparison of leakage reduction with source biasing scheme in standby mode

Cell leakage power			Improvement over source biasing scheme
Tech	Source biasing	Proposed scheme	
45nm	68.9 nW	6.37 nW	**10.82X**
70nm	41.66 nW	2.25 nW	**18.52X**

Table 2. Improvement in read noise margin

Voltage droop (due to bitline leakage) (values after 800ps, V_{DD}=1V,T= 300°K)								
Tech	Original SRAM				Proposed scheme			
	BL (mV)	BR (mV)	ΔV (mV)	I_{BL} (μA)	BL (mV)	BR (mV)	ΔV (mV)	I_{BL} (μA)
45nm	818.1	199.9	618.2	49.9	991.3	108.6	882.7	0.9
70nm	902.7	215.4	687.3	29.4	993.2	188.4	804.8	0.5

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