HVMOS and LDMOS Modeling Review

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ABSTRACT

Different modeling approaches are reviewed including macro models and compact models. Advantages and disadvantages of them are discussed. HVMOS model in early stage is descripbed using Cadence HVMOS model as example. Compact modeling techniques used in advanced LDMOS model are discussed to cover different features of LDMOS devices.

1 INTRODUCTION

Due to its feasibility of integration to standard CMOS/BiCMOS technoloty, LDMOS (Lateral Double Diffused MOS) devices are widely used for different high voltage applications such as switch-mode power supplies and power amplifiers [1~3]. Optimal design of power circuits based on LDMOS requires accurate high-voltage LDMOS models for circuit simulation which describe the device characteristics including both DC, AC and RF behaviors over a wide range of transistor geometries, operating voltages and operating frequencies.

There are different approaches for LDMOS modeling. Until recently, it has been a common practice to use sub-circuit model called macro model in high-voltage circuit simulation due to the lack of accurate and physical compact LDMOS model available in commercial circuit simulation tools [4-6]. Different macro models used in HVMOS/LDMOS modeling are either using bias dependent resistance (in VerilogA format, or in voltage controlled resistance) or using JFET to model drift region resistance. Macro models have the advantages of simulator independency and flexibility to fit different device structures. However, it often suffers from accuracy, performance and convergence issues.

While macro models can usually fit I-V data well [7], it often has difficulty in fitting C-V data. However, the capacitance model accuracy, especially for Cgd, is critical for predicting dynamic behaviors of LDMOS circuits in switching transition. This is even more important for RF applications in which accurate capacitance modeling is even critical for circuit simulation. The Cgd modeling in LDMOS is complicated due to the unique process flow and device structure of the LDMOS devices. Specifically, the existence of large gate-to-drain overlap region contributes a big part to Cgd, and the lateral non-uniform doping of channel also plays an important role in the Cgd characteristics. All those limitations require compact HVMOS/LDMOS models to capture all the major effects including both DC and AC for circuit simulation with good accuracy and robustness. Compared with macro model approach, compact model has obvious advantages. It can accurately model DC, AC and high frequency behavior of the high voltage devices. It can easily model self-heating effect. And compact model approach usually has better performance and convergence behavior. Early stage of compact model development for HVMOS devices, represented by Cadence HVMOS model, was empirical. The quasi-saturation behavior in HVMOS devices is modeled by changing saturation velocity formulation to include gate bias dependency. Newly developed physics-based LDMOS models usually use bias dependent drift region resistance to model the quasi-saturation behavior. Several unique features of LDMOS/HVMOS devices and their modeling approaches are discussed. Those includes quasi-saturation, bias dependency of drift region resistance, non-uniform doping in channel region, substrate current, self-heating effect, distributed RC network effect on charge model.

In this paper, different macro modeling approaches are presented. Historical and current status of HVMOS/LDMOS compact models is reviewed and various modeling techniques are discussed.

2 LDMOS STRUCTURE ANDMODELING CONCERNS

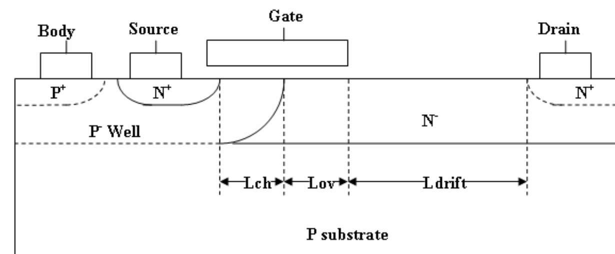

Figure 1: Typical LDMOS structure.

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

Figure 1 shows the typical N-channel LDMOS structure used in this study. Compared with conventional MOSFET devices, the LDMOS has the following unique features:

- The channel length Lch of the LDMOS device is defined by the P-Well and N-Well formation, i.e. the P-Well underneath the gate.
- The doping in the channel region is highly laterally non-uniform as a result of the existence of P-Well and N-Well regions.
- There is a significant gate-to-drain overlap region Lov between the gate and the drain because of the overlaping between the gate and the N-Well region.
- The LDMOS device is non-symmetric between the source and drain due to the introduction of drift region Ldrift and the gate-to-drain overlap region Lov on the drain side only.
- Vth of the LDMOS device mainly depends on the doping level of the channel region Lch, while the drain current is significantly modulated by the overlap region Lov and the drift region Ldrift on the drain side.
- The unique LDMOS structure yields different device scaling effects as compared to that in standard CMOS devices

Due to its special device structure and high voltage application, special considerations are needed for LDMOS modeling including the following items:

- Self-heating effects
- Bias dependent drift region resistance modeling
- Overlap region resistance modeling
- Substrate current modeling with double-peak Isub
- Multiple junction effect
- Breakdown behavior
- Physical charge model including lateral non-uniform channel doping and overlap region capacitance
- Gate/substrate resistance network for RF modeling
- Model scalability for both temperatuer and geometry

3 MACRO MODEL APPROACH

Macro model approach uses an intrinsic MOSFET model as the core of the LDMOS device (usually bsim3 model). And use either a bias depedent resistance, or using a jfet device to model the bias dependent drift region resistance.

Figure 2 shows a typical macro model using bias depedent resistor to model the bias dependency of the drift region resistance [8]. In this model, two intrinsic transistors are connected in serial, with different threshold voltage. In this way, the lateral non-uniform channel doping effect on charge can be modeled well. The drift region resistor can be either modeled as a parameterized resistance in a subcircuit, or using VerilogA code to describe the bias depedent of the resistance with respect to Vds and Vgs, as well as Vbs in some cases.

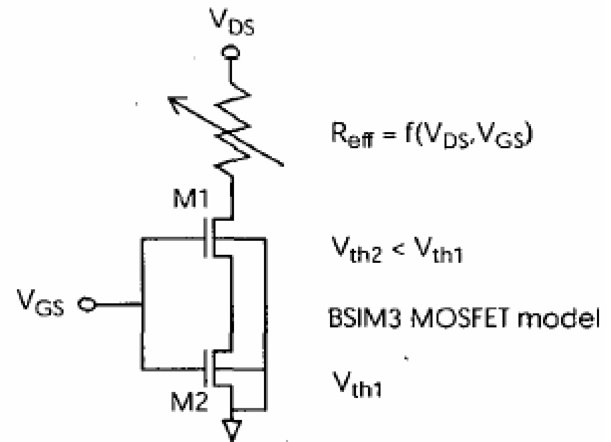

Figure 2: Macro model of LDMOS using bias depedent resistance.

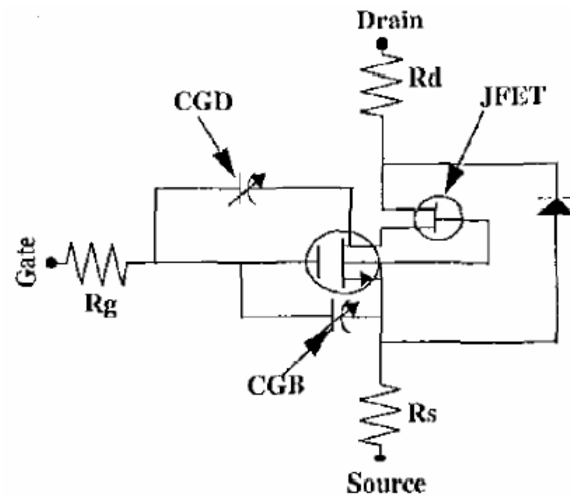

Figure 3: Macro model of LDMOS using JFET

Figure 3 shows another commonly used macro model for LDMOS model. The drift region resistance is modeled as a JFET. The gate of the JFET is connected to the body of the intrinsic MOSFET. Junction of the JFET is actually the junction between body and drain, and it's depeletion width is modulated by drain/body bias as shown in the model. In this way, the drain/body bias modulated conduction width in drain extended region is modeled physically. It is worth to mention that in this model, a bias dependent capacitance is added between gate and drain. This is used to model the gate/drain overlap region capacitance, and can be applied to any macro models.

4 EARLY STAGE OF HVMOS MODELS

Early stages of HVMOS devices are using extended drain region to sustain high voltage as shown in figure 4. Compared with LDMOS devices, the channel doping of HVMOS is uniform in lateral, and usually there is no significant overlap region between gate and drain. However, they are the same that both have a significant length of lightly doped drain region. From device behavior, both of them have quasi-saturation effects due to the large drain resistance from the extended drain region in HVMOS, or the drift region in LDMOS.

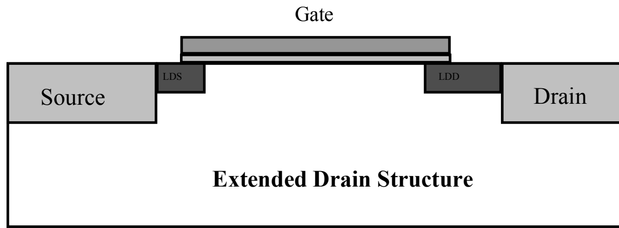

Figure 4: Extended Drain Stucture for HVMOS

Early stage of HVMOS model is represented by Cadence HVMOS model. This model was developed about 10 years ago by BTA modeling group (acquired by Cadence) and was widely used by foundries and IDMs for HVMOS device modeling. In this model, the quasi-saturation effect of Id-Vd behavior is handled by gate bias dependent velocity saturation model. Here are the unique features of Cadence HVMOS model:

- Vsat reduction at high Vgs to model Gm reduction
- Asymmetric and bias dependent S/D resistance
- Mobility reduction due to parasitic resistance
- SCBE gate-voltage dependence
- Channel length dependence of Vbseff
- Self-heating effect
- Forward and reverse operating modes

5 ADVANCED LDMOS MODELS

LDMOS devices are more and more widely used in high voltage application due to its superior performance than concentional HVMOS devices. To address the limitation of macro model approach, various compact LDMOS models are developped. [9,10]. Different LDMOS model might use different model techniques to handle the special LDMOS device behavior. Here in this section, some major effects and their model approaches are discussed in details.

5.1 Bias Dependent Drift Region Resistance

Compared with conventional MOSFET, LDMOS shows significant quasi-saturation effect for the drain currents at high Vgs biases. This is believed to be caused by the bias-dependent drift region resistance. Drift region resistance also has important effects on LDMOS capacitance model [11]. So accurate modeling of drift region resistance is critical in LDMOS model development.

Drift region resistance depends on the width of the conduction region so it is highly modulated with drain substrate biases. In high Ids region, carrier drift velocity can saturate. From the velocity saturation, one can derive current equation through the drift region:

$$I_{drift} = \mu_{eff} \times q_{sheet} \times \frac{V_{drift}}{L_{drift}} \times W_{drift} = \frac{\mu_0}{1 + \frac{V_{drift}}{L_{drift} \times E_{sat}}} \times q_{sheet} \times \frac{V_{drift}}{L_{drift}} \times W_{drift} \tag{1}$$

Then the drift region resistance is given by.

$$R_{drift} = \frac{V_{drift}}{I_{drift}} = \frac{L_{drift}}{W_{drift}} \times \frac{1 + \frac{V_{drift}}{L_{drift} \times E_{sat}}}{q_{sheep} \times \mu_0} = \frac{L_{drift}}{W_{drift}} \times \rho_{sh} \times \left(1 + \frac{V_{drift}}{L_{drift} \times E_{sat}}\right) \tag{2}$$

5.2 Self-heating effects

Self-heating effect is significant in LDMOS and it is modeled by proposed thermal network shown in figure 5. IdVd is the power of the device, Rth is thermal resistance and Cth is the thermal capacitance. Thermal node voltage is calculated during simulation, which is the device temperature used in model evaluation.

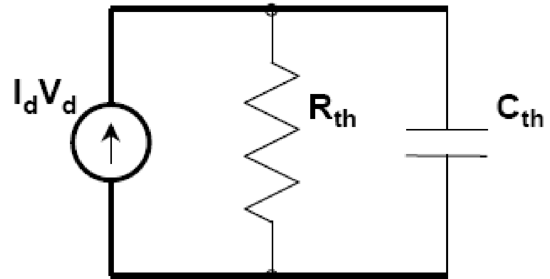

Figure 5: Thermal network used in self-heating modeling

5.3 Impact ionization currents

Due to complicated drain structure and electric field distribution along the drain region at different gate biases, there could be two peaks in measured substrate current. Then two substrate current components are necessary for modeling Isub behavior. The first one accounts for impact ionization current in intrinsic MOSFET near drain region, which happends at lower Vgs bias region. The second one account for the impact ionization current happening at higher Vgs bias region in drift region.

5.4 Non-uniform Channel Doping Effects

Due to the fact that the channel of LDMOS is formed by lateral diffuction of P-Well (for N-type LDMOS), channel

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

doping is highly non-uniform in both lateral and vertical direction. This causes complicated capacitance behavior of the channel region. At Vds=0, When Vgs increases from sub-threshold region to above threhold region, drain end of the channel will be inverted before source channel part, due to the fact that drain side doping level is lower than source side. This part of channel charge contributes completely to Cgd. As Vgs increases further, source end of the channel is inverted as well. Then channel charge will be partitioned to both source side and drain side. The change of partition of channel charge to drain side or source side has effect on Cgd and Cgs behavior during the transition. Specifically, this two stages inversion results in the increase of Cgd at early stage, and then drop of Cgd as well as increase of Cgs in second stage. So, properly modeling of the lateral non-uniform doping effect is important in accurate predicting Cgd/Cgs behavior.

One approach to handle this is using different effective Vth for drain side channel and source side channel in charge model [11]. Approach in [12] directly include the effect of channel doping profile on charge model and partition scheme.

5.5 Overlap Capacitance Modeling

As shown in Figure 1, there is a significant gate-to-drain overlap region near the drift region at the drain side. This reduces the electric field near the boundary of the drain and the channel at high Vds biases. This can also reduce the resistance of overlap region when the device is turned on. Physically, the LDMOS near the drain side is more like a depletion-mode N-channel MOSFET which is always in series with another enhancement-mode N-channel MOSFET in the channel region.

Comprehensive modeling of the overlap region capacitance include a p-type mos capacitance which can be in accumulation mode, depeletion mode and even inversion mode. In different modes, the charges are associated to different node [11]. In [12], a depletion mode transistor is used to model the overlap region capacitance.

5.6 Model Scalability

A good model should be able to fit into data for devices with various LDMOS structures and sizes. This requires a good scalability of the model. Channel length scalability is not so critical in LDMOS since the channel region is formed by lateral diffusion and its channel length is more or less the same for all devices in the same process. The scalability of the drift region length and device width is much more important in LDMOS for both DC and AC models. The proposed model in this work fully addresses the model scalability issues in terms of the drift region length and width, the overlap region length and width, the channel length and width, and the device geometries.

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6 SUMMARY

In this paper, different modeling approaches are reviewed including macro models and compact models. Advantages and disadvantages of them are discussed. HVMOS model in early stage is descripbed using Cadence HVMOS model as example. Compact modeling techniques used in advanced LDMOS model are discussed to cover different features of LDMOS devices.

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