Concurrent Process, Device and Integrated Circuit Development by Predictive Engineering for Smart Power Technologies

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ABSTRACT

Predictive TCAD has been shown to be a powerful tool for the development of low voltage CMOS and VLSI memory technology development [1], [2] in which the main features of advanced p-channel and n-channel MOS transistors could be accurately predicted. This paper presents the successful application of predictive engineering to the concurrent process, device and circuit development of a family of submicron smart power technologies. The implemented TCAD environment uses a combination of commercially available tools, proprietary software, improved process models and systematic, computer-aided calibration procedures. The importance of a systematic calibration of the TCAD tools is particularly emphasized and illustrated through the accuracy improvements made over the three versions of the technology. The generation of the technology data base from simulated results allowed early circuit design then shortening the cycle time by 8-12 months.

Keywords : predictive engineering, TCAD, calibration, smart power technology

INTRODUCTION

The success of predictive simulations critically depends upon the quality of the models coded in the TCAD tools and their calibration to silicon data. It is commonly accepted that, to extend the calibration space, TCAD tools should rely increasingly on physical models. A model based on fitting experimental curves (e.g. with polynomials) will quickly misbehave outside its fitting domain, making extrapolations extremely risky. As opposed to that, physical models, while often more cumbersome, are expected to capture the essence of the phenomena, therefore allowing better extrapolations.

There is a strong economical incentive for extrapolative, quantitatively accurate TCAD capabilities, even if only possible under restrictions. A semiconductor company will only start recovering investments in new technologies when circuits and systems built using those technologies are qualified and marketed. Performing circuit and system development concurrently with the experimental process development would considerably shorten the time to the onset of a revenue stream. Quantitatively accurate TCAD tools are the key to the success of such an approach. To progress towards a better calibration and to improve the predictive capabilities of the simulation techniques, the TCAD tools must fulfill two requirements:

- provide accurate descriptions of all the devices in the technology (i.e., within specified, acceptable tolerances)
- generate output results compatible with the IC design tools.

In this work, we achieved both goals as required for the concurrent development of a family of three smart power technologies.

SMOS5 TECHNOLOGIES

SMOS5 is a family of sub-micron smart power technologies, including three 0.65 µm (0.8µm minimum feature) Bipolar/CMOS/DMOS versions. This fifth generation of smart power technologies, targeted a wider range of applications than its predecessors. Three market have been identified, with enough variability to justify a customization of the technology requirements, however with enough commonality to consider them members of the same family.

The three versions of SMOS5 family and their main areas of application are :

- SMOS5CB, a low voltage (8-10V) BiCMOS technology for consumer applications.
- SMOS5AP, a high voltage (13-65V), high current Bipolar/CMOS/DMOS technology for automotive applications.
- SMOS5LP, a lower voltage (2.7-18V), low power Bipolar/CMOS/DMOS technology for battery operated and desktop applications.

SMOS5LP is the most complex of the three versions in the family, integrating power devices, 11 distinct MOS and bipolar transistors, 5 resistors and 8 capacitors. Table 1 summarizes all the device set of each version for which SPICE parameters have been generated from TCAD simulations.

SMOS5CB	SMOS5AP	SMOS5LP	SMOS5CB	SMOS5AP	SMOS5LP
POWER DEVICES			BIPOLARS		
	13V LDMOS	FD 18V LDMOS	NPN	NPNHH	NPNHH
	25V LDMOS		VPNP *	NPNL	NPNL
	35V LDMOS		LPNP *	VPNP	VPNP
	45V LDMOS			LPNP	LPNP
	65V LDMOS			PNPS	PNPS
	65V Line TMOS		MOSFET		
	65V Cell TMOS		LVNMOS	LVNMOS	LVNMOS
CAPACITANCES			LVPMOS	LVPMOS	LVPMOS
Cnsd-pw	Cnsd-pw	Cnsd-pw		MVNMOS	MVNMOS
Cpsd-nepi	Cpsd-nepi	Cpsd-nepi		MVPMOS	MVPMOS
Cnsd-pbase	Cnsd-phv	Cnsd-phv		HVPMOS	HVPMOS
Cpbase-nepi	Cphv-nepi	Cphv-nepi			MVDNMOS
Cpsd-nbase *	Cpsd-nhv	Cpsd-nbase	RESISTORS		
Cnbase-pw *	Cnhv-pw	Cnbase-pw	Rnsd	Rnsd	Rnsd
Cnepi-psub	Cnepi-psub	Cnepi-psub	Rpsd	Rpsd	Rpsd
	Cpw-nepi	Cpw-nepi	Rnbase *	Rnhv	Rnbase
			Rpbase	Rphv	Rphv
				Rpw	Rpw

Table 1 : List of all the devices simulated for the generation of SPICE models for the 3 versions of SMOS5 technologies. * indicates that these data could not be provided by the simulation.

The technology specification for the SMOS5 family imposed additional restrictions, to ensure the commercial viability of the family by emphasizing the commonalities of the three versions. The family members have been required to share:

- a common wafer fab capacity
- at least 80% of the processing steps
- the same CAD system for IC design, requiring common SPICE models, CMOS digital libraries, design rules, verification tools etc.

It is now evident that, as opposed to pure CMOS processes, the SmartMOS technology must provide a large variety of device types, requiring a much more extensive and accurate calibration of the process simulation tools. Since the process versions belonging to the SMOS5 family have been developed serially, it was possible to identify, in each generation, limitations and errors in the TCAD tools, then improve models and perform systematic calibration to determine optimum parameter values, thereby considerably expanding the calibration space for the following generation. At the end of the sequence, all the numerous devices provided in by SMOS5LP could be simulated with a unique set of impurity profiles. Except for features for which no models exist (e.g. flicker noise), the TCAD accuracy allowed to perform virtual SPICE parameter extraction and generate job decks for physical IC design at the transistor level. Furthermore, all library views required for automated digital IC design could be produced and the IC design could be started before manufacturing any functional silicon.

To accelerate the development of the SMOS5 family members, a predictive engineering environment has been implemented and extensively used.

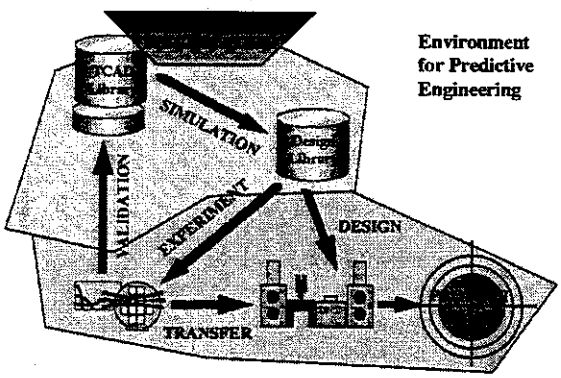


Fig.1 Environment for Predictive Engineering improved with each cycle of learning.

CONCEPT OF PREDICTIVE ENGINEERING

A considerable amount of simulation software is required to perform the tasks specified above. Our strategy consisted in using commercially available tools whenever possible (TSUPREM-4 and MEDICI for process and device simulation, respectively), and expanding their capabilities when necessary by systematic calibration, advanced physics-based models and internally developed software.

Ideally, all devices should be simulated using impurity profiles obtained from process simulation and device geometries obtained from GDSII layouts based on the

design rules. Simulated device characteristics can then be used to extract SPICE parameters. Large power devices require additional layout modeling to determine their characteristics and model parameters. At this point, all information is available to produce technology specific files for the IC CAD system. IC design can be started based on simulated characteristics and parameter extraction concurrently with the experimental process development. In our case, this approach shortened the time to market by 8-12 months.

The main steps of the predictive engineering methodology used for the current work are illustrated in Fig.1:

1) Extract from the TCAD Library of previously calibrated process flows the technology nearest to the current work.

2) Implement the process flow according to the Technology specification.

3) Perform process and device simulations, generate sets of device characteristics and extract SPICE parameters.

4) Concurrently perform experimental process development while starting circuit design using simulation based SPICE parameters.

5) Validate simulation results against silicon measurements.

6) If predicted parameters are within tolerance, proceed with step 7; If not, perform extensive systematic calibration including new model developments.

7) Place calibrated flow in the TCAD Library for future iterations.

SYSTEMATIC TCAD TOOL CALIBRATION

Commercial TCAD software is often inaccurate when used with default parameters and/or settings. To improve the TCAD predictive capabilities, advanced proprietary models have been generated using a systematic calibration methodology [3].

It is difficult to accurately simulate shallow junctions due to the necessity of calibrating transient enhanced diffusion (TED) models. The accuracy of their profiles is strongly required to do predictive simulation of devices such as narrow base bipolar or submicron MOS transistors. A calibration software named CALYPSO (CALibrating Yoke for Process Simulators with Optimization) was developed for systematic optimization of process model parameters.

Most of the defect-based diffusion model parameters [4] in FLOOPS [5] process simulator were transferred and reused in TSUPREM-4 [6]. Three of the most unestablished parameters were calibrated to match more than 25 SIMS and SRP profiles that were obtained from process integration of a MOSFET technology by using CALYPSO. The main regime of interest was TED of boron and phosphorus under low-dose implant conditions. One of the results is shown in Fig. 2. Boron was implanted at a low dose, followed by multiple thermal cycles ranging from 800°C to 1025°C including RTP. The source/drain regions were implanted with arsenic to a high dose. The calibration led to a significant improvement in the accuracy of the simulation of the dopant redistribution after a low-dose implantation.

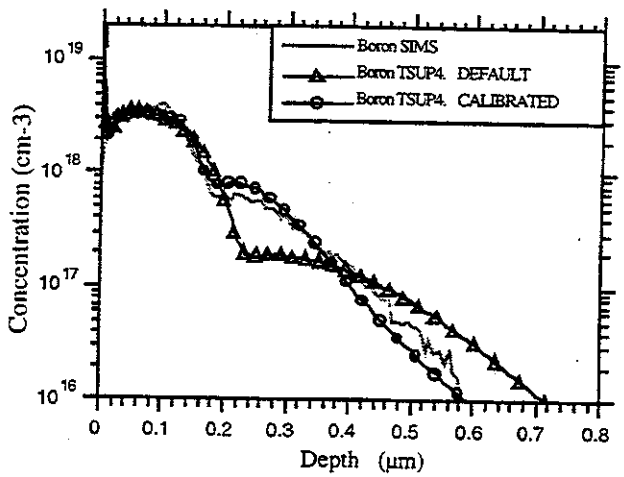
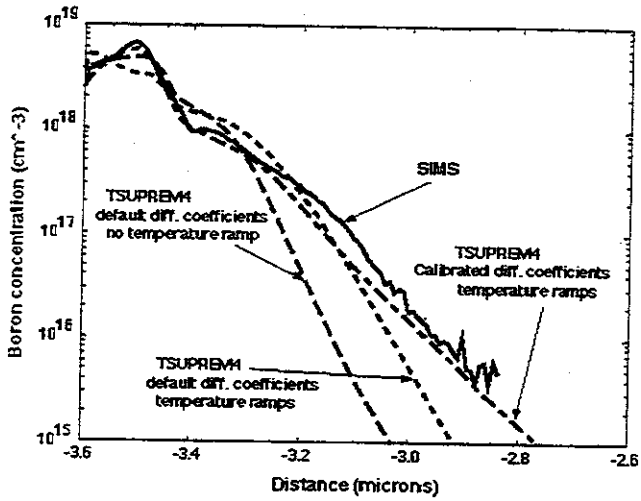


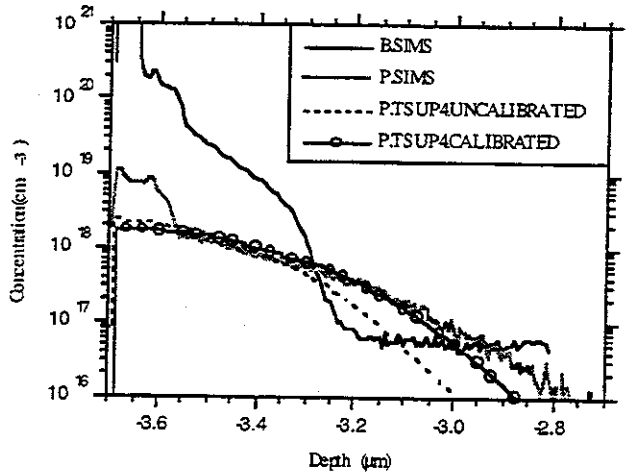
Fig. 2. An example of calibration for TSUPREM-4 simulation of diffusion of boron in a MOSFET device.

The same set of calibratedparameters was applied to the simulation of the bipolar devicesof the SMOS5CB process flow which is totally independent of the calibration database. Bipolar devices are the more critical in terms of both dimensions (submicron base) and doping. Fig. 3 (a) and (b) show a consistent match between the predictive simulation and SIMS data for the npn and pnp bipolar transistors of the technology. The reasonably good match with SIMS data obtained with the calibrated process flow demonstrates the improvement in the predictive capability of the TED simulation system.

To complete the calibration process, device simulation results of the reference device were compared to electrical measurements. For a good matching, some fine tuning of parameters was necessary, in particular, the mobility models and the carrier lifetime. Regarding the NPN, the process simulation calibration greatly improved the matching of the dopant, but the differencein the electrical characteristics was not very significant. In other words, a good fit of the npn electrical characteristics would have allowed for a considerablevariability in impurity profiles. In contrast, for the PNP, the simulation with uncalibrated diffusion coefficients resulted in a non-functional transistor whereas with the calibrated one a reasonable matching was obtained (Fig. 4). The discrepancyat high currents is due to the fact that this simulation consideredonly the intrinsic transistor, whereby in the measureddata the parasitics (e.g. series base resistance) force the characteristics to deviate at high currents from their intrinsic shape.



(a)



(b)

Fig.3 : Predicted base doping profiles compared to experiment for NPN (a) and PNP (b) : Impact of advanced physical models.

When completed, our calibration allowed the simulation of all the different active and passive devices of the technology starting from a common, coherent process flow simulation. In particular, we normally started the calibration process by fitting the npn and pnp devices, but we automatically obtained good fits for the MOS transistors, demonstrating a clear improvement in the predictive capabilities of the environment.

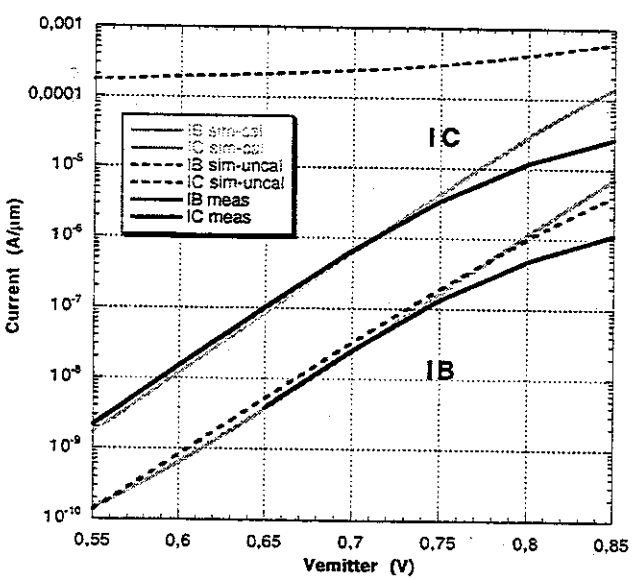


Fig.4 : Predicted Gummel characteristics for VPNP: impact of advanced physical models.

Fig. 5 shows the comparison of simulated and measured Id(Vg) characteristics of the NMOS transistor. A very good agreement is obtained for the threshold voltage and the transconductance for low voltage drain, a discrepancy of 9.7% being observed at a gate voltage of 4V. Comparisons against measurements at different substrate biases as well as measured subthreshold currents further confirmed that the accuracy of the predicted characteristics.

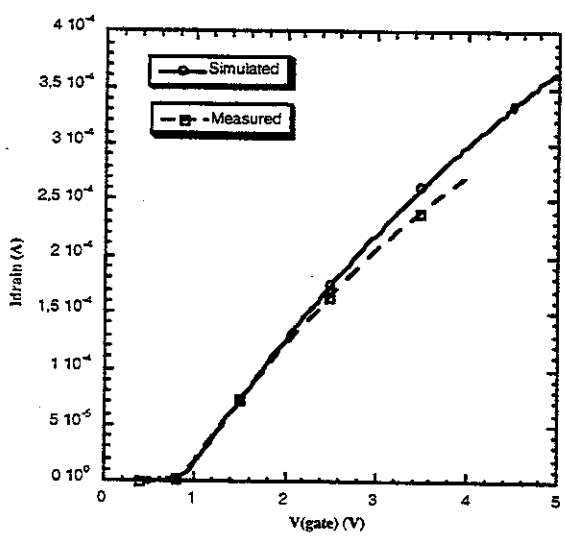


Fig. 5 : Comparison of MEDICI simulated and measured Id(Vg) characteristics of the NMOS transistor of SMOS5CB.

The first version of the SMOS5 technologies allowed the set-up of the methodology. The calibration work of the vertical pnp described in Fig. 3 could not be completed in time to be effective in the development of SMOS5CB. Other methods had to be used for the SPICE model generation of the vertical pnp transistor, as discussed in the next section. For the subsequent versions, available silicon data were used to improve the calibration of both the process and device simulation. As a result, starting with

SMOS5AP, all active and passive devices could be simulated with the same set of impurity profiles.

SPICE PARAMETER EXTRACTION

Small signal devices

SPICE parameter extraction have been generated for the small signal devices using a combination of the following methods :

- direct extraction from the 2D-simulated device characteristics.
- educated guess and extrapolation from a previous model parameter set.
- estimations from analytical calculation.

Device	SMOS5CB Sim. VBE	SMOS5CB Meas. VBE	SMOS5AP Sim. VBE	SMOS5AP Meas. VBE
NPN	680 mV	667 mV	675 mV	688 mV
VPNP	Not functional	740 mV	745 mV	756 mV

Table 2 : Improvements in bipolar V_{BE} with cycles through Predictive Engineering System.

To allow the extraction of SPICE parameters from curve fitting, the simulation must produce the same number of characteristics as the real measurements used for this purpose. In line with current practices, for MOS devices we performed only DC simulations, whereby for the bipolar devices we performed both DC and AC simulations. For some characteristics, the simulations were performed over temperature. In order to keep under control the number of characteristics required, we took advantage of the scaleable models for bipolar devices available in our SPICE flavor, so that only the minimum geometry bipolar devices needed numerical simulations.

Even with this simplification, the simulation requirements once the calibration was satisfactory have been quite extensive. For instance, for SMOS5AP we performed 242 device simulation runs for 51 device structures corresponding to different device types and geometries. The voltage covered the range from 3V to 65V, depending of the particular device considered. The ideal predictive engineering process, i.e. running each required simulation no more than once, required 68 CPU days on a single HP9000K460-class workstation. The actual run time was considerably shortened by extensive job farming over a FDDI network.

This systematic approach quickly yielded decisive improvements in our predictive capabilities, making eventually possible to match all simulable device characteristics over the whole design space. Table 2 which compares the resulting, measured and simulated, V_{BE} voltage for a given collector current in the npn and pnp bipolar transistors of two successive technology versions, shows the accuracy improvement.

Power devices

Large area power devices required additional tools to evaluate the current distribution across their large layout, an aspect of the simulation that cannot be captured by 2-D numerical tools. Internally developed, proprietary software has been used in addition to the traditional TCAD tools, to provide support to the circuit designer [7]. A library including the size and shape of the complete device is mandatory for adequate modeling.

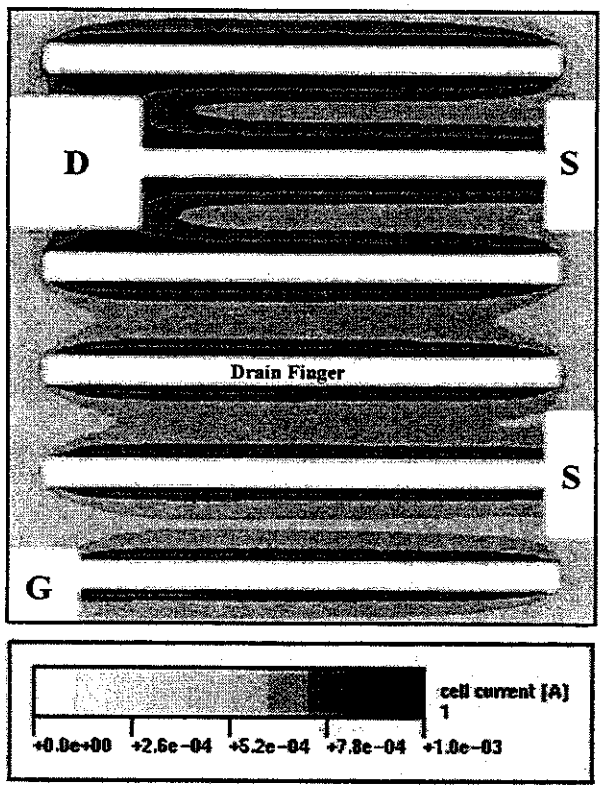


Fig. 6 : Simulation results for the vertical current through the cells of a DMOS power transistor.

The optimization of the vertical DMOS devices requires information about the single cell on-resistance, the sheet resistance of the buried-layer and of the metal layers as well as the layout of the metal interconnect of the complete device. MEDICI 2D-device simulation was used to provide sheet resistance information and the on-resistance for the optimized layout of one single DMOS cell with respect to the required breakdown voltage. The impact of the layout and of the interconnect was estimated either by SPICE-type simulations modeling the full 3-D resistor network of the complete power device or by an analytical approach on the basis of an improved SPICE-model of the power device including its resistive parasitics [8]. Fig. 6 shows the 2D-distribution of the vertical cell current in a device with 4 pads and 6 drain-fingers over the first level of metal. It can

be noticed that the highest values of the current are found close to the drain fingers. Device regions with low current density indicate strong debiasing effects induced by the interconnect resistance, mainly the buried layer. The top part of the device is most efficient, because the bond-wires and the current path to the drain pad made with the second level of metal are shorter.

These simulation efforts resulted in the specification of the optimum number of DMOS cells between drain fingers, the optimum length of the drain-fingers, and the appropriate location of the drain and source pads for wire bonding to the package. Today, the available simulation tools allow to compute the characteristics of the resulting device in the format of SPICE-type circuit simulators.[8].

CONCLUSION

It has been shown that it is possible to perform concurrent engineering in the development of submicron smart power technologies. The consequent use of TCAD software coupled with a systematic calibration methodology allowed to generate, on a solid simulation basis, enough information to be able to start circuit design prior to experimental process technology development.

The systematic calibration approach helped improve the quality of the prediction and the number of parameters simulated within tolerances with each consecutive generation. The computing resources required to generate all the data needed for the circuit design is considerable, however parallel computing techniques allow to greatly shorten the project duration. In our case, the evolutionary character of the development allowed us to compare the cycle time improvement obtained by using this concurrent approach. We determined that we have shortened the cycle time from the start of technology development to the first revenue by 8-12 months, providing a strong motivation for this approach.

The current state of the TCAD tools made it necessary to determine several device parameters, relevant for the circuit design, by methods other than TCAD simulations. However, the TCAD results have been able to provide a large majority of parameters with a satisfactory accuracy, providing a solid basis for SPICE parameter extraction.

It must be emphasized that the key for the accuracy is the systematic calibration of the models in the simulators as well as the development of advanced new models. The large amount of long-term efforts in the work presented here had a tremendous impact on the timeliness of the technology development. Nevertheless, much more investment is still required in various areas, particularly in the process modeling, to make further progress in improving the predictive capabilities and the accuracy of TCAD.

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