

Equation of p–n Junction for High Current Density Models of Transistor

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ABSTRACT

The results of theoretical and experimental investigations of p–n junction at junction voltages close to the potential barrier are presented. It is shown that in such a situation the voltage–current characteristic can be described by algebraic equation in explicit form and that exponential description of characteristic is in conflict with physics at junction voltages close to the potential barrier.

Possibility to create the transistor models for high current density and possibility to describe on basis of these models in many cases the static parameters of integrated circuits by mathematical expressions in explicit form is the advantage of suggested p–n junction equation.

Keywords: high current density, junction model, transistor model, accuracy.

1 INTRODUCTION

Model of p–n junction is the base for development of bipolar transistor model. The most part of bipolar transistor models for integrated circuits (IC's) analysis are based on description of p–n junction by Shockley equation (Shockley model) [1]

$$I = I_0 [\exp(U/mj_T) - 1], \quad (1)$$

where I is junction current, U is voltage applied to the junction, I_0 is saturation current of junction, j_T is thermal potential and m is empirical coefficient.

The equation (1) is valid for p–n junction voltage [2]

$$0 \leq U \leq \Psi - 2j_T, \quad (2)$$

where Ψ is potential barrier of p–n junction.

P–n junctions of present–day bipolar transistors work by relatively high forward current densities and U falls outside of values described by inequality (2). In such a situation, the Shockley model (1) and its parameters lose their physical meaning. By this is meant that the results of modelling of IC's on transistor models based on equation (1) in many cases can not be linked with IC's process technology parameters or with dimensions of transistors. Consequently, it's difficult if not impossible to apply these results for IC's parameters improvement.

2 EQUATION OF P–N JUNCTION FOR HIGH CURRENT DENSITY

We would like to present the results of theoretical and experimental investigations of p–n junction under condition of high current density. The theoretical investigation was performed for p–n junction voltage

$$\Psi - j_T \leq U < \Psi. \quad (3)$$

In the general case minor carrier densities in p–n junction can be described by following classical equations [1]:

$$n_p = \frac{N_p}{2sh \frac{\Psi - U}{j_T}} \left[\frac{N_n}{N_p} + \exp\left(-\frac{\Psi - U}{j_T}\right) \right], \quad (4)$$

$$p_n = \frac{N_n}{2sh \frac{\Psi - U}{j_T}} \left[\frac{N_p}{N_n} + \exp\left(-\frac{\Psi - U}{j_T}\right) \right], \quad (5)$$

where n_p and p_n are electron and hole densities, N_p and N_n are dopant densities on p–n boundary in p and n regions. On basis of equations (4) and (5) at the equilibrium state ($U=0$), taking in to account that $\exp(-\Psi/j_T) \ll \exp(\Psi/j_T)$, minor carrier densities

$$n_{p0} = N_n \exp(-\Psi/j_T), \quad (6)$$

$$p_{n0} = N_p \exp(-\Psi/j_T). \quad (7)$$

On basis of equations (6) and (7)

$$N_n = n_{p0} \exp(\Psi/j_T), \quad (8)$$

$$N_p = p_{n0} \exp(\Psi/j_T). \quad (9)$$

Using equations (8) and (9), on basis of equations (4) and (5), minor carrier densities in p–n junction are following:

$$n_p = \frac{n_{p0} \exp(\Psi/j_T) + p_{n0} \exp(U/j_T)}{2sh[(\Psi-U)/j_T]}, \quad (10)$$

$$p_n = \frac{p_{n0} \exp(\Psi/j_T) + n_{p0} \exp(U/j_T)}{2sh[(\Psi-U)/j_T]}. \quad (11)$$

Taking in to account inequality (3) we can make following approximations:

$$sh[(\Psi-U)/j_T] \approx (\Psi-U)/j_T, \quad (12)$$

$$\exp(U/j_T) = k \cdot \exp(\Psi/j_T), \quad (13)$$

where $0.37 \leq k < 1$.

On basis of equations (10) and (11) using approximations (12), (13)

$$n_p \approx (n_{p0} + kp_{n0}) \frac{j_T \exp(\Psi/j_T)}{2(\Psi-U)}, \quad (14)$$

$$p_n \approx (p_{n0} + kn_{p0}) \frac{j_T \exp(\Psi/j_T)}{2(\Psi-U)}. \quad (15)$$

The variation of coefficient k by changing the junction voltage within the limits (3) is moderate in comparison with variation of $j_T/(\Psi-U)$ member. In such a situation we can consider coefficient k in equations (14), (15) as constant with some average value.

We can see (14) that flow of electrons from n-region to p-region under high current density condition (3) depends on voltage by the law $j_T \exp(\Psi/j_T)/[2(\Psi-U)]$. Accordingly, the electron current increases in relation to the equilibrium state of current I_{0N} by the same law. The thermal electron current from p-region to n-region by high current density is infinitesimal in comparison with electron current from n-region to p-region and can be neglected. Consequently, the electron current can be described by equation

$$I_N = I_{0N} \frac{j_T \exp(\Psi/j_T)}{2(\Psi-U)}. \quad (16)$$

In a similar manner on basis of (15), hole current from p-region to n-region

$$I_p = I_{0p} \frac{j_T \exp(\Psi/j_T)}{2(\Psi-U)}. \quad (17)$$

Total current of p-n junction $I = I_N + I_p$. Consequently, on basis of (16) and (17) the equation of

junction under condition of high current density (3) can be presented following:

$$I = I_0 \frac{1}{2} \exp(\Psi/j_T) \frac{j_T}{\Psi-U}, \quad (18)$$

where $I_0 = I_{0n} + I_{0p}$ is the saturation current of junction.

It is well known from semiconductor physics [2] that the voltage on p-n junction can not exceed a value of junction potential barrier Ψ . By this is meant that in case when junction current tends to infinity ($I \rightarrow \infty$) the junction voltage approaches potential barrier value ($U \rightarrow \Psi$). Equation of p-n junction (18) takes in to consideration this point. The junction voltage by Shockley equation (1) $U \rightarrow \infty$ when $I \rightarrow \infty$. Consequently, model (1) is in conflict with physics of p-n junction under condition of high current density.

The equation (18) can be modified to extend its possibilities. It can be multiplied by U/U for this purpose

$$I = I_0 \frac{j_T \exp(\Psi/j_T)}{2U} \frac{U}{\Psi-U}. \quad (19)$$

Using designation

$$\frac{j_T \exp(\Psi/j_T)}{2U} = \mathbf{x}, \quad (20)$$

the equation (19) can be presented following:

$$I = I_0 \mathbf{x} \frac{U}{\Psi-U}. \quad (21)$$

The variation of coefficient \mathbf{x} by changing the junction voltage within limits (3) is moderate in comparison with variation of $U/(\Psi-U)$ member. In such a situation we can consider coefficient \mathbf{x} as constant

$$\mathbf{x} \approx \frac{j_T \exp(\Psi/j_T)}{2\Psi} \quad (22)$$

and on basis of (21) and (22) derive the following modification of junction equation (18):

$$I = I_0 \frac{j_T}{2\Psi} \exp(\Psi/j_T) \frac{U}{\Psi-U}. \quad (23)$$

Compared to junction equation (18), equation (23) is more suitable for creating of transistor models because it has reasonable accuracy in junction voltage range $0 \leq U < \Psi$. It is necessary to stress that equation (23) and

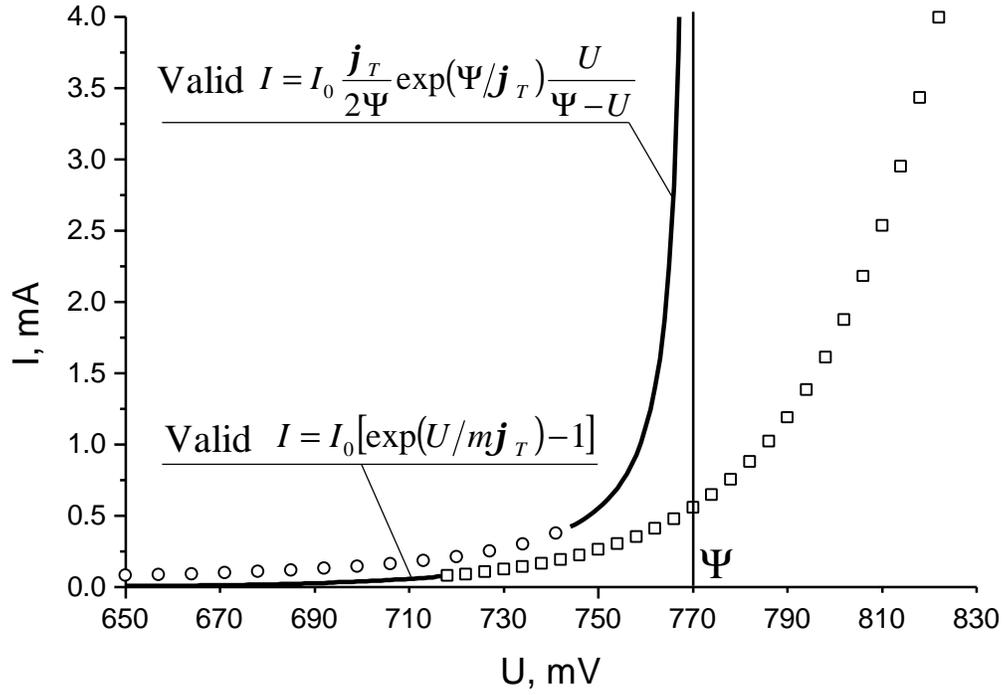


Figure 1: Voltage–current characteristic of emitter junction:
 □□□ ——— calculated on basis of equation (1);
 ○○○ ——— calculated on basis of equation (23).

its parameters lose their physical meaning and becomes as empirical model in junction voltage range $0 \leq U < \Psi - j_T$.

Possibility to create the transistor models for high current density and possibility to describe on basis of these models in many cases the static parameters of IC's by mathematical expressions in explicit form is the advantage of equation of p–n junction (23).

The equation of p–n junction (23) resembles the equation suggested by D. Zanevicius [3]. The qualitative differences between these two descriptions are that in equation (23) appear coefficient $x = j_T \exp(\Psi/j_T)/(2\Psi)$ and that equation (23) is derived on basis of p–n junction physics, while equation presented in [3] was derived empirical. The quantitative difference is that due to appearance of coefficient x accuracy of equation (23) is higher in comparison with accuracy of equation presented in [3].

The actual emitter junctions of IC's transistors have been investigated experimentally and current regions where equations (1) and (23) are valid have been obtained. The results show that many of investigated junctions work in regions where equation (23) is valid. For example, the results of investigation of emitter junction of comparator IC n–p–n transistor which works in region of emitter current $0 \div 4 \text{ mA}$ show that junction is characterised by parameters $I_0 = 1.2 \cdot 10^{-16} \text{ A}$, $m j_T = 26.4 \text{ mV}$ and $\Psi = 770 \text{ mV}$. Using inequalities (2) and (3) we can determine that

equations (1) and (23) are valid in emitter current regions $I = (0 \div 0.078) \text{ mA}$ and $I > 0.42 \text{ mA}$ accordingly (Figure 1).

3 THE ACCURACY OF EQUATION

The accuracy of p–n junction equation (23) taking in to account volume resistance of junction has been investigated. The experimental voltage–current characteristics of emitter junctions of various bipolar transistors that work in concrete IC's in operating ranges $0 \div I_{\max}$ of emitter current have been compared with characteristics calculated by equation (23). The distributions of maximum voltage error d_U and standard voltage error s_U for junction current regions $(0.05 \div 1)I_{\max}$ have been obtained and the maximum values of errors $d_{UM} = 3.0\%$ and $s_{UM} = 2.0\%$ have been estimated. The distributions of errors d_U and s_U of emitter junction of comparator IC n–p–n transistor are presented in Figure 2.

The comparison of maximum voltage errors with technological deviations of emitter junction voltage–current characteristics show that model errors at currents $(0.05 \div 1)I_{\max}$ are inside of deviations.

The transfer characteristics of difference amplifier (DA), digital–to–analog converter (DAC) and emitter–coupled logic gate (ECL) IC's have been simulated by bipolar transistor model based on junction equation (23)

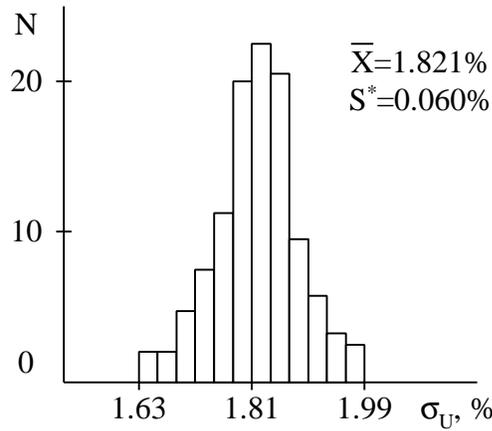
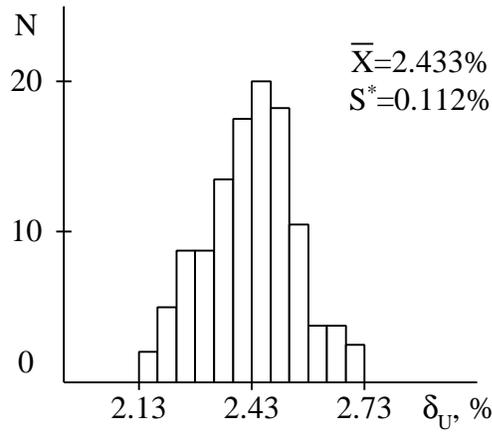


Figure 2: The distributions of errors δ_U and σ_U
 (\bar{X} – mean; S^* – standard deviation).

with account of transistor volumes resistances. In addition, the transfer characteristics using similar transistor model with the only difference that it was based on junction equation (1) have been simulated. The simulated transfer characteristics have been compared with experimental

characteristics and maximum errors have been estimated (Table 1). The simulation errors of transfer characteristics show that transistor models based on equation (23) can be used for quantitative calculations in region of junction voltage $0 \leq U < \Psi$.

Transistor model \ IC	DA	DAC	ECL
based on p–n junction equation (23)	0.6%	1.0%	2.5%
based on p–n junction equation (1)	1.0%	0.6%	3.0%

Table 1: The simulation errors of transfer characteristics of concrete IC's.

4 CONCLUSIONS

Equations of p–n junction (18) and (23) in contrast to Shockley equation (1) has a physical meaning at high current densities and gives a possibility to create in many cases the expressions of IC's static parameters in an explicit form.

The errors of difference amplifier, digital – to – analog converter and emitter – coupled logic gate transfer characteristics simulation by bipolar transistor model based on junction equation (23) with account of transistor volumes resistances varies from 0.6% to 3.0%.

REFERENCES

- [1] Muller R. S., Kamins T. I., Device Electronics for Integrated Circuits, N. Y., 353 – 360, 412 – 415, 1986.
- [2] Agahanian T. M., The principles of transistor electronics, Moscow, Energia, 25, 26, 1974.
- [3] D. Zanevicius, "Multilevel analysis of IC", Elektronnaja tehnika, ser.3, Mikroelektronika, No 3, 3–7, 1988.