

Self assembled monolayer(SAMs) and electroplating process for Cu filling on 32nm trench

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ABSTRACT

To improve the conformality of Cu seed layer prepared by ELD, we have also developed a novel activation technique by combining a self assembled monolayer (SAM) and Au catalyst. A coupling agent to anchor Au complex ions instead of metallic catalysts on the substrate was used, which enabled a defect free Cu filling of trenches by minimizing the electrical repulsion among the Au catalysts in the solution. The Cu seed layer formed by this method showed a highly conformal and continuous structure. Cu electrodeposition on the 32-nm trench was demonstrated using an acid cupric sulfate electrolyte containing chloride, polyethylene glycol 4000 and bis(3-sulfopropyl)disulfide. The resulting electroplated Cu showed excellent filling capability and no voids or other defects were observed in a 32-nm trench pattern. Therefore, this proposed method has the potential solution to replace the Cu seed layer formation method for future Cu metalizing technology for sub-32nm features. .

Keywords: Cu seed layer, self assembled monolayer, Au catalyst

INTRODUCTION

The microelectronics industry is undergoing rapid expansion and miniaturization, producing semiconductor devices which are increasingly smaller, faster and of higher density [1]. Increasing the degree of integration on semiconductor devices is governed by the material and practical limits of the device features. These limits include properties of the semiconducting and insulating materials, the layout of the device, and the circuit configuration [2]. In real manufacturing terms the most severe limitation for chip fabrication is not the transistor or other complex features, but the metal interconnects performing signal communication and power distribution [1]. These conducting networks are currently impeding the development of chips with shorter response delays. This issue is presently circumnavigated by keeping the interconnects short [2]. To roll back the frontiers of interconnect technology, considerable efforts are directed toward more conductive interconnects which are easier to manufacture. Ultra large-scale integration (ULSI) has led to metal interconnects on these devices being processed well below 0.25 μm [3]. The logic speed of a device is determined by its RC time constant, where R is the resistivity and L is the total length of the interconnects). To produce faster and

smaller devices it has become necessary to use a metal with lower resistivity [4-6]. Traditionally aluminum has been widely used in the fabrication of metal interconnects [4]. Metallization with aluminum typically is deposited by sputtering system. However, Al metallization becomes unreliable below 0.5 μm due to its high tendency of electromigration (EM) and stress induced migration (SM) which can lead to voiding. The next generation of faster integrated circuits (IC) will have higher device densities, faster operating frequencies, and larger die sizes, but it may be limited by metal interconnects [8]. There is an obvious need for new interconnect materials with lower resistivities, and that is true especially for longer global interconnects that run from one end of a chip to the other [2]. In recent years Cu has attracted increasing attention as a candidate to replace aluminum due to its low bulk resistivity, 1.7 $\mu\Omega/\text{cm}$ compared with 2.7 $\mu\Omega/\text{cm}$ for aluminum [9-11]. In fact, the only metal with a lower resistance is silver [4]. Cu is also less susceptible to EM, being 2 orders of magnitude more resistant than aluminum, possibly due to its higher melting point [12]. In addition, Cu has good thermal stability and a low-temperature coefficient of resistance [2]. There are however problems associated with using Cu; it diffuses substantially into Si/SiO₂ layers, which could cause electrical malfunctions also so far no easy dry etching process has been developed. Cu electrodeposition for on-chip metallization has been developed by Andricacos [19]. it is characterization of the proposed technique that under certain conditions, electrodeposition inside trenches occurs preferentially in the bottom, leading to void-free deposits, which phenomenon is called superfilling. To accomplish superfilling, the several additive such as chloride ion, inhibitor, such as poly(ethylene glycol) (PEG), accelerator such as bis(3-sulfopropyl) disulfide (SPS), and leveler such as Janus green B (JGB) are included in the bath [13,14]. The surfactant nature of the inhibitor can lead to rapid formation of a thin passivating PEG-based film on the metal electrode during its immersion through the air-electrolyte interface. Subsequently, the passivating layer is disrupted by the adsorption of the catalytic sulfonated-terminated short chain thiol/disulfide; the thiol/disulfide head group tethers the catalyst to the surface while the sulfonate terminal group interacts to prevent reformation of the PEG blocking layer [15, 16]. This displacement of adsorbed PEG by SPS impacts the metal deposition rate through a monotonic dependence on catalysts coverage. under certain conditions, this activation of the metal deposition rate is sustained by the tendency of the catalyst

to remain segregated at the growing interface [15-18]. Feature size effect will continue to increase the effective Cu resistivity. Electron scattering models have been improved and can now predict the Cu resistivity rise as a function of line width and aspect ratio. There is a significant contribution to the increase in resistivity from both grain boundary and interface electron scattering. To completely fill the Cu in trenches, it is necessary to deposit a high conductive seed layer. As feature sizes shrink, the PVD Cu seed layer must be made thinner to minimize overhang. This may result in discontinuous coverage, so that resulting in incomplete Cu gap fill. This problem is more severe at the wafer edge, where off-angle Cu deposition causes sidewall coverage asymmetry. At 2x, achieving high step coverage is extremely difficult because even a small overhang can almost completely occlude the trench from the target. Therefore, it is need that the modification of ion metal plasma (IMP) sputtering to control the Cu⁺ flux or the introduction of new deposition method with continuous and low cost.

EXPERIMENTAL PROCEDURE

A SAM was formed as part of the catalyst layer for the ELD of the Cu seed layer. The trench patterned wafer provided by Hynix Semiconductor Inc. was rinsed in de-ionized water (D.I.), followed by rinsing in a sulfuric peroxide mixture solution (SPM) at 60°C for one hour. After SPM cleaning, an organosilane SAM was formed on the substrate by immersion in a solution of 3-aminopropyltriethoxysilane (APTES) dissolved in ethanol at 60°C for three hours. Then, the SAM was activated in an AuNPs suspension for one hour. The ELD of the Cu seed layer on a patterned wafer was done at 60°C and at a pH 12.5. Cu was electrodeposited on the Cu seed layer for filling the trench pattern by using a copper-sulfate bath. The details of the composition and the condition of the plating bath are described in Ref. 5. Cathodic polarization measurements were performed with a three-electrode cell and rotating systems (Pine, AFMSRX rotator), which consisted of a saturated calomel electrode (SCE), a platinum sheet, and a Cu disk (10 mm in diameter) rotating at 200 rpm acting as a reference, a counter electrode, and a working electrode, respectively. The zeta potentials and the particle size distribution of the AuNPs were measured at room temperature with electrophoretic light scattering equipment (ELS-8000, OTUSKA). Surface and cross-sectional views of the Cu seed layer and Cu-filled trench pattern were observed using field emission scanning electron microscopy (FE-SEM, FEI, Nova NanoSEM630), transmission electron microscopy (TEM, JEOL, JEM2010), and atomic force microscopy (AFM, Digital Instruments, Nanoscope III). The surface composition of the SAM-modified substrate was measured by using X-ray photoelectron spectroscopy (XPS, VG, ESCALAB220i) with a Mg source.

RESULTS AND DISCUSSION

ELD is a heterogeneous catalytic electron-transfer reaction in which electrons are transferred from a reducing agent to metal ions at the solid-liquid interface. Therefore, a non-catalytic substrate such as SiO₂/Si has to be catalyzed to produce catalytic nuclei. For use as catalysts in Cu ELD, requirements such as a narrow particle size distribution and a small particle size within 5nm must be met because feature sizes have been approaching 100 nm for higher performance.

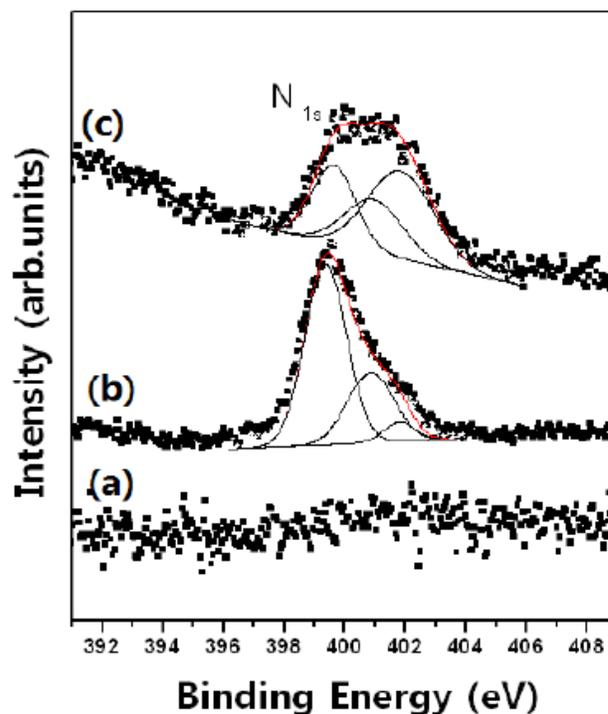


Fig. 1. High-resolution XPS spectra of N1s obtained from (a) SiO₂/Si, (b) amine-SAM/SiO₂/Si, and (c) immobilized Au on amine-SAM/SiO₂/Si substrates.

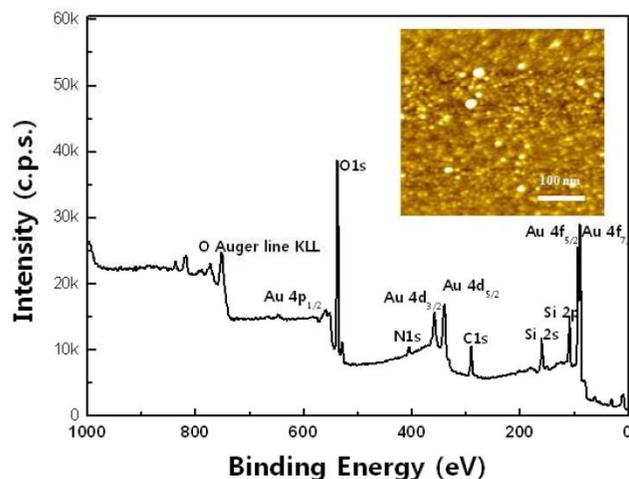


Fig. 2. XPS spectrum of the NH₂-SAM surface after soaking 1 hr in the Au-dispersed solution. The inset shows an AFM image of immobilized AuNPs on an amine-modified substrate.

The XPS results of the substrate before (Figure 1(a)) and after (Figure 1(b)) modifications with 3-aminopropyltriethoxysilane (APTES) are summarized in Figure 1. Assembly of the APTES on the substrate was confirmed by the emergence of the core-level N_{1s} spectrum (Figure 1(b)). This N_{1s} spectrum of the APTES is fitted by one peak at ca. 399.2 eV and two shoulders at ca. 400.7 and 401.8 eV, which can be assigned to free amines on the substrate [7], Au-coordinated amines [8], and protonated amines [9], respectively. However, after soaking the APTES-assembled wafer in the AuNPs suspension (pH 6), the peak area of the three different amines changed (Figure 1(c)). In particular, the peak located at ca. 401.8 eV, which is associated with protonated amine groups, increased significantly. These phenomena suggest that free amine on the wafer can capture protons from the AuNPs suspension with Ph 5 and be converted into a protonated amine, resulting in a positively-charged substrate. These protonated amines can immobilize AuNPs via an electrostatic interaction with the negatively-charged AuNPs surface. Figure 2 showed the XPS and AFM results from soaking the APTES-assembled wafer in the AuNPs suspension. As shown in a typical wide scan spectrum, all the standard photoelectron and Auger lines of silicon, oxygen, nitrogen, gold, and adventitious carbon were present. Particularly, strong Au metal peaks were observed at 83.8 eV and 87.5 eV, which correspond to $4f_{7/2}$ and $4f_{5/2}$, respectively. AFM analysis of the AuNPs assembled layer showed that AuNPs were closely immobilized on the amine-modified wafer.

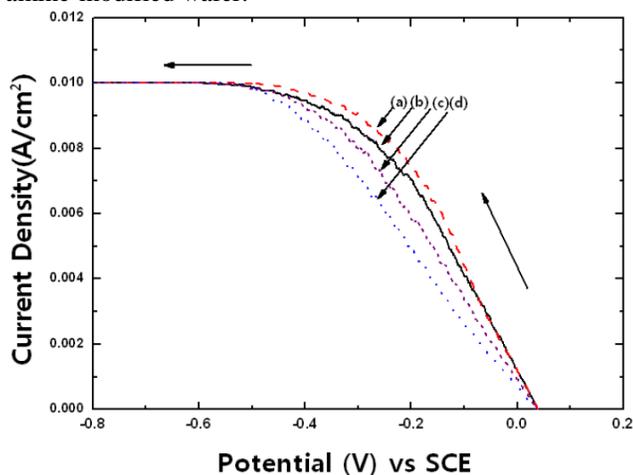


Fig. 3. Cathodic polarization curves for copper electrodeposition from (a) additive-free, (b) PEG4000, (c) Cl-PEG4000-SPS, and (d) Cl-PEG4000. The rotation speed of RDE and the potential scan rate were 200 rpm and 2 mVs⁻¹, respectively.

The steady-state I-E characteristics for Cu ED from electrolytes containing Cl-PEG-SPS are shown in Figure 3. The polarization curve of the additive-free bath (Figure 3(a)) showed that the current density gradually increased from the beginning of the potential scan and reached a plateau at -0.5 V vs SCE. This plateau corresponds to the mass-transfer-limiting current for the reduction of cupric

ions. The addition of PEG to the additive free bath (Figure 3(b)) slightly decreased the limiting current density. On the other hand, when Cl⁻ was added to the electrolyte containing PEG (Figure 3(d)), the Cu deposition rate significantly decreased due to the absorbed PEG molecules (Cl-Cu⁺-PEG complex) blocking the transport of cupric ions to the Cu electrode's surface [10]. The polarization curve in Figure 5(c) shows that the addition of SPS to the Cl-PEG bath led to an acceleration of the deposition rate. The SPS changed the nucleation process (enhanced cuprous-complex formation) by providing growth sites and accelerated the charge transfer process at the copper interface [4]. As a result, a large differential deposition rate was induced between the accelerator (Cu(I)(thiolate)_{ad}) sites and the absorbed suppressor (Cl-Cu⁺-PEG complex).

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