Analytic Potential Solution for Modeling the Symmetric DG Accumulation Mode MOSFETs

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ABSTRACT

This paper presents a potential model for symmetrical DG accumulation mode MOSFETs. The proposed model is derived from complete 1-D Poisson-Boltzmann equation and takes three components of net charge density (fixed charge, holes and electrons) into account. This model provides a smooth potential solution from subthreshold to accumulation regions. The solved potentials are verified by numerical results for various bias condition and different structure parameters. In order to model short channel effects like CLM and DIBL, a linear shift in flatband voltage using a fitting parameter is included. The presented potential solution provides the framework of a physically-based DG AMOSFET compact model for circuit simulation.

***Keywords**:* symmetric DGMOSFET, analytic potential model

1 INTRODUCTION

As the continuous scaling down of integrated circuits calls for aggressive demand to conventional devices, novel devices are gaining attention for their potential to become an alternative to traditional counterparts. Among them, accumulation mode MOSFETs (AMOSFETs), which shows their merits including higher transconductance [1], lower vertical field [2], lower sensitivity to oxide thickness variations [2] and better subthreshold performance [2-4] are under study in a wide range. Device fabrication and tests have been conducted using SOI and nanowire (NW) AMOSFETs. The experimental data is in favor of the advantages of AMOSFETs aforementioned. Simulation results by numerical simulator like TCAD are also verified [4]. However, previously published analytic models on AMOSFETs failed to account for all three terms, namely fixed charge, electrons and holes, in the expression of net charge density. Models on undoped DG or SRG MOSFETs can be applicable for AMOSFETs with the same structure by adding a minus sign in front of q [5-6]. These models neglect fixed charge and minority carriers, thus introduce inaccuracy in the subthreshold region for doped devices. R.Murali provided short channel modeling of bulk AMOFETs in the subthreshold region and performed analysis on threshold voltage rolling off, with only fixed charge considered [7]. This model can only be used to analyze device performance in subthreshold and is not able to predict saturation current.

To build a current model which can provide accurate simulation results both in subthreshold and saturation region, it is necessary to solve complete Poisson-Boltzmann equation to obtain potential distribution in advance. This paper aims to provide such a potential model taking fixed charge, electrons and holes into account for symmetrical DG AMOSFETs, as the prerequisite to current model. The calculation method is described in detail in Section II. Section III presents simulated potentials provided by the proposed model and verified them with numerical results and Section IV concludes the whole paper.

2 POTENTIAL MODEL

For p-type symmetric DG structure, the general 2-D Poisson-Boltzmann equation can be written as:

$$\frac{d^2\psi}{dx^2}+\frac{d^2\psi}{dy^2}=\frac{qN_a}{\varepsilon}[1-e^{\beta(V_{ch}-\psi)}+e^{\beta(\psi-2\psi_f)}] \qquad (1)$$

With the boundary condition given by:

$$\frac{d\psi}{dx}|_{x=0}=0\ ,\ \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}}=\frac{C_{ox}}{\varepsilon}(V_{gs}-V_{fb}-\psi_s)$$

In this paper, the x-axis and y-axis are chosen to be normal to and along the channel direction, respectively. The x-coordinate of the center of channel is set to *0* while the surface's is $\pm t_{si}/2$.

To simplify, Gradual-Channel-Approximation (GCA) where electrical field along y-direction can be neglected is adopted, making the 2-D equation to 1-D form as:

$$\frac{d^2\psi}{dx^2}=\frac{qN_a}{\varepsilon}[1-e^{\beta(V_{ch}-\psi)}+e^{\beta(\psi-2\psi_f)}] \qquad (2)$$

To accurately model the *I-V* characteristics for DG AMOSFETs, any of the three terms of the right hand side of Eq.(2) should not be neglected. However, to the authors' knowledge, no analytic solution to Eq.(2) has been found yet. Previously published papers on AMOSFETs either used a regional method with smooth function [8] or neglected fixed charge (substrate doping) to obtain an analytic solution [5-6].

For a given bias voltage, only surface potential ψ_s and central potential ψ_0 at both source and drain end are important to model drain current in AMOSFETs. Considering this fact, we proposed the following method to obtain ψ_s and ψ_0 as the function of V_{gs} and V_{ch}.

Multiplying both side of Eq.(2) with $2d\psi$, and integrating from $x = 0$ to $x = t_{si}/2$ gives:

$$(\frac{d\psi}{dx})^2 \mid_{x=\frac{t_{si}}{2}} = \frac{2qN_a}{\varepsilon}[\psi + \frac{1}{\beta}e^{\beta(V_{ch}-\psi)} + \frac{1}{\beta}e^{\beta(\psi-2\psi_f)}]\mid_{\psi_0}^{\psi_s} \quad (3)$$

Substituting left-hand-side of Eq.(3) with boundary condition gives the first equation relating ψ_s to ψ_0:

$$[C_{ox}(V_{gs}-V_{fb}-\psi_s)]^2 = 2\varepsilon qN_a[\psi + \frac{1}{\beta}e^{\beta(V_{ch}-\psi)} + \frac{1}{\beta}e^{\beta(\psi-2\psi_f)}]\mid_{\psi_0}^{\psi_s} \quad (4)$$

Since there are two unknowns (ψ_s and ψ_0), another equation is needed. Integrating Eq.(1) from $x = 0$ to $x = t_{si}/2$ twice gives:[9]

$$\psi_s = \psi_0 + \frac{qN_a t_{si}^2}{8\varepsilon}\int_0^1\int_0^1[1 - e^{\beta(V_{ch}-\psi)} + e^{\beta(\psi-2\psi_f)}]dx'dx' \quad (5)$$

Where $x' = 2x/t_{si}$ is normalization of vertical position in the channel.

The integrating in Eq.(5) can not be conducted unless using a numerical method. However, it is possible to adopt the local approximation to obtain a solution with acceptable error. Thus the integrating can be done by a series of iteration [10].

The iteration starts from a rough approximation: $\psi \approx \psi_0$. By Substituting ψ with ψ_0 in Eq.(5) and integrating, a better approximation is given by: $\psi = \psi_0 + hx'^2/\beta$,where

$$h = \beta\frac{qN_a t_{si}^2}{8\varepsilon}[1 - e^{\beta(V_{ch}-\psi_0)} + e^{\beta(\psi_0-2\psi_f)}]$$

Repeating the substituting and integrating again gives an even more accurate approximation that:

$$\psi_s = \psi_0 + \frac{qN_a t_{si}^2}{8\varepsilon}[1 - 2S_A e^{\beta(V_{ch}-\psi_0)} + 2S_I e^{\beta(\psi_0-2\psi_f)}] \quad (6)$$

Where $S_A = \sum_{n=0}^{\infty}\frac{(-h)^n}{n!(2n+1)(2n+2)}$ and $S_I = \sum_{n=0}^{\infty}\frac{h^n}{n!(2n+1)(2n+2)}$.

It is obvious that further iteration makes the solution more precise but requires more a complex expression and longer computing time. As simulation results indicate that Eq.(6) is enough for provide good agreement with numerical solutions shown in Section III, iteration is ended at Eq.(6).

By solving the equation group consists of Eq.(4) and Eq.(6) using Newton-Raphson (NR) method, a continuous and smooth potential solution is obtained. In this paper, an analytic potential solution [5] taking only majority carrier into account is used as the initial guess for ψ_s and ψ_0. Then ψ_0 is updated by Eq.(6) using first-order NR method. After that, ψ_s is updated by Eq.(4) using second-order NR method. This loop continues until both ψ_s and ψ_0 convergence.

3 SIMULATION RESULTS

In this section, a numerical simulator to solve for static potential in DG AMOSFETs is used to verify the surface potential ψ_s and central potential ψ_0 obtained with the method described in Section II. This numerical simulator solves 1-D Poisson-Boltzmann Equation with its boundary condition using central difference method (CDM). If not specified, a mid-gap gate electrode is assumed, so that:

$$V_{fb} = \phi_{ms} = -\frac{kT}{q}\ln(\frac{N_a}{n_i})$$

Fig.1 presents ψ_s and ψ_0 obtained from solution to Eq.(4) and Eq.(6) and compares the potential with numerical results. From Fig.1, good agreement is achieved for ψ_s and ψ_0 in all regions (from accumulation to inversion). There are slight differences between ψ_0 curves between numerical results at strong accumulation or inversion regions, which come from the approximations made in Eq.(6). However, such small error in ψ_0 only brings little inaccuracy to drain current in the simulation.

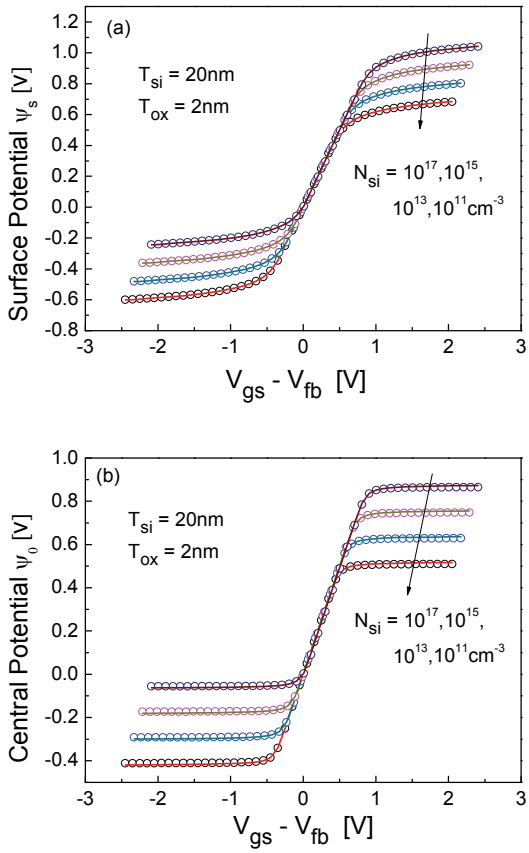

Fig 1: Comparison of calculated (lines) surface potential ψ_s (a) and central potential ψ_0 (b) at various applied gate voltage V_{gs} with numerical results (dots) for symmetric DG AMOSFETs. The thickness of silicon film is 20nm, and the thickness of oxide layer is 2nm. Channel doping ranges from 10^{11}cm^{-3} (intrinsic) to 10^{17}cm^{-3}.

For varying structure parameters like T_{si} and T_{ox}, Fig.2 and Fig.3 present corresponding potential obtained as a function of applied gate voltage. In typical situations, terms including ψ_0 in Eq.(4) can be neglected, so ψ_s largely depends on the solution of the following equation:

$$[C_{ox}(V_{gs}-V_{fb}-\psi_s)]^2 = 2\varepsilon qN_a[\psi_s + \frac{1}{\beta}e^{\beta(V_{ch}-\psi_s)} + \frac{1}{\beta}e^{\beta(\psi_s-2\psi_f)}] \quad (7)$$

Further simplification can be achieved by neglecting fixed charge and electrons in accumulation region that:

$$C_{ox}(V_{gs}-V_{fb}-\psi_s) = \sqrt{2\varepsilon qN_a\frac{1}{\beta}e^{\beta(V_{ch}-\psi_s)}} \quad (8)$$

T_{si} does not have direct influence on the constants

appeared in Eq.(8). As a result, T_{si} has little control over ψ_s, which can be verified by Fig.2(a) where surface potential for different T_{si} overlap. On the contrary, the solution of Eq.(8) is affected by T_{ox} for the reason that gate capacity C_{ox} follows the change in T_{ox}. For thinner T_{ox}, C_{ox} increases, leading to an increment in the exponential term and causing ψ_s to be more negative. This tendency can be observed from Fig.3(a).

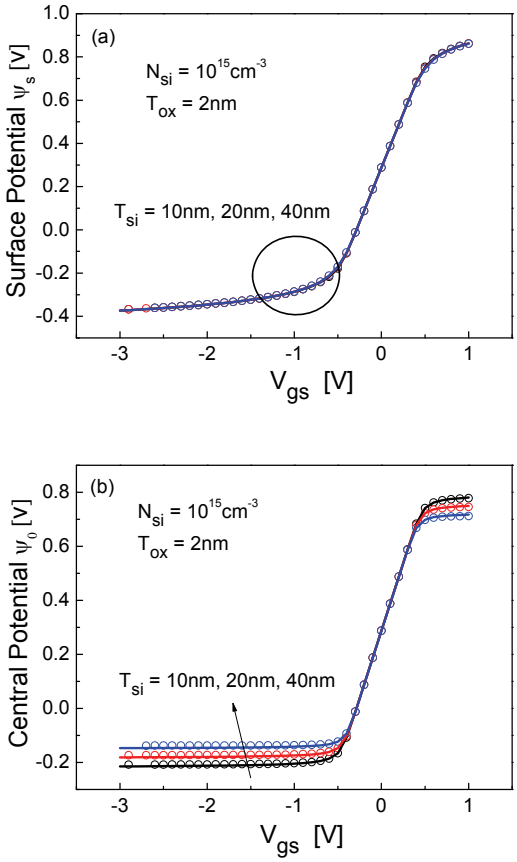

Fig 2: Comparison of calculated (lines) surface potential ψ_s (a) and central potential ψ_0 (b) at various applied gate voltage V_{gs} with numerical results (dots) for symmetric DG AMOSFETs. The thickness of oxide layer is 2nm, and doping concentration is 10^{15}cm^{-3}. The thickness of silicon film ranges from 10nm to 40nm.

Both Fig.2 and Fig.3 can be understood from a more physical angle. In the accumulation region, ψ_s is fixed for the same reason that ψ_s is fixed in the vicinity of $2\psi_f$ in strong inversion. And thicker T_{ox} tends to lower the electrical field in the channel, resulting in decreasing ψ_s .

Similar analysis on Eq.(6) can account for changes in ψ_0. By neglecting fixed charge and electrons in accumulation region, Eq.(6) transform to:

$$\psi_s = \psi_0 - \frac{qN_a t_{si}^2}{4\varepsilon} e^{\beta(V_{ch}-\psi_0)} \sum_{n=0}^{\infty} \frac{(-h)^n}{n!(2n+1)(2n+2)} \qquad (9)$$

Where $h = -\beta q N_a t_{si}^2 e^{\beta(V_{ch}-\psi_0)} / 8\varepsilon$.

When T_{si} increases, ψ_s does not change, so the right hand side of Eq.(9) should stay the same, causing ψ_0 to be more positive. This tendency is verified by Fig.2(b).

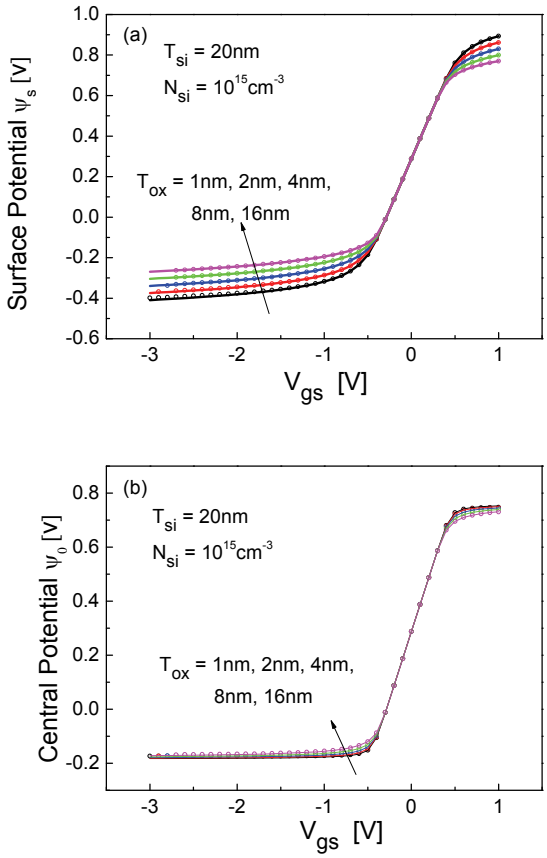

Fig 3: Comparison of calculated (lines) surface potential ψ_s (a) and central potential ψ_0 (b) at various applied gate voltage V_{gs} with numerical results (dots) for symmetric DG AMOSFETs. The thickness of silicon film is 20nm, and doping concentration is 10^{15}cm^{-3}. The thickness of oxide layer ranges from 1nm to 16nm.

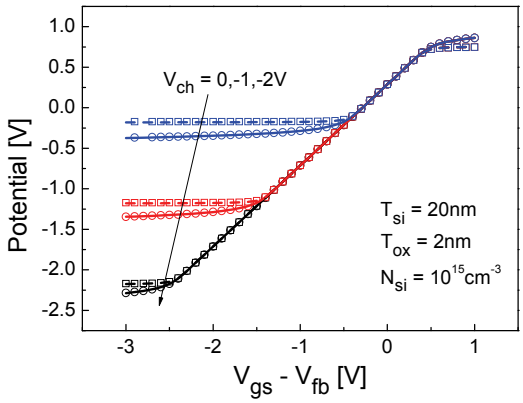

Fig 4: Comparison of calculated surface potential ψ_s (solid lines) and central potential ψ_0 (dashed line) at various applied gate voltage V_{gs} with numerical results (dots and squares) for symmetric DG AMOSFETs with doping concentration of 10^{15}cm^{-3}. The thickness of silicon film is 20nm, and the thickness of oxide layer is 2nm. Results for channel potential V_{ch} of 0V,-1V,-2V are presented.

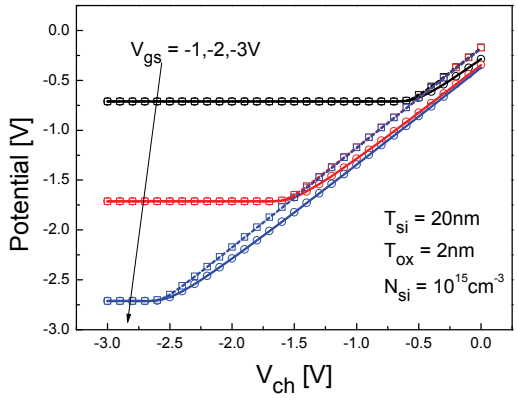

Fig 5: Comparison of calculated surface potential ψ_s (solid lines) and central potential ψ_0 (dashed lines) at various channel potential V_{ch} with numerical results (dots and squares) for symmetric DG AMOSFETs with doping concentration of $10^{15}cm^{-3}$. The thickness of silicon film is 20nm, and the thickness of oxide layer is 2nm. Applied gate voltage V_{gs} ranges from -1V to -3V.

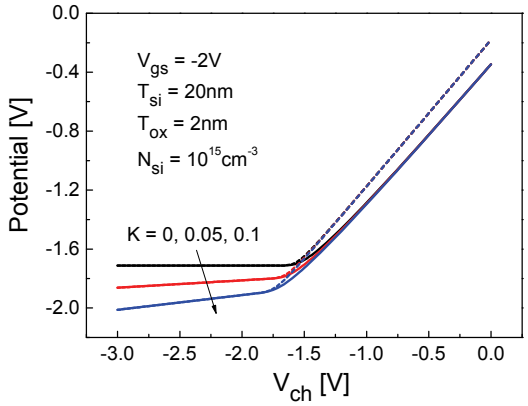

Fig 6: Simulation results of surface potential ψ_s (solid) and central potential ψ_0 (dashed) in symmetric DG AMOSFETs with doping concentration of $10^{15}cm^{-3}$, for various K. The thickness of silicon film is 20nm, and the thickness of oxide layer is 2nm. Applied gate voltage V_{gs} is fixed at -2V.

Fig.4 illustrates the modulation of V_{ch} on ψ_s and ψ_0. From Fig.4, it can be observed that for a small $|V_{gs}|$, V_{ch} only slightly affects potential that three groups of curves overlap in this region. Divergence happens when $|V_{gs}|$ increases. Then both ψ_s and ψ_0 are fixed at the point determined by the structure parameters and applied voltage.

When a p-type AMOSFET is in operation, the quasi-Fermi level V_{ch} in the channel varies from 0 to V_{ds} (<0) along the y-direction. Fig.5 shows ψ_s and ψ_0 obtained from solution to Eq.(4) and Eq.(6) for various V_{ch} in comparison with numerical results. Both ψ_s and ψ_0 are modulated by V_{ch}. When AMOSFETs are operating in saturation region, both ψ_s and ψ_0 keep constant though $|V_{ch}|$ increases, fixing drain current at its peek value.

It should be pointed out that because GCA where electrical filed along the y-direction can be neglected is assumed in derivation of Eq.(2-6), the proposed model fails to account for short channel effects like Channel Length Modulation (CLM) and Drain Induced Barrier Lower (DIBL). But with a linear shift in the flatband voltage V_{fb} proportional to the channel potential V_{ch} adopted [8, 11], this model can thus account for both CLM and DIBL. An empirical constant K is used and now V_{fb} is given by $V_{fb} = V_{fb}^{'} - K \times V_{ch}$, where $V_{fb}^{'}$ denotes the flatband voltage at $V_{ch} = 0$.

Fig.6 presents simulation results for K with different values. Both ψ_s and ψ_0 no longer saturate even at high $|V_{ch}|$, but continue to be more negative, which would result in finite output resistance in the saturation.

4 CONCLUSION

In this work, a potential model for symmetric DG AMOSFETs taking both fixed charge and mobile carriers is proposed. Verification is done by comparing the model to numerical results for devices with different structure parameters and various bias conditions. Good agreement is achieved for all situations, which demonstrates the accuracy of the proposed model. Moreover, a fitting constant K is introduced to the model to account for CLM and DIBL. This potential model can be served to calculate accurate surface potential and central potential needed for drain current model which will be reported in another work.

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REFERENCES

[1] T. Yoshitomi, M. Saito, H. Oguma, Y. Akasaka, M. Ono, H. Nii, Y. Ushiku, H.Iwai, and H. Hara, *Symp. VLSI Tech. Dig.*, 1993, pp. 99-100.
[2] A. W. Vinal, U.S. Patent Number 4 990 974, Feb. 5, 1991.
[3] T. Enda and N. Shigyo, *Elect. Comm.*, vol.79, no.11, pp.43-49, Nov. 1996.
[4] M. M. Iqbal, Y. Hong, P. Garg, F. Udrea, P. Migliorato, and S. J. Fonash, *IEEE Trans. Electron Devices*, vol.55, no.11, pp.2946-2959, Nov. 2008.
[5] Y. Taur, X. Liang, W. Wang, and H. Lu, *IEEE Electron Devices Lett.* vol.25, no.2, pp.107-109, Feb. 2004.
[6] D. Jimenez, B. Iniguez, J. Sune, L. F. Marsal, J. Pallares, J. Roig, and D. Flores, *IEEE Electron Devices Lett.* vol.25, no.8, pp.571-573, Aug. 2004.
[7] R. Murali, B. L. Austin, L. Wang, and J. D. Meindl, *IEEE Trans. Electron Devices*, vol.51, no.6, pp.940-947, June, 2004.
[8] C. J. Nassar, C. A. Williams, D. Dawson-Elli, and R. J. Bowman, *IEEE Trans. Electron Devices*, vol.56, no.9, pp.1974-1979, Sept. 2009.
[9] F. Liu, J. He, J. Zhang, Y. Chen, and M. Chan, *IEEE Trans. Electron Devices*, vol.55, no.12, pp.3494-3502, Dec. 2008.
[10] P. Francis, A. Terao, D. Flandrem, and F. Van de Wiele, *Solid State Electron.*, vol.38, no.1, pp. 171-176, Jan. 1995.
[11] B. Iniguez, V. Dessard, D. Flandre, and B. Gentinne, *IEEE Trans. Electron Devices*, vol.46, no.12, pp.2295-2303, Dec. 1999.