Analytical Modeling of the Subthreshold Electrostatics of Nanoscale GAA Square Gate MOSFETs

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ABSTRACT

An analytical model is presented of the 3-D subthreshold electrostatics of low-doped nanoscale square-gate MOSFETs operating in the subthreshold domain. The model is based on a solution of the 3-D Laplace equation utilizing the four-fold symmetry of the cross sections perpendicular to the channel axis and assuming parabolic potential distributions in the directions perpendicular to the gates for the central regions. Near source and drain other functional forms are used to precisely account for the transition to a flat potential at the two contacts. From the resulting electrostatics, capacitances, drain current, and scaling properties are obtained. The model compares very well with numerical calculations obtained from the ATLAS device simulator.

Keywords: Square gate MOSFET, electrostatic potential, subthreshold current, capacitances.

1 INTRODUCTION

Multigate nanoscale MOSFETs are strong candidates for replacing conventional single gate MOSFETs within the coming years. To combat the debilitating short-channel effects that result from the loss of gate control, gate-all around (GAA) devices, such as cylindrical [1-3] and square gate MOSFET [4], are superior to the double-gate (DG) MOSFETs. To our knowledge, very little work has been done in the modeling of square gate GAA devices. In this paper, an analytical model is presented of the 3-D subthreshold electrostatics of short-channel, low-doped, square gate MOSFETs, from which expressions for the basic electrical properties of this device are obtained.

The present model is based on the four-fold symmetry of the cross sections perpendicular to the channel axis, and the assumption of parabolic potential distributions in the directions perpendicular to the gates in the central regions of the device. From this, an approximate, analytic, long-channel solution for inter-electrode body potential distribution is obtained from the 3-D Laplace equation. However in order to precisely account for short-channel effects, the electrostatics near source and drain needs to be adjusted. This is done by introducing alternate functional forms and by applying auxiliary boundary conditions obtained either from conformal mapping analyses [1,2] or, alternatively, from numerical simulations.

The square gate device considered has gate length L = 30 nm, insulator thickness t_{ox} = 1.5 nm, silicon thickness t_{si} = 12 nm, and insulator relative dielectric constant ε_{ox} = 7. The doping density of the p-type silicon body is $N_a = 10^{15}\text{cm}^{-3}$. As gate material, we selected a near-midgap metal with work function 4.53 eV. Idealized Schottky contacts with a work function of 4.17 eV (corresponding to that of n+ silicon) are assumed for source and drain. To facilitate the modeling, the gate insulator is replaced by an electrostatically equivalent silicon layer with thickness $t'_{ox} = t_{ox}\varepsilon_{si}/\varepsilon_{ox}$, where ε_{si} is the relative permittivity of silicon.

2 DEVICE ELECTROSTATICS

2.1 Long-Channel Potential Distribution

The potential distribution in the parts of the device not too close to the source and drain can be modeled as

$$\varphi(x,y,z) = \hat{\varphi}(0,0,z)\left[1-\left(\frac{2x}{a}\right)^2\right]\left[1-\left(\frac{2y}{a}\right)^2\right]+V_{gs}-V_{FB}, \tag{1}$$

where x, y, and z are the spatial coordinates as indicated in Fig. 1, $a = t'_{ox} + 2t'_{ox}$ is the thickness of the extended body including the gate insulator, and $\hat{\varphi}(0,0,z) = \varphi(0,0,z) - V_{gs} + V_{FB}$ is the body potential along the source-drain (S-D) axis referred to the potential at the gate/extended body interface. Taking second derivatives of (1) with respect to x and y, the 3-D Laplace equation simplifies to the following form,

$$\frac{\partial^2\hat{\varphi}(0,0,z)}{\partial z^2}+\hat{\varphi}(0,0,z)\left[\frac{32(x^2+y^2)-16a^2}{a^4-4a^2(x^2+y^2)+16x^2y^2}\right]=0\ , \tag{2}$$

which, along the source-drain symmetry axis (x = 0, y = 0), reduces to

$$\frac{\partial^2\hat{\varphi}(0,0,z)}{\partial z^2}-\frac{\hat{\varphi}(0,0,z)}{\lambda^2}=0\ , \tag{3}$$

where $\lambda = a/4$ is the characteristic length of field penetration from source/drain into the device body. Solving (3) for

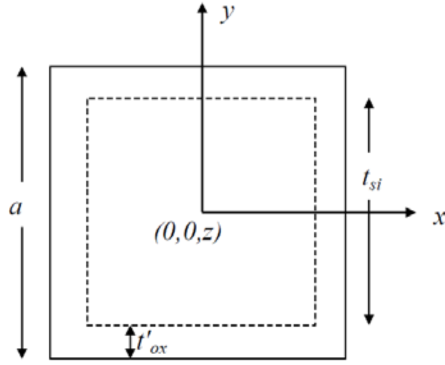


Figure 1: Cross section perpendicular to the channel axis of the square-gate MOSFET extended body.

the boundary conditions $\hat{\varphi}(0,0,0) = V_{bi} - V_{gs} + V_{FB}$ and $\hat{\varphi}(0,0,L) = V_{bi} + V_{ds} - V_{gs} + V_{FB}$, where V_{bi} is the built in voltage at the two contacts and V_{ds} is the drain-source voltage, we find the following solution

$$\hat{\varphi}(0,0,z) = \frac{(V_{bi}-V_{gs}+V_{FB})\sinh\left(\frac{L-z}{\lambda}\right)+(V_{bi}+V_{ds}-V_{gs}+V_{FB})\sinh\left(\frac{z}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}. \qquad (4)$$

Combined with (1), this gives the full 3-D potential distribution in the extended device body of a long-channel device.

2.2 Short-Channel Potential Distribution

As discussed in Section 1, the above model does not include short-channel effects. It is apparent that the parabolic approximations applied in the cross sectional potential profiles of (1) are not applicable near source and drain. Instead, inside the silicon body, these profiles should flatten when approaching these electrodes. This will also affect the potential distribution along the z-axis.

The latter can be remedied by introducing as extra boundary conditions the potential φ_c at the device center (0,0,L/2) and the electrical field E_s at the center of the source (0,0,0). These can be obtained by analyzing the device using conformal mapping techniques, as was shown previously for cylindrical gate MOSFETs [1-3], or by using such values obtained from numerical simulations [5]. To satisfy these conditions, (4) can then be adjusted by using a z-dependent λ of the form

$$\lambda(z) = \lambda_c + \gamma(z - L/2)^2, \qquad (5)$$

where

$$\lambda_c = \lambda(L/2) = L/2\cosh^{-1}\left(\frac{V_{bi}-V_{gs}+V_{FB}+V_{ds}/2}{\varphi_c-V_{gs}+V_{FB}}\right), \qquad (6)$$

$$\gamma = \left(\frac{2}{L}\right)^2\left[\frac{V_{bi}-V_{gs}+V_{FB}}{E_s} - \lambda_c\right]. \qquad (7)$$

Hence, an updated model for $\hat{\varphi}(0,0,z)$ is obtained by applying (5) to (7) in (4). Combined with (1), taking $x = y = 0$, gives $\varphi(0,0,z)$ along the entire source-drain axis. As shown in Fig. 2, a comparison of this model with numerical simulations using the Atlas TCAD simulator [4] indicates a very good agreement.

Close to source and drain, the flattening of the potential in the (x,y) cross sections typically takes place within the characteristic distance of source and drain, now defined by $\lambda_s = \lambda(0) = \lambda_c + \gamma(L/2)^2$. In the central device region, defined by $\lambda_s \le z \le L - \lambda_s$, we model the 3-D potential profiles according to expressions (1) to (7). This gives rise to potential distribution in the (x,y) plane as indicated by schematic equipotential contours to the upper right in Fig. 3. More precisely, Fig. 4a shows a comparison between modeled and simulated potential distributions along the x-axis and along the diagonal direction of the (x,y) cross section at the device center ($z = L/2$) for $V_{ds} = V_{gs} = 0$ V. Again, we find an excellent agreement between the modeled and simulated results.

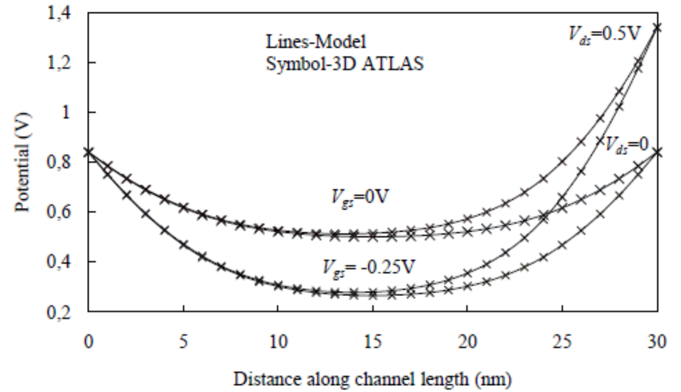


Figure 2: Comparison of modeled and numerical simulations of the potential distribution along the source-drain axis for different values of V_{ds} and V_{gs}.

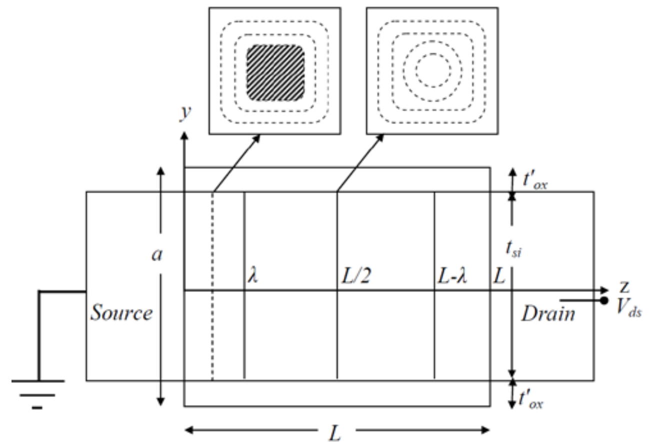


Figure 3: Longitudinal cross section of the device along the channel axis with schematic equipotential contours plot in two different (x,y) planes.

However, for $z < \lambda_s$ and $z > L - \lambda_s$, we propose the introduction of a z-dependent equipotential (flat) area of value $\varphi(0,0,z)$ about the z-axis, as indicated in gray in the upper left (x,y) cross section in Fig. 3. The width of area $a_o(z)$ is zero at $z = \lambda_s$ and $z = L - \lambda_s$, and is assumed to increase linearly towards the source or drain to cover these contacts at $z = 0$ and $z = L$, respectively, i.e., $a_o(z) = t_{si}(1-z/\lambda_s)$ near source and $a_o(z) = t_{si}(1-(L-z)/\lambda_s)$ near drain.

Outside the equipotential (gray) area, we use a potential profile based on (1), which is suitably scaled such that it exactly matches that of the gray area at its periphery. In the upper left cross section of Fig. 3, such a potential profiles is schematically indicated in terms of equipotential contours. Hence, the modified potential distribution for $z < \lambda_s$ and $z > L - \lambda_s$ can be expressed as follows:

$$\varphi(x,y,z) = \varphi(0,0,z) \quad (8)$$

in the equipotential (gray) area, and

$$\varphi(x,y,z) = V_{gs} - V_{FB} + \hat{\varphi}(0,0,z)\,\frac{1-4(x^2+y^2)/a^2+16x^2y^2/a^4}{1-[a_o(z)/a]^2} \quad (9)$$

outside this area. In Figure 4b, is shown a comparison between the modeled and numerical simulations of the potential distribution within the silicon body along the x-axis at different positions z along the channel axis. To test the scaling properties of the model, a similar comparison is shown in Fig. 5 for the center potential φ_c versus gate length, obtained from the conformal mapping analysis. In both cases, quite satisfactory agreement is observed.

3 CAPACITANCES

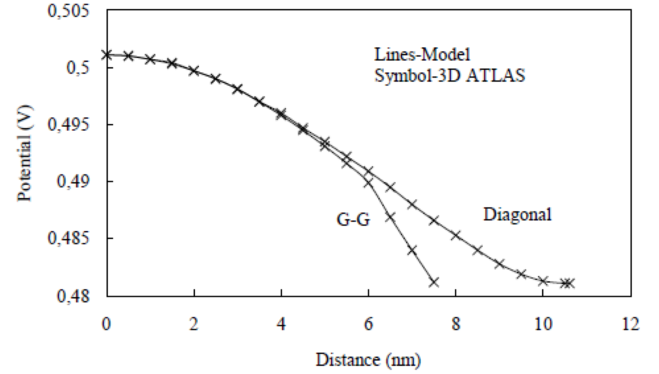
From the above modeling, we can calculate the intrinsic device capacitances in subthreshold, where they are dominated by the inter-electrode coupling. In the short-channel case, we obtain the following analytical expression for the perpendicular electric field at one of the four identical sidewalls of the gate:

$$E_g\left(\frac{a}{2},y,z\right) = -\left.\frac{\partial\varphi(x,y,z)}{\partial x}\right|_{x=a/2} = \hat{\varphi}(0,0,z)\begin{cases}4/a - 16y^2/a^3, & \lambda_s \le z \le L-\lambda_s\\ \dfrac{4/a - 16y^2/a^3}{1-[a_o(z)/a]^2}, & z<\lambda_s,\ z>L-\lambda_s\end{cases} \quad (10)$$

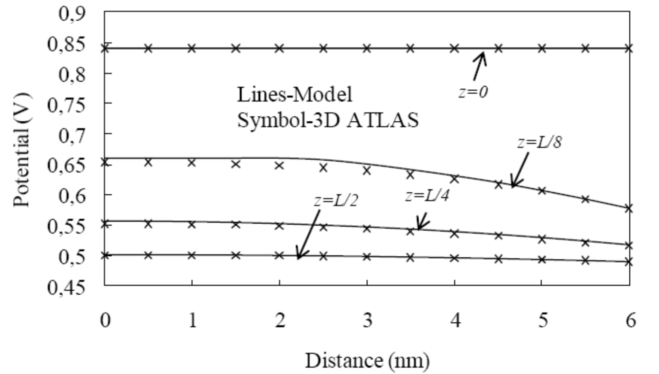
By integrating this along y-direction and accounting for all four sidewalls, we find the linear gate charge density distribution along the z-direction (ε_0 is vacuum permittivity)

$$q_g(z) = 4\epsilon_{si}\epsilon_0\int_{-a/2}^{a/2} E_g\left(\frac{a}{2},y,z\right)dy =$$

$$\frac{32\epsilon_{si}\epsilon_0}{3}\hat{\varphi}(0,0,z)\begin{cases}1, & \lambda_s \le z \le L-\lambda_s\\ \dfrac{1}{1-[a_o(z)/a]^2}, & z<\lambda_s, z>L-\lambda_s\end{cases} \quad (11)$$



a)



b)

Figure 4: Comparison of modeled and numerical simulations for potential distributions in the (x,y)-plane. (a) along the x-axis and the diagonal at $z = L/2$ and (b) along the x-axis within the silicon body for different positions along the S-D axis. $V_{ds} = V_{gs} = 0$ V.

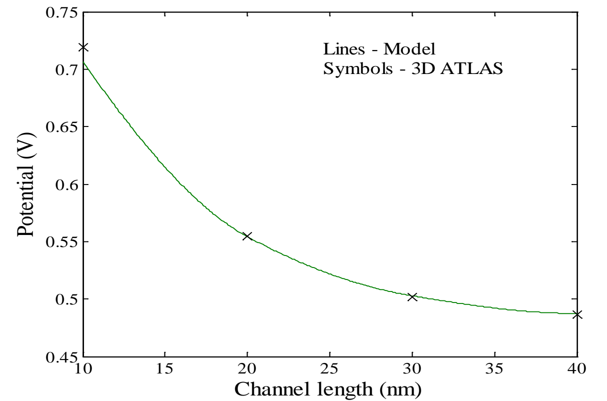


Figure 5: Comparison of modeled and numerical simulations of the device center potential φ_c versus gate length. The modeling results are obtained using conformal mapping techniques. $V_{ds} = V_{gs} = 0$ V.

Using (4) - (7) for $\hat{\varphi}(0,0,z)$, the above expression for $a_o(z)$, and integrating (11) from source to drain, we obtain the total gate charge Q_g. Because of overall charge conservation, Q_g must have an equal but opposite countercharge shared between source and drain. A reasonable approximation is to assign the source charge Q_s as the countercharge of the gate charge in the range $0 \leq z \leq L/2$, and the drain charge Q_d as the countercharge of the gate charge in $L/2 \leq z \leq L$. The subthreshold trans- and self-capacitances are then determined as derivatives of these charges with respect to the electrode voltages [2]. Because of symmetry considerations and charge conservation, we observe that many of these are closely related, i.e., $C_{gs} = C_{gd} = C_{sg} = C_{dg} = C_{gg}/2$, $C_{ds} = C_{sd}$, and $C_{ss} = C_{dd} = C_{gs} + C_{ds}$.

4 DRAIN CURRENT

A unified model for subthreshold current can be given as [6]:

$$I_d = \frac{2\mu V_{\rm th} n_{sm}}{\sigma\sqrt{\pi}} \frac{1 - exp(-V_{ds}/V_{\rm th})}{Erf\left(\frac{L-2z_m}{2\sigma}\right) + Erf\left(\frac{L+2z_m}{2\sigma}\right)} \quad (12)$$

This model is based on the assumption that the inversion charge sheet density assumes a normal distribution near the top of the barrier, i.e., at $z = z_m$. Here we have assumed a parabolic potential distribution along the S-D symmetry line within a distance σ of $z = z_m$, corresponding to an increase of the potential by a thermal voltage compared to that of the top of the barrier. The total integrated charge density at the top of the barrier is denoted n_{sm}. For a square gate device, we have:

$$n_{sm} = \frac{n_i^2}{N_a} \int_{-a/2}^{a/2} \int_{-a/2}^{a/2} exp\left[\frac{\varphi(x,y,z_m)}{V_{\rm th}}\right] dxdy, \quad (13)$$

In evaluating n_{sm}, we use (1) for the potential distribution in the (x,y)-plane to obtain an analytical expression in terms of error functions. Figure 6 shows the modeled current compared with numerical simulations for a 30 nm long device.

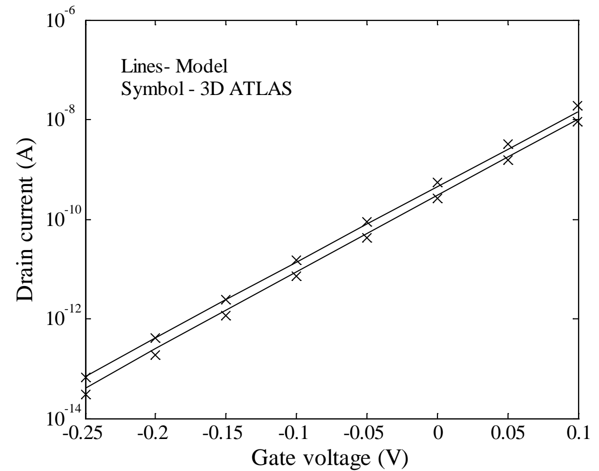


Figure 6: I_d-V_{gs} characteristics for 30 nm device. The upper and lower curves correspond to V_{ds} = 1V (upper curve) and V_{ds} = 0.1V (lower curve), respectively. V_{gs} = 0 V.

5 CONCLUSION

The electrical properties of long- and short-channel gate-all-around MOSFETs with a quadratic cross section are analyzed and modeled. The modeling of the device electrostatics is based on the 3-D Laplace equation of the extended device body, where the gate insulator is replaced by an electrostatically equivalent silicon layer. To account for the short-channel effects, the resulting long-channel potential distribution is modified to include the properties of the electrostatics near source and drain. Based on these results, the intrinsic capacitances and the drain current are derived. The model agrees very well with numerical simulations.

ACKNOWLEDGMENT

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