Process- and Random-Dopant-Induced Characteristic Variability of SRAM with nano-CMOS and Bulk FinFET Devices

Tien-Yeh Li, Chih-Hong Hwang and Yiming Li*

Department of Communication Engineering, National Chiao Tung University,
1001 Ta-Hsueh Road, Hsinchu 300, Taiwan; *Email: ymli@faculty.nctu.edu.tw
Phone: 886-3-5712121 ext. 52974; Fax: 886-3-5726639

ABSTRACT

In this study, a three-dimensional “atomistic” circuit-device coupled simulation approach is advanced to investigate the process-variation and random dopant induced characteristic fluctuations in planar metal-oxide-semiconductor field-effect-transistor (MOSFET) static random access memory (SRAM) from 65-nm to 16-nm gate length. As the gate length of the planar MOSFETs scales from 65 nm to 16 nm, the SNM fluctuation increases from 4% to 27%. To reduce the device variability induced fluctuation in circuit, a 16-nm-gate silicon-on-insulator fin-type field-effect-transistor (FinFET) with aspect ratio (fin height / fin width) equal to two is investigated. Due to its superior electrostatic integrity and larger effective device width, the fluctuation of SNM of 16-nm-gate FinFET SRAM could be suppressed by five times. Comparing with the 65 nm planar MOSFET SRAM, FinFETs’ SRAM is promising in aggressively scaled silicon technology.

Keywords: static noise margin, static random access memory, metal-oxide-semiconductor field-effect-transistor, fin-type field-effect-transistor, random dopant fluctuation, process variation effect.

1 INTRODUCTION

As the dimension of complementary metal-oxide-semiconductor (CMOS) devices shrunk into sub-65nm scale, the threshold voltage ($V_{th}$) fluctuation is pronounced and become crucial for the design window, yield, noise margin, stability, and reliability of ultra large-scale integration circuits [1-5]. Various randomness effects resulting from the random nature of manufacturing process have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) devices and circuits. The fluctuation of short channel effect includes process-variation-induced gate length deviation and line edge roughness (PVE) are growing worse due to serious short-channel effect when the dimension of device is further scaled [6,7]. Besides the process variation induced threshold voltage fluctuation ($\sigma_{V_{th,PVE}}$), the double-digit channel dopants in scaled channel size make transistor behaviors more complicated to be characterized with conventional “continuum modeling” because every “discrete” dopant has its significant weight impacting the resulting transistor performance. The random nature of discrete dopant distribution results in significantly random fluctuations, such as the fluctuation of threshold voltage ($\sigma_{V_{th,RDF}}$). The random dopant fluctuation (RDF) is unpredictable and caused by random uncertainties in the fabrication process such as microscopic fluctuations in the number and location of dopant atoms in the channel region [5-11] and therefore is hard to be characterized. The intrinsic parameter fluctuations can limit the performance, yield and functionality due to significant component mismatch in area constrained circuits, such as static random access memory (SRAM), in which the stability of a SRAM cell is often related to the static noise margin (SNM) in the read operation [4], defined as the maximum DC noise voltage tolerance to avoid the cell state been flipped. Various approaches have been proposed to investigate the process-variation effect [6,7] and random dopant fluctuation [5-11], and the influence upon SNM performance [1-3]. However, the dependence of SNM and its fluctuation on transistor’s gate length is not clear yet. Thus, in this study, a three-dimensional “atomistic” circuit-device coupled simulation approach [5] is proposed to investigate the process-variation and random dopant induced characteristic fluctuations in planar MOSFET SRAM from 65-nm- to 16-nm-gate length. To reduce the device variability induced fluctuation of SRAM circuit; we replace conventional MOSFETs by silicon-on-insulator (SOI) fin-type field-effect-transistor (FinFET) with aspect ratio (fin height / fin width) equal to two. The characteristic of 16-nm-gate FinFET SRAM is then compared with 65 nm planar SRAM to show its promising characteristics.

This paper is organized as follows. In Sec. 2, we introduce the analyzing technique for studying the random dopants effect in nanoscale device and circuit. In Sec. 3, we examine the discrete-dopant- and process-variation-induced characteristic fluctuations of the investigated device and SRAM circuit. Both device and circuit level characteristic fluctuations are discussed. Finally, we draw conclusions and suggestion future work.

2 SIMULATION METHODOLOGY

The nominal channel doping concentrations are $1.48\times10^{19}$ cm$^{-3}$ and the $V_{th}$ are calibrated for 16 nm gate MOSFETs. For RDF, to consider the random fluctuation effect of the number and location of discrete channel dopants, 758 dopants are randomly generated in a large cube (80x80x80 nm$^3$), in which the equivalent doping concentration is $1.48\times10^{18}$ cm$^{-3}$, as shown in Fig. 1(a). The
Fig. 1. (a) Discrete dopants randomly distributed in the large cube with the average concentration of $1.48 \times 10^{18}$ cm$^{-3}$. There will be 758 dopants within the cube, for 16 nm gate devices, dopants may vary from 0 to 14 (average = 13), within its sub cubes of 16 nm$^3$. [(b), (c)]. Otherwise, dopants may vary from 70 to 130 (average = 100) for 65 nm gate devices. (d). The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET (e), and the same approach for SOI FinFET(f), and the illustration of a SRAM cell (g).

The large cube is then partitioned into 125 sub-cubes of $(16 \times 16 \times 16)$ nm$^3$. The number of dopants may vary from zero to 14, and the average number is 6, as shown in Figs. 1(b) and 1(c), respectively. Similarly, we can obtain the distribution of dopant number for the 65-nm-gate transistor, in which the dopant number may vary from 70 to 130 as shown in Fig. 1(d). These sub-cubes are equivalently mapped into the device channel for the 3D device simulation with discrete dopants, as shown in Fig. 1(e). The device simulation is performed by solving a set of 3D density-gradient equations coupling with Poisson equation as well as electron-hole current continuity equations [12, 13]. Figure 1(f) shows the studied SOI FinFET with aspect ratio equal to two. Without losing generality, the SOI FinFET is with 16-nm-gate and $1.48 \times 10^{18}$ cm$^{-3}$ equivalent channel doping concentration. The explored SRAM circuit is illustrated in Fig. 1(g). The voltage level of BL, BL’, WL and $V_{DD}$ will be charged to applied voltage to gather the static transfer characteristics, where the applied voltages of 16 nm and 65 nm devices are 1.0 and 1.2 Volt, respectively. The physical model and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [5-7, 10, 11]. Similarly, we can generate 125 discrete-dopant-fluctuated cases for PMOSFET through the flow of Figs. 1(a)-1(d). Then, 125 pairs of NMOSFETs and PMOSFETs are randomly selected and are used for the examination of circuit characteristics fluctuations. Furthermore, we apply the statistical approach to evaluate the effect of PVE, in which the magnitude of the gate length deviation and the line edge roughness follows the projections of the ITRS 2007 [14]. The 3σ for process variation induced gate length deviation and line edge roughness are 1.5nm and 4.3nm for the 16 nm and 65 nm devices, respectively. In estimating circuit characteristics, since there is no well-established compact model for such ultrasmall nanoscale devices, and for capturing the discrete-dopant-position-induced fluctuations, a device-circuit coupled simulation approach [5] is employed. The characteristics of devices of test circuit are first estimated by solving the device transport equations and using as initial guesses in the device-circuit coupled simulation. The circuit nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics [5].

3 RESULTS AND DISCUSSION

Figures 2(a) and 2(b) show the threshold voltage fluctuations for both the 16 and 65 nm gate n- and p-type planar MOSFETs. Based upon the independency of the fluctuation components, the total $V_{th}$ fluctuation is given by:

$$\sigma V_{th,total}^2 \approx (\sigma V_{th,RDF}^2) + (\sigma V_{th,PVE}^2)$$ (1)

In 16 nm MOSFETs, RDF induced 3.5 times larger $V_{th}$ fluctuation than PVE, and 5 times larger in 65 nm devices. $V_{th}$ fluctuation of 16 nm MOSFET is 4 times larger than that of 65 nm in total. Therefore, RDF dominates $V_{th}$ fluctuations in both 16 nm and 65 nm MOSFETs. We notice that in our simulation result, RDF induced $V_{th}$ fluctuations are 61 mV and 15.8 mV in 16 nm and 65 nm devices, respectively. That shows a good agreement to the analytical model of deviation of threshold voltage [9]. Figure 3 shows the static transfer characteristics of 65 nm planar SRAM cells include process variation and random dopant fluctuation, where the dashed lines represent RDF and PVE fluctuated cases, and the solid line stands for the nominal case. The nominal SNM for the 65 nm planar MOSFET SRAM is 138 mV. Since the random dopant fluctuation induces larger device variability in threshold voltage, the SNM fluctuation of SRAM is dominated by...
random doping effect. The RDF and PVE induced SNM fluctuations are summarized in inset of Fig. 3. The normalized static noise margin deviation induced by PVE and RDF are 2.38% and 4.3%, respectively. Through similar approach, we can obtain the SNM fluctuation for the 16 nm planar SRAM. The fluctuations is investigated and then summarized in Fig. 4, in which the RDF and PVE induce 27.2% and 7.4% variations of SNM. The SNM fluctuation induced by RDF is about five times larger than the PVE induced fluctuation. The result shows that the fluctuation of SRAM dependents on transistor’s gate size. Moreover, following the scaling rule of ITRS, the SNM of 16 nm planar MOSFET is under 60 mV according to our simulation result. The small SNM may make the function of SRAM failed. The shrinking of the device size can significantly increase the density of memory; however, the decreased SNM and increased SNM fluctuation are crucial issues and may limit the usage of such small device. There have been several approaches to increase the SNM, such as the use of larger $V_{DD}$ and cell ratio or we can increase the $V_{th}$ of transistor. However, these approaches may increase the layout area, consuming more power, or slow down the operation speed. The International Roadmap for Semiconductors has forecasted a transition from bulk devices to silicon-on-insulator devices, and then to multiple-gate SOIs as high-performance devices [14]. Therefore, to reduce device-variability-induced fluctuation

in device and circuit characteristics, 16-nm-gate SOI FinFETs with an aspect ratio of two is then adopted to replace the planar MOSFETs to examine associated fluctuation resistivity against RDF and PVE. RDF-and-PVE-induced threshold voltage fluctuation is summarized in the inset of Fig. 5. The threshold voltage fluctuation of 16-nm-gate NMOSFET is significantly reduced from 63.6 mV to 43 mV. The well control of device channel reduces both effects of RDF and PVE. Similarly, the random dopant fluctuation dominates the device characteristic fluctuations. Figure 6 shows the static transfer characteristics of 16 nm

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**Fig. 2** Threshold voltage fluctuation ($V_{th}$) for 16 nm and 65 nm gate n-(a) and p-type (b) planar MOSFETs.

**Fig. 3** Nominal and fluctuated static transfer characteristics of 65 nm planar SRAM cells.

**Fig. 4** Normalized PVE and RDF induced SNM variation for 16 nm planar SRAM.

**Fig. 5** Nominal and fluctuated static transfer characteristics of 16 nm SOI FinFET SRAM cells.
SOI FinFET SRAM cells, where the dashed lines illustrated RDF and PVE fluctuated cases, and the solid line is the nominal case. The nominal SNM is 125 mV. The normalized of RDF and PVE induced SNM fluctuation are investigated in Fig. 6. Comparing with 16 nm planar SRAM, the FinFET SRAM has five times smaller SNM fluctuation and provides sufficient SNM almost as large as that of 65 nm planar SRAM, which shows the promising characteristics in next generation nanoscale transistor. We notice the nominal threshold voltage of SOI FinFET is 140 mV, which shows the promising characteristics in read/write speed of SRAM.

4 CONCLUSION

In this study, a three-dimensional “atomistic” device-circuit coupled simulation approach has been proposed to investigate the random-dopant-induced characteristic fluctuations in nanoscale SRAM circuits, concurrently capturing the random discrete-dopant-number- and random discrete-dopant-position-induced fluctuations. Using the experimentally calibrated analyzing technique, the result shows that fluctuation of SRAM dependents on transistor’s gate size. The 16 nm planar SRAM has about 3 times larger fluctuation than 65 nm one and can not provide sufficient SNM to ensure stable operation. Though the decrease of transistor size can significantly increase the density of memory, the decreased SNM and increased SNM fluctuations of SRAM may limit the use of the smallest manufacturable device sizes in a given technology. To reduce the device variability induced fluctuation in circuit, 16-nm-gate SOI FinFETs is used to examine its capability in SRAM operation. The SNM fluctuation of 16-nm-gate FinFETs is five times smaller than that of 16 nm planar MOSFETs. Furthermore, 16-nm-gate FinFETs also provide sufficient SNM almost as large as that of 65 nm planar, which shows the promising characteristics in next generation nanoscale transistor. This study provides an insight into random-dopant-induced static transfer characteristic fluctuations. The experimental and theoretical verification will benefit the development of state-of-art static random access memories design with reliability.

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6 REFERENCES