

# Quantum Dot Gate InGaAs FETs

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## 1 ABSTRACT

This paper describes using wide energy gap lattice-matched II-VI layers, such as ZnSeTe-ZnMgSeTe, serving as a high-k gate dielectric for n-channel enhancement mode InGaAs field effect transistors (FETs). The thrust is to reduce interface states at the channel-gate insulator boundary while providing sufficient barrier height to confine the carriers in the channel created by inversion. In addition, this paper describes the role of various types of cladded quantum dots incorporated in the gate region to achieve either 3-state FET operation or nonvolatile memories. The fabrication methodology involves the growth of II-VI insulators using metalorganic chemical vapor deposition (MOCVD) and site-specific self assembly of GeO<sub>x</sub>-Ge and SiO<sub>x</sub>-Si cladded quantum dot forming the gate region.

**Keywords:** Cladded quantum dot gate FETs, InGaAs-FETs, lattice-matched gate insulator, II-VI gate insulator FETs, QD nonvolatile memory.

## 2 INTRODUCTION

Unlike Si FETs, InGaAs and other III-V field-effect devices result in performance which is less than desirable and commensurate to their anticipated potential. Recently, we have reported the fabrication of FETs using a variety of lattice-matched high-k semiconductors that serve as the gate insulator [1]. Self-assembly of cladded quantum dots, such as SiO<sub>x</sub>-cladded Si quantum dots, have been successfully used to fabricate floating gate nonvolatile memory [2] as well as 3-state (bistable) Si FETs [3].

This paper attempts to show the design and fabrication of InGaAs FETs that can potentially perform in a superior fashion by using wide energy gap lattice-matched gate insulators. The thrust is two-fold: (1) reducing interface states at the channel-gate insulator boundary to obtain superior control over variation in flat band or threshold voltage, and (2) providing sufficient barrier height to confine the carriers in the channel created by inversion. In addition, simulation is presented for InGaAs FETs using adequate layers of cladded quantum dots in the gate to implement a 3-state FET, which has been already demonstrated in Si.

Preliminary experimental results (e.g. capacitance-voltage characteristics showing inversion) are presented on QD gate and conventional MOS configured InGaAs devices.

## 3 DEVICE STRUCTURE

Figure 1 shows the cross-section of a typical InGaAs FET. The p-InGaAs layer is grown on lattice matched p-InP substrate. The n-type inversion layer is formed on the p-InGaAs surface adjacent to the ZnMgSeTe layer, which may be lattice-matched or pseudomorphic. The gate insulator layer is deposited by a thin layer consisting of cladded quantum dots (shown here as GeO<sub>x</sub>-cladded Ge dots). This structure can now be used in two configurations: (1) 3-state FET having two layers of oxide cladded dots (as shown), and (2) the layer comprising of cladded dots have another insulator (control) layer if the device is used as a nonvolatile memory. A variety of cladded dots including monodispersed SiO<sub>x</sub>-cladded Si dots as well as self-organized ZnMgTe dots on mismatched ZnS layers have been used [1, 2].

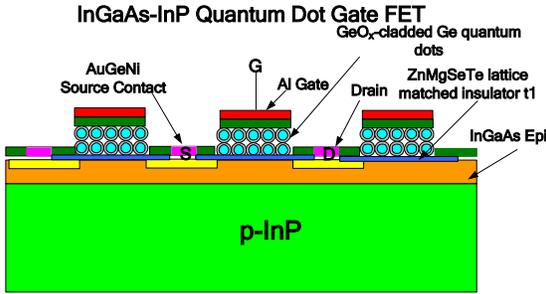


Fig. 1. Cross-sectional schematic of an InGaAs FET using II-VI lattice-matched gate insulator.

The oxide cladded Ge dot or  $\text{SiO}_x$ -cladded Si dots are self-assembled using the technique described elsewhere [2, 4]. The control gate insulator or cladded dots are contacted by a gate layer (e.g. metal aluminum in Fig. 1).

#### 4 SIMULATION OF 3-STATE QDOT GATE FETs

Figure 2 shows the energy band diagram of a 3-state FET (without control gate insulator) having two layers of  $\text{SiO}_x$ -Si cladded quantum dots.

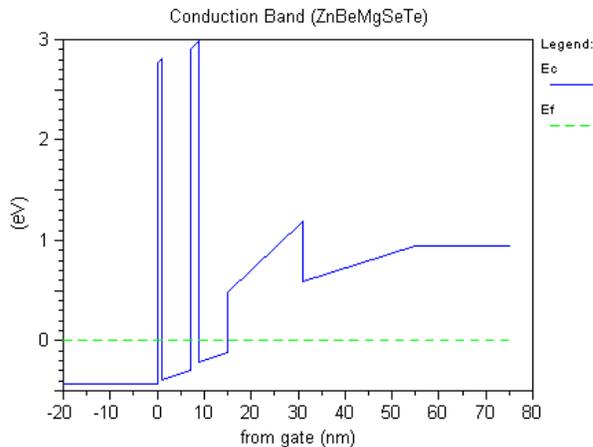


Fig. 2. QD ( $\text{SiO}_x$ -Si) gate with ZnMgSeTe on InGaAsP FET.

Figures 3a-c show the effect of gate insulator layer (II-VI) thickness  $t_1$  on the observation of manifestation of bistable (3-state) behavior. Three-state behavior results from the transfer of charge from the n-channel (inversion layer) to first and subsequently second layer of cladded quantum dots in the gate region. When the charge is located in either of these quantum dot layers, it modifies the threshold voltage. That is, as the gate voltage is increased, the threshold

voltage is also increased. This results in a state where drain current does not increase as the gate voltage is increased. This intermediate state “i” has been reported [1, 2].

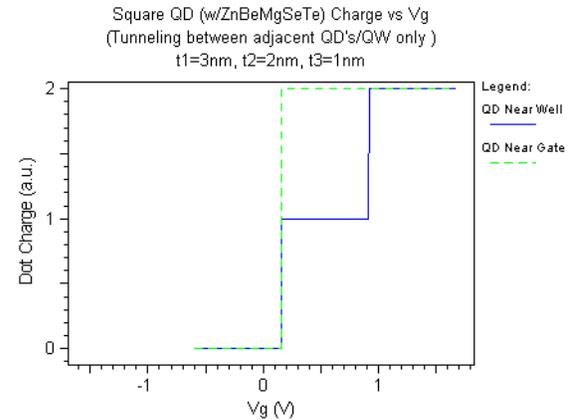


Fig. 3a. Variation in the charge on quantum dots in the gate region as a function of gate voltage  $V_g$ .

Figures 3b and 3c show the dot charge when the  $t_1$  thickness is increased to 8nm and 16nm, respectively. It is to be noted that the dot charge now has only one value. This is reflected in the bistable behavior recently reported in QD gate Si FETs having II-VI lattice-matched gate insulators [1]. In Fig. 3,  $t_2$  is the thickness of two cladding layers that separates two layers of cladded quantum dots. It is about 2nm. The outer cladding layer, adjacent to the gate, is referred by  $t_3$  (which is about 1nm).

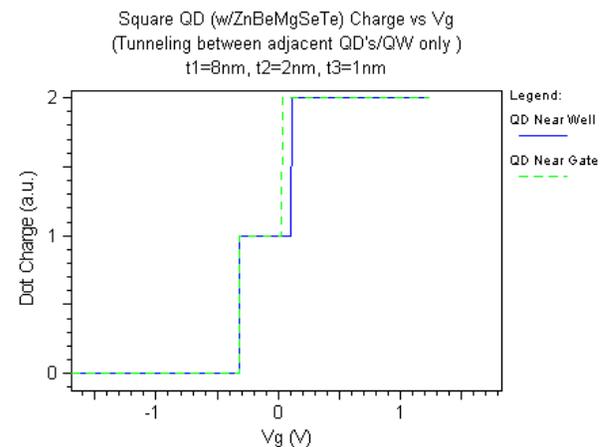


Fig. 3b. Reduction in the variation in the charge on quantum dots in the gate region as a function of gate voltage  $V_g$  when  $t_1$  thickness is raised to 8nm (from 3nm in Fig 3a).

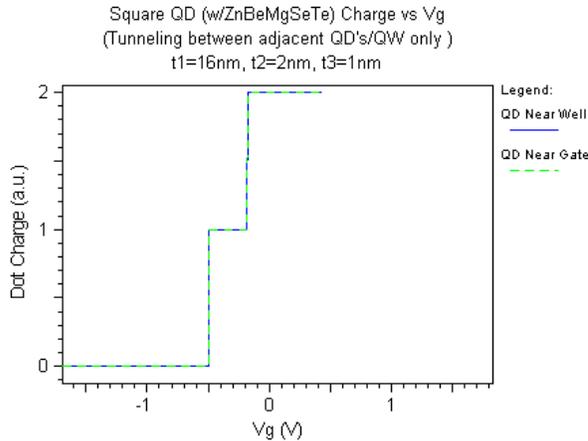


Fig. 3c. No variation in the charge on quantum dots as a function of gate voltage  $V_g$  when  $t_1$  thickness is raised to 16nm.

## 5 Experimental Results

Figure 4 shows the capacitance-voltage characteristics of an InGaAs device having lattice matched insulator.

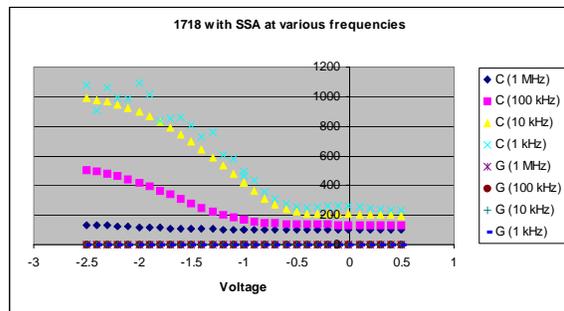


Fig. 4. QD-Gate InGaAs/InP MOS capacitor.

Figure 5 shows C-V characteristics of a MOS InGaAs device without cladded quantum dot gate. Note the variation in capacitance as a function of measurement frequency.

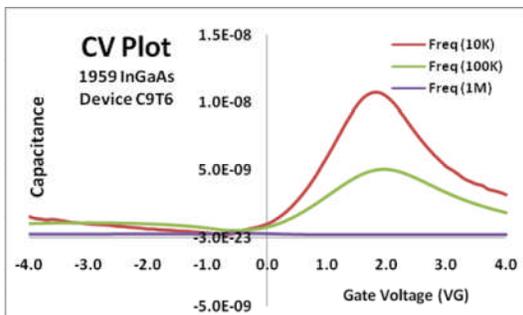


Fig. 5. C-V data for an InGaAs MOS device with II-VI variable band gap 3-layer insulator.

Here, we have used a stack of three layers to realize the gate insulator. They consist of a thin buffer layer (band gap  $E_{g1}$ ), a middle layer ( $E_{g2} > E_{g1}$ ) and a lattice-matched layer of ZnMgSeTe. These layers are approximately 600 angstroms in thickness. These layers are grown in a photo-irradiated MOCVD reactor similar to one described by Zhang *et al.* [5].

Recently, we reported observing FET characteristics [1] in InGaAs channels. However, we have not observed the 3-state behavior. The results are summarized below in Table I. The data shows that as the gate voltage is increased from -1.5 V to 0 Volts, the drain current  $I_D$  increases as a function of  $V_D$ . Thus, the gate influences the channel current. The relatively low value of drain current is attributed to significant source/drain resistances, which needs to be improved in future devices.

Table I. InGaAs FET characteristics.

Drain current $I_D$ (mA)	Drain Voltage $V_D$ (V)	Gate Voltage $V_G$ (V)
$2.33 \cdot 10^{-8}$	0.5	0
$1.55 \cdot 10^{-6}$	1	
$5.37 \cdot 10^{-6}$	1.5	
$1.91 \cdot 10^{-5}$	2	-0.5
$2.92 \cdot 10^{-8}$	0.5	
$1.36 \cdot 10^{-6}$	1	
$4.48 \cdot 10^{-6}$	1.5	-1.0
$1.64 \cdot 10^{-5}$	2	
$3.16 \cdot 10^{-8}$	0.5	
$9.02 \cdot 10^{-7}$	1	-1.5
$3.27 \cdot 10^{-6}$	1.5	
$1.100 \cdot 10^{-5}$	2	
$3.33 \cdot 10^{-8}$	0.5	-1.5
$5.26 \cdot 10^{-7}$	1	
$1.81 \cdot 10^{-6}$	1.5	
$8.23 \cdot 10^{-6}$	2	

## 6 CONCLUSION

Preliminary simulation of quantum dot gate 3-state FETs using InGaAs channel with lattice-matched II-VI gate insulators is presented. Capacitance-voltage characteristics of fabricated MOS configured devices, with and without quantum dot gate, show promise of high performance memory and FET devices. Work is in progress to improve the n-channel (Table I) InGaAs FET characteristics by the optimization

of the barrier height of the lattice-matched insulator and improving the source/drain regions and their Ohmic contacts.

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