Compact Model of Low-Frequency Noise in Nanoscale Metal-Oxide-Semiconductor Field Effect Transistors

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ABSTRACT

The future of mixed-signal, memory, and microprocessor technologies are dependent on ever increasing analog and digital integration, higher cell densities, and demand for more processing power. However, device variability creates challenges at each technology node which decreases yield, performance, and noise margins [1]. At these device dimensions the low-frequency noise (LFN) is dominated by the influence of one or more active traps capturing and emitting charge in the oxide creating wide variations in noise from otherwise identical devices. Additionally, the random position of dopant atoms near the Si/SiO₂ creates potential landscapes that induce regions of high and low conductivity and percolating current. The compact LFN model presented here accounts for the action of traps on percolating current in deep-submicron and sub-100nm MOS transistors.

Keywords: low-frequency, noise, rts, variation, model

1 INTRODUCTION

In today’s electronics there are sources of variability that impact performance, yield, and noise. LFN noise can vary over several orders of magnitude between otherwise “identical” devices, Fig. 1.

![Histogram of Drain Current Fluctuation](image)

**Figure 1: Power Spectral Density of 5 identical deep-submicron devices**

To date there is not a model available that adequately describes the effects of bias, device geometries, and processing on the LFN in MOSFETs.

Random Telegraph Signal (RTS) has been measured for some time and it is well accepted that the source of this noise signal in metal-oxide-semiconductor devices is due to the capture and emission of carriers at and near the oxide-semiconductor interface. In deep-submicron and nanoscale devices this source of noise is often dominant at low-frequencies (< 100kHz). The amplitudes of the fluctuations result in non-Gaussian distributions, see Fig. 2(a). A single RTS appears as a Lorentzian in the Power Spectral Density (PSD) plot, Fig. 2(b). For this model uncorrelated RTS is assumed. Individual PSDs will add causing additional bumps in the PSD plot, Fig. 3(b).
Second, there exists traps in the oxide capable of capturing and emitting charge, during capture the trapped charge is capable of reducing the conductivity of a localized region in the channel.

Finally, both the random potential and the effect of trapped charge have a dependence on the bias conditions and device fabrication which can be tailored to reduce the LFN.

Researchers have discovered that device biasing and processing does have a remarkable effect on the low-frequency noise in MOSFETs [2, 3]. This model described here can explain the noise reductions. In this model the biasing effects on the low-frequency noise is due to the change in trap time constants and the width of percolating currents.

2 NANOSCALE IMPERFECTIONS

Ionized dopant atoms near the surface and oxide charge create a random potential throughout the active region of a MOS device. These imperfections are a root cause of device variability and the high LFN observed in nanoscale devices. This effect occurs in both large and small devices, however, this effect is most prominent in deca-nanometer scale dimensions [1], and due to low oxide charge densities now common place, the randomness in the potential is primarily due to ionized dopant atoms [4].

2.1 Ionized Dopants

Ion-implantation is the standard means for controlled doping of well regions under the gate. These regions are for raising the background doping in epitaxial layers, punch-through suppression, and threshold adjustment. The dopant ions under the gate in general take substitutional positions in the lattice throughout the bulk. An increase in the doping, results in an increase in the threshold voltage.

The surface plot in Fig. 4 demonstrates a 3-D simulation of a random arrangement of dopant atoms near the Si/SiO₂ interface. This is the situation due to the presence of ionized dopant atoms due to an ion-implant.

2.2 Oxide traps

Any oxide will contain some number of traps which can become electrically active if the trap energy is within a kT of the quasi-Fermi level at the interface. At this energy separation mobile carriers in the channel can trap and be subsequently emitted with time constants based on the depth and energy of the trap. The amount of trapped charge and trap levels vary from one process to the next. There are interface traps and deeper oxide traps both of which become electrically active when the quasi-Fermi level approaches the trap energy or when the tunneling probability is appreciable enough for tunneling to the trap.
3 MODEL

Based on the previous discussion on the source of random potential the compact model is developed starting with the basic equation for a single RTS [5, 6]:

\[
S_I = 2(\Delta I_{DS})^2 \frac{\beta}{(1 + \beta)^2} \frac{1}{\omega_c} \frac{1}{1 + \frac{\omega^2}{\omega_c^2}}
\]

(1)

There are two variables in (1) that need to be addressed and will be considered separately. The first variable, \(\Delta I_{DS}\), is a measure of how effectively the trapped charge modulates the drain current. Secondly, the trap time constants consist of the ratio, \(\beta\), and the corner frequency, \(\omega_c\).

3.1 Drain Current Modulation

The drain current modulation term takes into account the existence of percolation currents and the geometrical positioning of the trap over the percolating current. In this model an ideal arrangement of dopant atoms is assumed as seen in Fig. 5.

The modulation of the drain current is given as:

\[
\Delta I_{DS} = \frac{I_{DS}}{N_{perc}} \eta
\]

\[
N_{perc} = \sqrt{N_DWLw_d}
\]

(2)

The \(\eta\) term captures the fractional change in the percolation current due to the effect of the coulomb blockade on the underlying channel filament and the bias conditions for gate/substrate image charge. \(N_{perc}\) is the average number of dopant atoms along the source within 1nm of the surface, \(w_d\).

From Fig. 6 the fractional change in the percolation current can be written as:

\[
\eta = \frac{2\alpha r_T}{w_{perc}}
\]

(3)

\(r_T\) is the effective trap radius, \(w_{perc}\) is the width of an individual percolation channel, and \(\alpha\) is how well the trap is centered over the percolation channel width. With \(\alpha = 1\) the situation is as seen in Fig. 6, and \(\alpha < 1\) is shown as the broken circle in Fig. 6.

![Figure 5: 3-D pictorial view of perfect dopant arrangement and percolation currents](image)

![Figure 6: 2-D schematic of single percolation path](image)

A basic equation for \(r_T\) is estimated by finding the distance where the interaction energy of the trapped charge is down to kT [7]:

\[
r_T = \frac{1}{4\pi kT} \frac{qQ_s}{2q^2} + \frac{1}{2\sqrt{2}\pi kT}
\]

(4)

At this point the field has virtually no effect on the channel carrier concentration. The first term in the denominator is the dielectric screening. The effect of carrier screening is brought into the picture as an additional term.
which effectively reduces the screening length as the channel carriers, $Q_s$, increases.

Briefly discussed next is the influence of the trap radius and the radius due to ionized acceptor atoms. Fig. 7 shows pictorially how the percolation widths are affected by the bias conditions. Increasing the gate voltage increases the channel carriers which screens the field due to the ionized acceptors, as seen from (4). On the other hand increasing the substrate bias shrinks the depletion region and the ionized dopants will have increased coupling to the edge of the depletion region reducing the effective radius at the interface and hence widening the percolation channels and reducing the effect of the trapped charge on the overall current flow.

$$\beta(V_{gs}) = \frac{\tau_c}{\tau_e} = e^{-1/kT} \left( K + q\psi_s + q \frac{2\pi}{T_{ox}} q(V_{gs} - V_{FB} - \psi_s) \right)$$

(6)

$K$ is a constant and the other terms retain the usual meaning. Equation (6) can be used to find the ratio factor, $\beta$, and the corner frequency, $\omega_c$, of the traps for use in (1).

## 5 SUMMARY

LFN has become an increasingly unavoidable problem as device dimension continue to decrease. Provided here is an alternative model for the estimation of LFN in nanoscale MOS devices. This model is intended to shed some additional light and give an alternative and hopefully more intuitive insight into how device dimensions, processing, and bias conditions can be effective in reducing LFN in nanoscale devices now and into the future.

## REFERENCES