Effective Width Modeling for Body-Contacted Devices in Silicon-On-Insulator Technology

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ABSTRACT

Effective width of a body-contacted MOSFET depends on the width offset, which comes from the specific layout one needs in Silicon-on-Insulator technology to contact the body node of these devices. This paper demonstrates and models the length dependence of the mentioned width-offset for 0.18 μm technology. The length dependence of width-offset is demonstrated by a simple technique of comparing linear currents of identical body-contacted and floating-body device for thick-oxide devices. Similar demonstration for thin-oxide devices is done by comparing maximum linear transconductance (peak g_m) of identical body contacted and floating body devices. This work then goes on to model this phenomenon semi-empirically. The improvement in the fits obtained with the proposed model over existing model validates it.

Keywords: SOI, width-offset, floating body, body-contact

1 INTRODUCTION

Silicon-on-insulator (SOI) technology has recently become a leading candidate for high performance VLSI applications which need increased circuit speeds [1]. The advantages come from the insulating layer which reduces parasitic source/drain-to-substrate junction capacitances, limits source/drain junction depths thus helps in making shallower junctions and also provides full device isolation [2]. But because of the presence of this insulating layer, the devices fabricated in SOI have body node as floating. These devices have been observed to have well-known kink effect [1]. This occurs due the the body node of the device is floating and it raises to a higher potential due to impact ionization [3]. This raised body potential reduces threshold voltage of the device and produces sudden rise in drain current, which is seen as kink [4]. This increase in the current is useful in increasing the speed in digital circuits [5]. But this effect is not desirable in many analog applications as it changes the gain of device suddenly and creates many problems [6]. To avoid this body-contacted (BC) devices are used in many analog applications.

The ways to get body-contact in SOI currently in literature are described in [7]. Because of this specific body-contact layout of the device, these devices have additional width offset. This width offset is modeled using non-binable *dwbc* parameter in standard BSIM-SOI4 [8]. This paper demonstrates that the parameter *dwbc* has length dependence. The length dependence is demonstrated using measurement data on NFET and PFET for thick and thin-oxide devices. The convention followed in the paper for the two types of devices is that for thin-oxide FET it will be explicitly said, else consider it to be thick-oxide device. After demonstrating mentioned length dependence from data, semi-empirical model to fit this length dependence is described. This is then followed by the comparison between fits obtained with and without proposed model.

2 WIDTH OFFSET IN BC DEVICES

In SOI if connection to body node is desired then specific layout needs to be made for the device. There are different type of layouts used for connecting body node [7]. Two of such ways to connect the body node are shown in Fig.1. The first one shown is T-type where body is contacted only from one side. The second one shown is H- type where body is contacted from two sides. Clearly H-type layout gives better body-contact because of lower body resistance. These two configurations are used in state-of-art SOI technologies for body connection.

The specific layout for the BC devices in SOI gives rise to extra currents flowing. This happens because the poly-silicon is needed to be put to provide isolation to connect the body (see Fig.1) , and that causes area under that extra poly-silicon to behave as MOSFET and extra current flows through it. This current is shown schematically in Fig.1. The way this extra current is modeled in BSIMSOI4.0 is through "Width offset for body contact Isolation edge" (*dwbc*) parameter. In model this parameter is added to the effective width of the device, the increase in effective width then models the extra current. But in BSIMSOI4.0 *dwbc* is parameter independent of channel length, which this paper demonstrates to be otherwise.

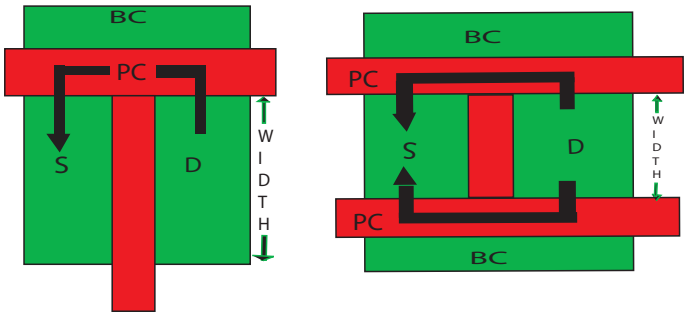

Figure 1: T-type and H-type layouts for body-contacted devices in SOI. Arrows show extra current due to specific layout. S and D are source and drain of device respectively. BC refers to the region from which body-contact will be taken. PC is poly-silicon gate

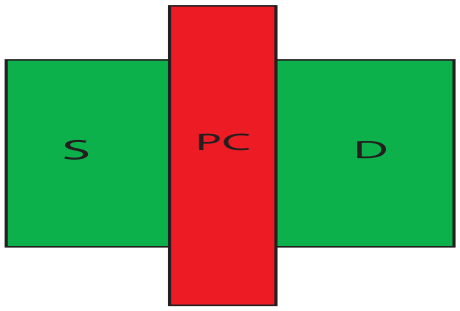

Figure 2: Layout of FB device in SOI. S and D are source and drain of device respectively. Note that there is no BC region as this is FB device. PC is poly-silicon gate

3 WIDTH OFFSET MODELING

As described earlier *dwbc* is independent of channel length in standard BSIMSOI4.0. While doing extraction for BC and floating body (FB) devices of different channel lengths, we found it difficult to fit them all with constant *dwbc*. To analyze this in detail we used a simple technique of comparing currents of identical BC and FB device. We took exactly same dimension FB and BC device and compared the currents of these two devices. From the layout of a floating body device as shown in Fig. 2, it is apparent that it does not have any width offset. If linear currents of these two devices are compared the difference is expected only to come from the width offset in BC device. We compare only linear current as in saturation or higher drain biases the FB device may have floating body effects [9], which will make these two identical devices not comparable.

The comparison of linear currents is then used to extract *dwbc* parameter for different geometry devices. Extraction of *dwbc* by comparing linear currents of identical BC and FB devices was done using Eq. 5, the derivation of which is through Eq. 1 to Eq. 4.

$$\frac{I_{BC}}{I_{FB}} = \frac{W_{BC}}{W_{FB}} \tag{1}$$

where I_{BC} is linear current of BC device of particular geometry,I_{FB} is FB device linear current of same geometry. W_{BC} and W_{BC} are total widths of BC and FB device respectively.

$$W_{BC} = W_{eff} + dwbc \tag{2}$$

$$W_{FB} = W_{eff} \tag{3}$$

So,

$$\frac{I_{BC}}{I_{FB}} = 1 + \frac{dwbc}{W_{eff}} \tag{4}$$

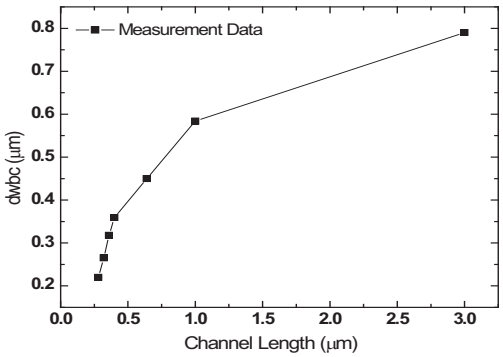

Figure 3: Variation of width offset parameter with channel length

And,

$$dwbc = W_{eff}\frac{I_{BC}}{I_{FB}} - W_{eff} \tag{5}$$

The result of extracting *dwbc* for NFETs for seven different channel length devices is shown in Fig.3. From Fig. 3 it is apparent that *dwbc* increases with length of the device and then saturates. This can be explained from the layout (Fig. 1). As the channel length increases the field lines from drain to source for extra current increases, this causes width offset to increase. As these field lines increase further more, they approach physical limit from edge of the extra poly-silicon. The field lines can not extend beyond poly-silicon edge, which causes them to saturate and not increase further. Similar variation in *dwbc* for PFETs was also observed. These observations from the *dwbc* behavior with length are semi-empirically modeled.

The equation used to model this *dwbc* variation with L is,

$$dwbc = dwbc_0 - \frac{dwbc_l}{L} \tag{6}$$

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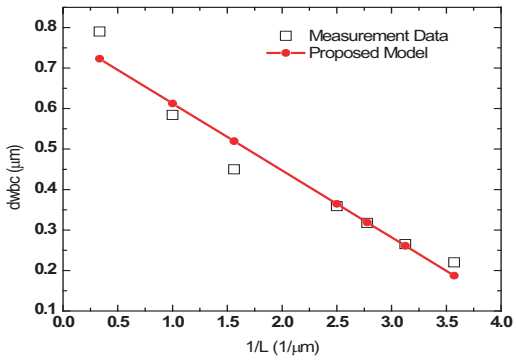

Figure 4: *dwbc* Vs $1/L$ fit obtained with proposed model for NFET

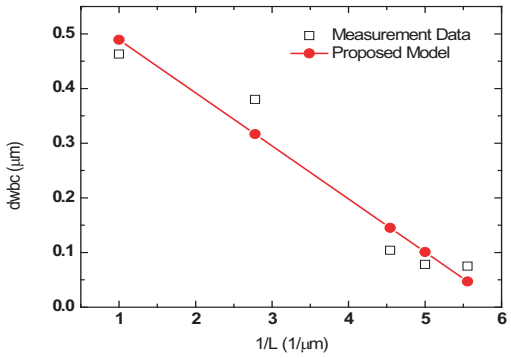

Figure 5: *dwbc* Vs $1/L$ fit obtained with proposed model for thin gate-oxide NFETs

where $dwbc_0$ and $dwbc_l$ are parameters which can be extracted from *dwbc* Vs L data to obtain best fit. From this equation its clear that as L increases *dwbc* will increase as observed. Also it will tend to saturate as length increases, the way we see in the data. The fit obtained for NFET is shown in Fig. 4. In Fig. 4 we have plotted *dwbc* Vs $1/L$ which is a straight line from Eq. 6. Similar fits were obtained for PFETs also. Apparent from the figure Fig. 4 , that Eq. 6 models the phenomenon reasonably well.

All of the above analysis was carried out on the devices with very thick gate-oxide, where gate-leakage was negligible. In this work we also included devices with thin gate-oxide where threshold voltage of BC and FB devices even in linear conditions are not equal. This is because gate-leakage causes body potential of FB devices to rise [10], changing the threshold voltage. To carry similar analysis for these devices peak linear *gm* (trans-conductance) was used. So in place of linear currents in Eq. 7, we have peak g_m as,

$$\frac{gm_{peak,BC}}{gm_{peak,FB}} = \frac{W_{BC}}{W_{FB}} \tag{7}$$

where, $gm_{peak,BC}$ and $gm_{peak,FB}$ are peak of linear trans-conductances of BC and FB devices respectively. Using gm_{peak} threshold mis-match between FB and BC devices was overcome and same analysis was carried out. As explained earlier $dwbc_0$ and $dwbc_l$ were extracted. The fit obtained for thin oxide NFET is shown in Fig. 5. Similar fits were obtaines for thin-oxide PFETs also. The reasonable fits in all the cases validated that Eq. 6 models the length dependence well.

4 RESULTS AND DISCUSSIONS

In this section comparison between fits obtained with and without using proposed model is presented. The model proposed (Eq. 6) has length dependence. So, the most interesting plot will be to see the improvement obtained in I_{dlin} ($V_{drain} = 0.05V$) fits with this model. This comparison when drawn for NFETs looks like Fig. 6 for $W = 3\mu$m device. It is apparent from figure that proposed model improves the fits substantially.

To further emphasize one more interesting plot will be of error. So, we computed error η which is given by Eq. 8. Fig 7 shows the error variation with channel length with and without proposed model. It is apparent from figure that error with proposed model is considerably less. Moreover from the error plot without proposed model its quite clear that it increases with channel length and then saturates, the exact behavior which proposed model for *dwbc* variation with channel length captures.

$$\eta = \frac{I_{data} - I_{model}}{I_{data}} \tag{8}$$

The comparison of $Idlin$ Vs L for thin oxide devices was also carries out. Fig. 8 shows the results obtained. This also shows that there is clear improvement we obtain when using proposed model. Similar results were obtained for PFETs also for both the flavors of the devices.

In this paper the *dwbc* parameter extraction and all fitting results are shown for H-type body-contact. But as explained earlier in this paper T-type body-contact also has same phenomenon. So this model is easily extendable to the T-type body-contacted devices also. Authors think that with same formulations and change in $dwbc_0$ and $dwbc_l$ parameters it should be possible to model T-type body-contacted device width offset also.

5 CONCLUSION

The conclusion from the analysis done in this paper is that the extra current in BC devices in SOI technologies, which comes because of specific layout is length dependent. This is seen for state-of-the-art H-type layout structure. BSIMSOI4 parameter *dwbc* which models

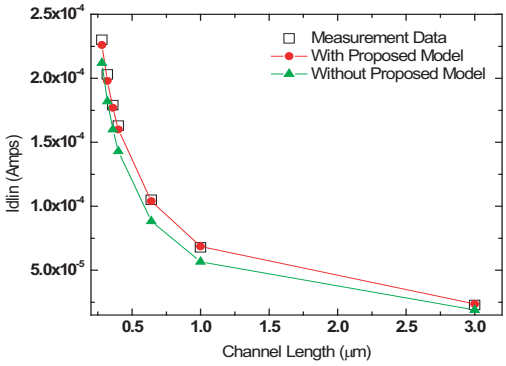

Figure 6: I_{dlin} Vs L fit obtained with and without proposed model for NFET

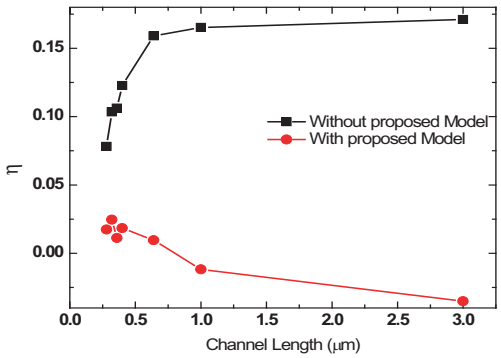

Figure 7: η Vs L with and without proposed model for NFET

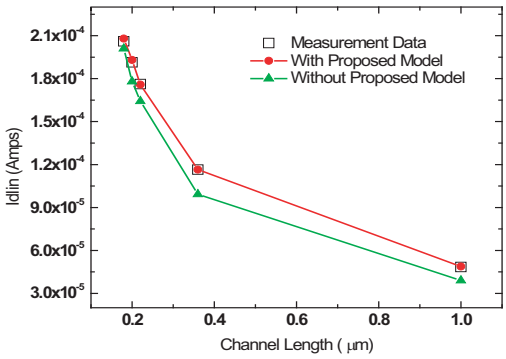

Figure 8: I_{dlin} Vs L fit obtained with and without proposed model for thin gate-oxide NFET

this effect hence has to be length dependent. The length dependence for *dwbc* proposed in this paper seems to capture the phenomenon reasonably well and improves the quality of the fits. These improved fits will help in improving the quality of all RF-SOI circuits' simulation where body-contacted devices are used.

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