Increased Piezoresistive Effect in Crystalline and Polycrystalline Si Nanowires

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ABSTRACT

Recently, a giant piezoresistance effect has been observed in bottom-up fabricated silicon nanowires [1]. Here we present the results of piezoresistive measurements on boron doped crystalline silicon nanowires at two different doping levels, as well as polycrystalline boron doped silicon nanowires, fabricated using a traditional top-down approach compatible with industrial mass-production techniques. In crystalline silicon nanowires, at a doping level of 10^{17} cm^{-3}, we find an increase in the piezoresistive effect of up to 633% that of bulk silicon. While at a doping level of 10^{20} cm^{-3}, we find a constant or decreasing piezoresistive response, relative to bulk measurements. In polysilicon nanowires we find an increase in the piezoresistive response of up to 39% that of bulk polysilicon. Finally, an increase in the temperature sensitivity is observed in low doped crystalline silicon nanowires.

Keywords: piezoresistivity, silicon nanowires, top-down

1 INTRODUCTION

The piezoresistive effect is much larger in silicon than in most other materials, and silicon piezoresistors have therefore been used for force sensing in several MEMS devices in the past three decades [2, 3]. While there has been a large interest in the temperature and doping dependence of the piezoresistive effect, the dimensional dependency has not been investigated until recently. In self-assembled silicon nanowires, a piezocoefficient of up to $\pi_{[111]} = 3550 \cdot 10^{-11}$ Pa^{-1} has been measured [1]. A large number of micro and nano sensors can thus be greatly improved if such highly piezoresistive silicon nanowires can be integrated with conventional mass-produced sensor designs. Self-assembly of silicon nanowires is still a relatively new fabrication method, and is not yet fully compatible with standard top-down micro- and nanoscale fabrication technologies. Furthermore, self-assembly has several disadvantages including the tendency to prefer growth along specific crystal directions, as well as the difficulty of positioning the catalyst particle and creating electrical contact to the nanowire, e.g. for four-point measurements. While top-down fabrication of silicon nanowires can not be achieved using standard MEMS fabrication methods, such as UV lithography (UVL), one can easily reach the sub-100 nm range using technologies such as e-beam lithography (EBL), nano imprint lithography (NIL) and oxidation thinning. Top-down fabricated highly piezoresistive silicon nanowires thus show great promise of a new generation of highly sensitive piezoresistive sensors.

2 DESIGN

In order to measure the piezoresistive effect in silicon nanowires, a test chip has been designed. The chip is 4 cm long, 5.3 mm wide and approximately 350 μm thick. Each test chip carries 6 dielectrically isolated p-type piezoresistors, as seen in Figure 1. The piezoresistors are located at the center of the chip and oriented along the chip, i.e. in the [110]-direction. Using a four-point bending (4PB) fixture for bending the chip will thus cause a uniaxial stress in the piezoresistors along the length direction. The 6 piezoresistors includes 50, 100, 150, 250, 350 nm wide nanowires as well as a 25 μm wide bulk type reference piezoresistor. All piezoresistors have a width:length ratio of 1:20. This design gives a single chip analysis of the dimension dependence of the piezoresistive effect. The contact surface between the nanowires and the electrical contacts will usually be very small, and contact resistances can therefore be large compared to the resistance of the nanowires. To minimize voltage drops due to contact resistances each piezoresistor is fabricated with integrated four-point probes, see Figure 2. It is known from bulk measurements, that the largest piezocoefficient in p-type silicon is π_{44}. If an uniaxial stress is applied in the [110]-direction, the effective piezocoefficient of the piezoresistors is

$$\pi_{\text{eff}} = \frac{1}{2}(\pi_{11} + \pi_{12} + \pi_{44}) \approx \frac{1}{2}\pi_{44} \quad (1)$$

3 FABRICATION

The main fabrication steps are illustrated in Figure 3. Crystalline (100)-oriented SOI wafers with a device layer of 340 nm are implanted with boron to a final concentration of either 10^{17} cm^{-3} or 10^{20} cm^{-3}. The polycrystalline device layers are deposited using LPCVD at 620 °C and in-situ doped. Macroscale structures, such

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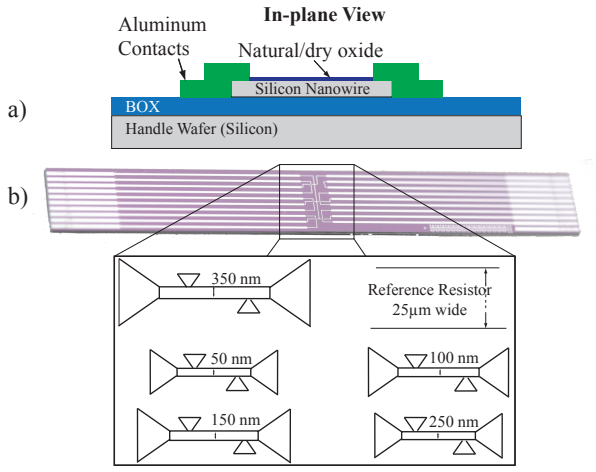

Figure 1: (a) The piezoresistors are lying on top of the buried oxide and thus dielectrically isolated. (b) The test chip consists of 6 piezoresistors of which five are nanowires of different dimensions and one is a 25 μm wide reference resistor. The length to width ratio of the piezoresistors is 20. The illustration is not to scale.

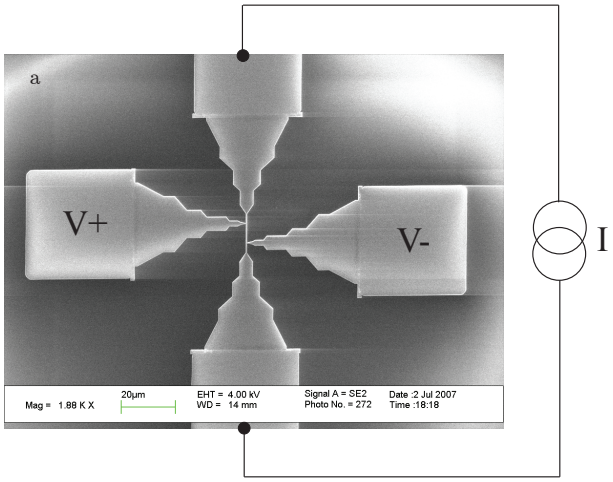

Figure 2: SEM image of a silicon nanowire with integrated four-point probe lying on SiO_2. A constant current is applied using the upper and lower contacts, and the resistance of the nanowire is then found by measuring the resulting voltage drop.

as contacts and test structures are made by standard UVL and transferred to a gold mask by liftoff. Nanowires and four-point probes are made by EBL (JEOL JBX9300FS) in the positive resist ZEP520A and likewise transferred to the gold mask. Using a reactive ion etch (RIE) the structures are defined in the silicon device layer. The gold mask is removed using potassium iodide, and aluminum wires for electrical contact are made by e-beam evaporation.

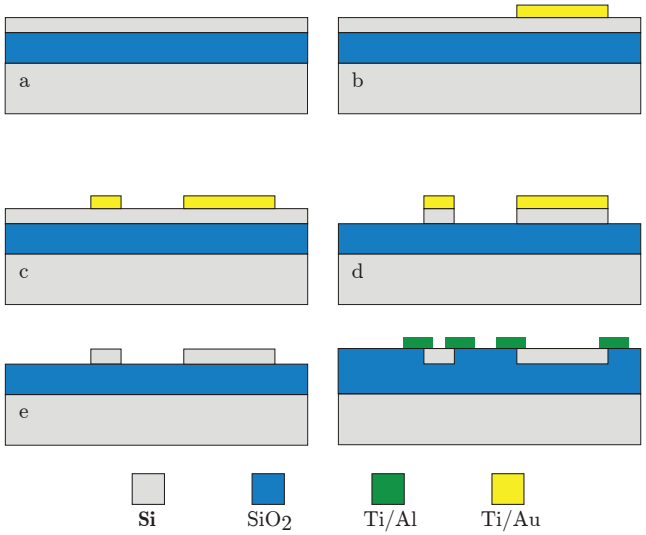

Figure 3: (a) A SOI wafer with crystalline or polycrystalline device layer is implanted with boron. (b) Macroscopic structures are made in 60 nm thick gold by UVL and liftoff. (c) Nanoscopic structures are made in 60 nm thick gold by EBL and liftoff. (d) The gold structures are used as masking in a RIE, thereby defining the structures in the device layer. (e) The gold mask is removed in potassium iodide. (f) Electrical contacts to the piezoresistors are made by e-beam evaporation of aluminum.

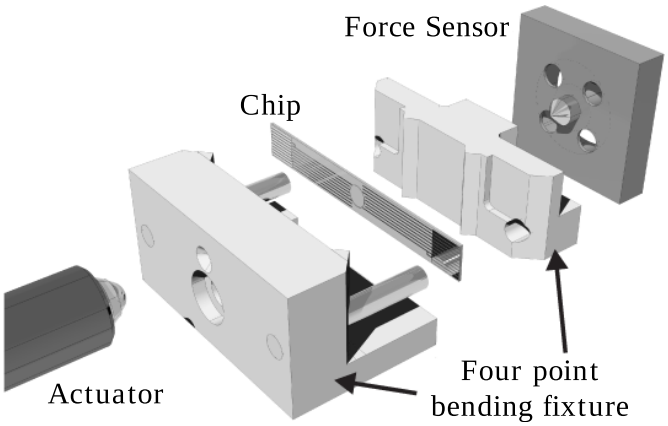

Figure 4: A four-point bending fixture is used to apply an uniaxial stress in the center of the test chip, where the piezoresistors are located. The two parts of the fixture are forced together using a microstep actuator, and the resulting force is measured using a force sensor.

4 EXPERIMENTAL SETUP

The stress dependence of the resistance in the piezoresistors, i.e. the piezoresistive effect, is measured using a four-point bending (4PB) fixture, see Figure 4. The test chip is placed between the two pair of blades, which are then forced together using a microstep actuator. The

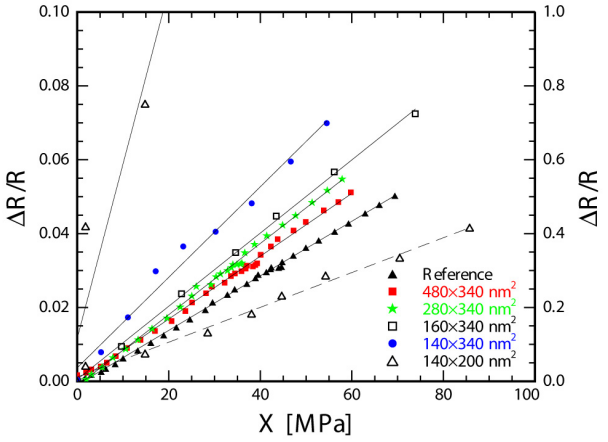

Figure 5: The relative change in resistance for five different dimensioned crystalline silicon nanowires as function of compressive stress. All data except the one fitted by the dashed line are plotted on the left hand side axis.

resulting force on the test chip is measured using a conventional force sensor. Assuming the test chips behaves as a beam subjected to pure bending, the stress in the test chip at the location of the piezoresistors, X, is calculated from the measured force, F, as

$$X = -\frac{6 \cdot F \cdot a \cdot z}{w \cdot t^3}, \tag{2}$$

where a is the distance between the inner and outer blades of the 4PB fixture, z is the distance from the surface of the test chip to the neutral plane (i.e. half the thickness of the test chip), w is the width of the test chip and t is the thickness of the test chip.

The 4PB fixture is situated in an aluminum box with built-in resistive heating and Peltier cooling. Current is applied to the piezoresistors using a HP4145A parameter analyzer, and the resulting voltage drop is measured using a Keithley 2182A nanovoltmeter. Electrical contact to the test chip is obtained using zero insertion force flat flexible cable (FFC) connectors.

5 Results

The relative change in resistance as function of compressive stress for crystalline silicon nanowires at a boron concentration of 10^{17} cm^{-3} is seen in Figure 5. It is observed that the relative change increases as dimensions are reduced. Using the approximation in Equation 1, the π_{44} coefficient for these nanowires has been listed in Table 1. Considering the relatively large dimensions of the nanowires, the increased piezoresistive effect can not be contributed to quantum effects. However, the increase in the number of surface states compared to the number of carriers as dimensions are decreased, might explain the observed increase piezoresistive effect.

Table 1: Approximations of π_{44} for different sized crystalline silicon nanowires at a boron concentration of 10^{17} cm^{-3}.

Dimensions	ρ [Ω·cm]	π_{44} [Pa^{-1}]	$\Delta\pi_{44}/\pi_{44,ref}$
Reference	0.17	$124 \cdot 10^{-11}$	-
480×340 nm^2	0.17	$140 \cdot 10^{-11}$	13%
280×340 nm^2	0.17	$165 \cdot 10^{-11}$	33%
160×340 nm^2	0.12	$198 \cdot 10^{-11}$	60%
140×340 nm^2	0.17	$245 \cdot 10^{-11}$	98%
140×200 nm^2	0.09	$910 \cdot 10^{-11}$	633%
Smith [2]	7.8	$138 \cdot 10^{-11}$	11%
Tufte et al. [3]	0.02	$113 \cdot 10^{-11}$	-9%

The relative change in π_{44} for crystalline silicon nanowires at a boron concentration of 10^{20} cm^{-3} as function of nanowire width is seen in Figure 6. At widths down to 150 nm, the piezoresistive effect remains approximately constant. At widths below 150 nm the piezoresistive effect decreases rapidly approaching zero at 50 nm. This rapid decrease can be contributed to an increase in the resistance of the nanowires due to surface scattering. Assuming the mean free path is generally smaller than the dimensions of the nanowire, the conduction through the nanowire will be dominated by bulk-like conductance. At the surface regions, however, the conductance is reduced due to an extra surface scattering term. Due to the lowered conductance, the change in resistance due to the piezoresistive effect is vanishing in the surface regions. When the width of the nanowire is comparable to the width of the surface scattering dominated regions, the piezoresistive response will decrease rapidly, and approach zero as surface scattering becomes dominant. Based on these assumptions the effective piezocoefficient can be found as

$$\pi_{eff} \approx \frac{G_{bulk}}{G_{bulk} + G_{surface}} \pi_{bulk}, \tag{3}$$

where G is the conductance. Using this equation and the theory of Richardson and Nori [4], the obtained data has been fitted as seen in Figure 6. Deviations from the fit are primarily contributed to variations in surface roughness and uncertainties in the nanowire dimensions.

The relative change in resistance for boron doped polycrystalline silicon nanowires under compressive stress is seen in Figure 7. Again the piezoresistive effect increases as dimensions are decreased, with a maximum increase of 39% compared to the reference resistor. Assuming that it is changes in the number of surface states that is responsible for the increased piezoresistive effect, it is not expected that the increase in the piezoresistve effect will be as large in the polysilicon nanowires as in the low doped crystalline silicon nanowires, since the polysilicon nanowires already have a large number of surface states at the grain boundaries.

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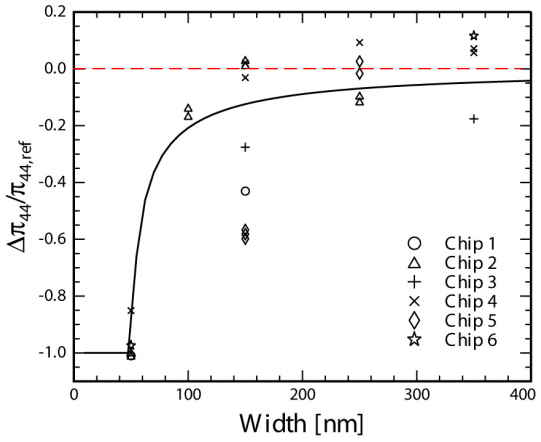

Figure 6: The piezoresistive effect in top-down fabricated high doped crystalline silicon nanowires decreases as the widths are reduced. The thickness of all piezoresistors is 340 nm. The fit is based on the assumption that the decrease is due to surface scattering.

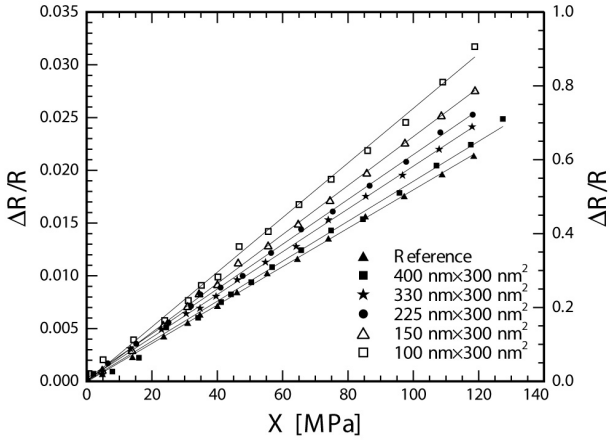

Figure 7: As for low doped crystalline silicon nanowires, an increase in the piezoresistive effect is observed in polysilicon nanowires, as dimensions are decreased. Compared to the reference resistor an increase of up to 39% is measured.

Measurements of the temperature dependence of the piezoresistive effect in the low doped crystalline silicon nanowires are shown in Figure 8. As expected from theory and bulk measurements [5], the piezoresistive effect shows a $1/T$ dependence. However, it is also noted that the temperature sensitivity of the piezoresistive effect increases as dimensions are decreased. Comparing the smallest nanowire with the reference, one finds an approximately 4 times larger temperature sensitivity. It is thus critical that piezoresistive silicon nanowire sensors incorporate temperature compensation.

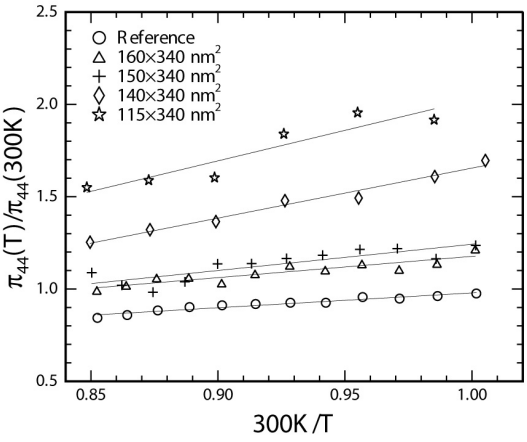

Figure 8: The π_{44} piezocoefficient for low doped crystalline silicon nanowires normalized with respect to the results of Smith [2], as function of inverse temperature.

6 Conclusion

Crystalline and polycrystalline p-type silicon nanowires have been fabricated using a top-down approach. In low doped crystalline silicon nanowires an increased of up to 633% that of the bulk reference resistor was found. This increase is contributed to an increase in the surface states to carrier ratio. In highly doped crystalline silicon nanowires the piezoresistive effect is approximately constant down to widths of 150 nm, whereafter it decreases rapidly due to surface scattering. In polysilicon nanowires an increase of up to 39% were found as dimensions were decreased. The temperature sensitivity of the piezoresistive effect has been found to increase in low doped crystalline silicon nanowires as dimensions are reduced.

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