Construction of a Compact Modeling Platform and Its Application to the Development of Multi-Gate MOSFET Models for Circuit Simulation

M. Miura-Mattausch, M. Chan[*], J. He[**], H. Koike[***], H. J. Mattausch
T. Nakagawa[***], Y. J. Park[+], T. Tsutsumi[++] and Z. Yu[+++]

Graduate School of Advanced Sciences of Matter, Hiroshima University
Higashi-Hiroshima, Hiroshima, 739-8530, Japan, mmm@hiroshima-u.ac.jp, hjm@hiroshima-u.ac.jp
[*]Department of Electronic and Computer Engineering, Hong Kong University of Science & Technology, Hong Kong, mchan@ee.ust.hk
[**]School of computer & Information Engineering, Shenzhen Graduate School, Peking University Shenzhen, 518055, P. R. China, frankhe@pku.edu.cn
[***]Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology, Tsukuba, Ibaraki, 305-8568 Japan, h.koike@aist.go.jp, nakagawa.tadashi@aist.go.jp
[+]School of Electrical Engineering and Computer Science and NSI-NCRC, Seoul National University Seoul, Korea, ypark@snu.ac.kr
[++]Department of Computer Science, School of Science and Technology, Meiji University Kawasaki, 214-8571, Japan, tsutsumi@cs.meiji.ac.jp
[+++]Institute of Microelectronics, Tsinghua University, Beijing 100084, China, yuzhip@tsinghua.edu.cn

ABSTRACT

We aim at constructing a common platform for compact model development based on the Verilog-A language for collaboration among different research groups. The project aims in particular at a framework for efficient development of multi-gate MOSFET models for circuit simulation. We have developed several prototypes of multi-gate MOSFET models based on different concepts till now. Phenomena expected to become important for the multi-gate MOSFET generation are modeled on the basis of their physical origins. These phenomena are implemented into each of the specific multi-gate MOSFET models by plugging in modules from the common platform. Parasitic resistive and capacitive contributions are also modularized to represent the complete circuit performance of the multi-gate MOSFET device for efficient circuit development.

Keywords: common platform, quantum effect, multi-gate MOSFET, circuit simulation, parasitic effect

1 INTODUCTION

Many different kinds of basic devices have been developed with different kinds of fabrication technologies for the application in integrated circuits. To efficiently utilize these devices for a specific integrated circuit design, accurate compact models of these devices have to be developed. It is furthermore desired to predict resulting circuit performances at an early stage ideally in parallel to the device-technology development. To realize the necessary rapid compact model development, the availability of a modular compact-modeling platform will be very useful.

We have started the project called Nano Device Modeling Initiative (NDMI) in 2005 October as a collaborative effort among different research groups from different countries.

Subjects being investigated are summarized in Table 1. One of our important aims is to construct a platform for rapid compact model development by providing a prototype consisting of modules for different model functions, which are individual elements calculating different device features, as schematically shown in Fig. 1. This platform will enable the plugging in of developed modules for compact model parts by substituting modules of the prototype or by adding new modules We take the advanced MOSFET model HiSIM [1] as the prototype model for modularization.

The multi-gate MOSFET has been considered as a possible candidate for the next generation device below the 45nm technology node. Phenomena expected to become obvious in this device are investigated based on device physics. Modeling of the multi-gate MOSFETs has been performed in the NDMI project based on different concepts. The SOI-MOSFET modeling has been also investigated as a foregoing study.

Subject	Purpose
1	Common Platform Development
2	Model Development for Microscopic Phenomena
3	Model Development for SOI-MOSFET
4	Model Development for MG-MOSFET

Table1. Subjects aimed at in the NDMI project.

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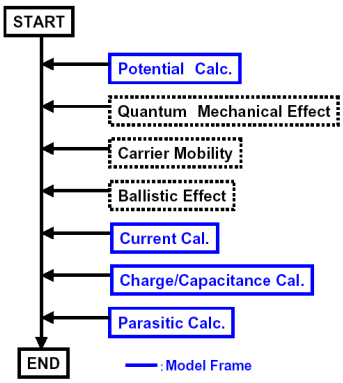

Fig. 1. Schematic representation of the concept for the compact-modeling framework, providing modules of individual functions of the complete compact model.

2 OVERVIEW OF RESULTS OBTAINED

2.1 Modeling of Quantum Phenomena

It is expected that the quantum mechanical effects cannot be ignored for sub-50nm technologies and beyond. The most important quantum effect is observed in the quantized carrier distribution at different energy states as schematically shown in Fig. 2.

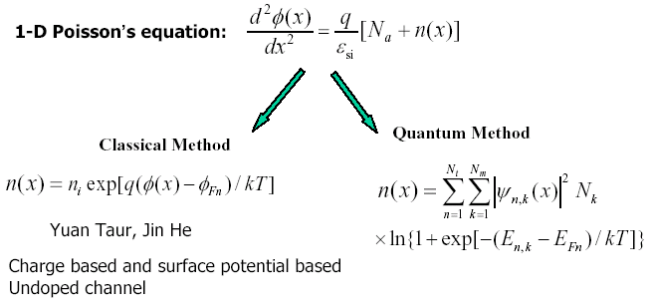

Fig. 2 Illustration of the conceptual differences between the classical and quantum mechanical solution of the Poisson equation.

Figure 3 compares results with developed quantum model for the inversion charge, the Baccarani results, and the Schred results, by solving the Poisson equation and the Schrödinger equation simultaneously [2].

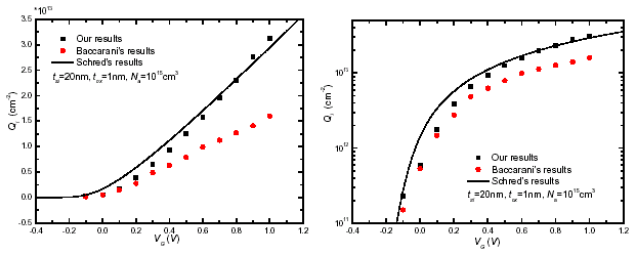

Fig. 3. Calculated inversion charge with the quantum method in comparison to other existing results.

Surface potentials are calculated in our approach by solving the basic device equations with the quantized charge, which, in the conventional planar case, leads to [3]

$$C_{ox}\left(V_{gs}-V_{FB}-\phi_s\right)=Q_n+Q_b \tag{1}$$

$$Q_n=q\sum_i\sum_{j=1}^{3}\frac{m_{xy}^i}{\pi\hbar^2}k_BT\log\left(\exp\left(\frac{E_f-E_j^i}{k_BT}\right)+1\right) \tag{2}$$

where i denotes the valley's index, $m_{xy}=\sqrt{m_xm_y}$ is the two-dimensional DOS effective mass, while the z-axis is directed to the oxide interface, j is the sub-band index, E_f and E_j are the Fermi level and quantization energy levels in the channel, respectively.

The energy spectrum in the conventional planar structure can be calculated with the triangular potential approximation, where the effective field is determined as

$$E_{eff}=\frac{\alpha Q_n+Q_b}{\varepsilon_{Si}}=\alpha C_{ox}\frac{V_{gs}-V_{FB}-\phi_s}{\varepsilon_{Si}}+\frac{1-\alpha}{\varepsilon_{Si}}Q_b(\phi_s) \tag{3}$$

where α is the fitting parameter, which is equal to 0.5 as a nominal value. Then the sub-bands in conventional MOSFET are determined as

$$E_{SG,j}^i=-q\phi_s+\left(\frac{\hbar^2}{2m_z^i}\right)^{\frac{1}{3}}\left[\frac{3}{2}\pi qE_{eff}\left(j-\frac{1}{4}\right)\right]^{\frac{2}{3}} \tag{4}$$

where the intrinsic energy in the substrate is the reference point. Since the effective field is a function of ϕ_s and V_{gs}, we can solve the equations iteratively.

The effective field in the double-gate structure can be defined in the similar manner, and we use the energy spectrum for two lowest energy levels as

$$E_{DG,j}^i\left(\phi_s,V_g\right)=-q\phi_s+\frac{\hbar^2\pi^2}{8m_z^id^2}j^2+\left(\frac{\hbar^2}{2m_z^i}\right)^{\frac{1}{3}}\left[\frac{9}{8}\pi qE_{eff}\right]^{\frac{2}{3}} \tag{5}$$

Once the surface potential is calculated with the quantized condition, the gate current density can be calculated analytically using the effective field of Eq. (3) and a semi-classical approach [3]. We derive the drain current using the drift-diffusion model, where the lateral field is determined by the gradient of the lowest sub-band along the channel, namely

$$I_{ds}=\mu Q_n\frac{1}{q}\frac{E_0}{dy}+\mu\frac{kT}{q}\frac{dQ_n}{dy} \tag{6}$$

where E_0 is the lowest subband.

To show the validity of the model, we compare the simulation results for MOS structures with the Schrödinger-Poisson scheme, which includes the wave function penetration into oxide region [4]. The *C-V* characteristics

for a planar structure are shown in Fig. 4, where the substrate doping is Na = 5e10^{18}cm^{-3}. The corresponding gate tunneling current densities are shown on Fig. 5.

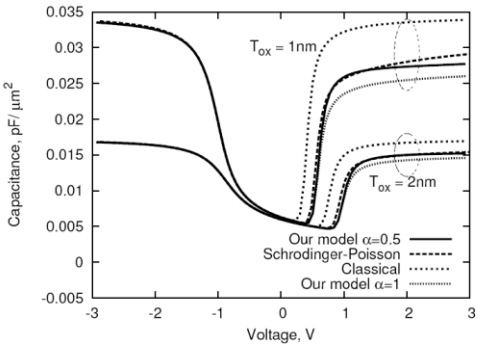

Fig. 4. The dependence of capacitances on the gate voltage.

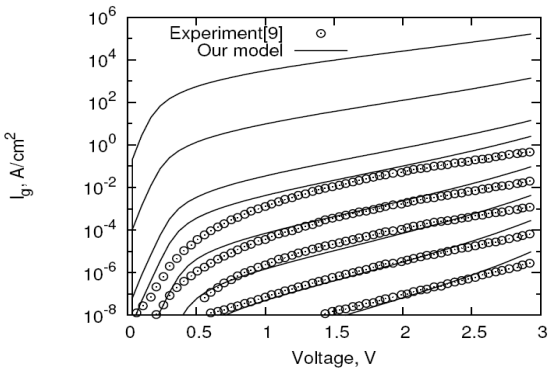

Fig. 5. The gate tunneling current density in a comparison between our model and experimental data.

2.2 Modeling of the SOI-MOSFET

Modeling of the SOI-MOSFET has been undertaken, and is focused on accurately capturing the floating-body effect, which should be also observed in the multi-gate MOSFET. The hole charge stored at the source side is explicitly considered in the Poisson equation, solved iteratively [6,7]. Result is shown in Fig. 6.

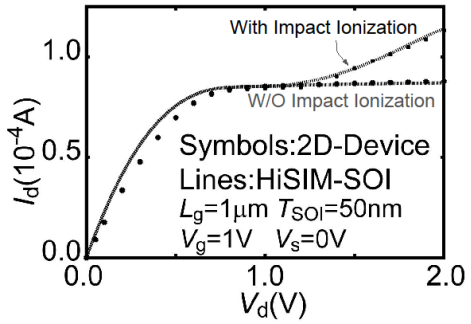

Fig.6. Calculated drain current with the developed SOI model HiSIM-SOI in comparison to 2D-device simulation.

2.3 Modeling of Multi-Gate MOSFETs

Modeling of MG-MOSFET has been investigated intensively at different affiliations (see for example [8,9]). Since it is till a beginning phase of the development, and there are still many unknown elements to be understood. Our approach is split on several different aspects. Here results are summarized.

[Modeling of Short-Channel Effect]

In device design of MG-MOSFET or DG-MOSFETs, the silicon substrate thickness together with channel doping concentration can be determined, if the channel charge is resulted from the surface or volume inversion. Because of the volume inversion, the concept of a surface potential, being a determining factor of the channel inversion charge density (per unit gate area), is no longer valid. It is thus imperative to know the potential distribution across the channel to the depth direction in order to predict the device characteristics.

First the short-channel effect is modeled as shown in Fig, 7 [10] by considering the volume inversion effect. For the modeling the effective oxide thickness is considered for the quantum-mechanical effect.

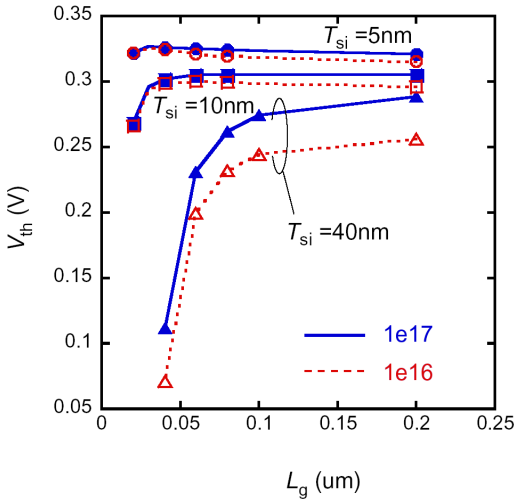

Fig. 7. Calculated threshold voltage V_{th} as a function of the gate length L_g for two impurity concentrations. Symbols are 2D-device simulation results and lines are model results.

[Independent Gate Control]

The DG-MOSFET has been invented 1980 by Sekigawa et al. [11]. The two gates have been controlled independently to obtain an additional feature of freedom, applicable for circuit design as shown in Fig. 8. The developed model focuses on the basic features of the gate control [12]. Results are shown in Fig. 9.

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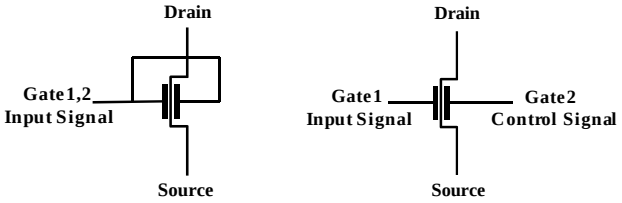


Fig. 8. DG MOSFET schematics with common and independent control of the 2 gates.

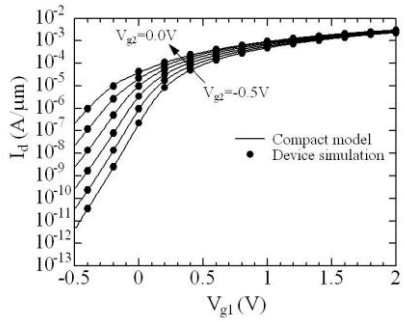


Fig. 9. Calculated drain current Id as a function of the gate voltage V_{g1} at one side of the double gate MOSFET for different gate voltage of the opposite side V_{g2}, based on the charge-sheet approximation.

[Versatile Generic DG Core Model]

A generic core model for the undoped four-terminal double-gate (DG) MOSFET valid for symmetric, asymmetric, SOI, and independent gate operation modes is also developed [13]. Based on the exact solution of the 1-D Poisson's equation of a general DG-MOSFET configuration, a generic drain current model is derived from Pao-Sah's double integral. The core model is verified by extensive comparisons with 2-D numerical simulations under different bias conditions to all four terminals. The concise mathematical formulation allows the unification of various double-gate models into a carrier-based core model for compact DG-MOSFET model development. Some significant results are shown in Figs. 11 and 12.

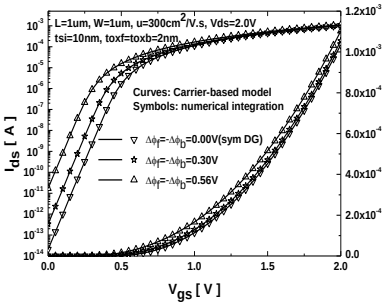


Fig.10. Drain current versus gate voltage for various work-function asymmetry differences.

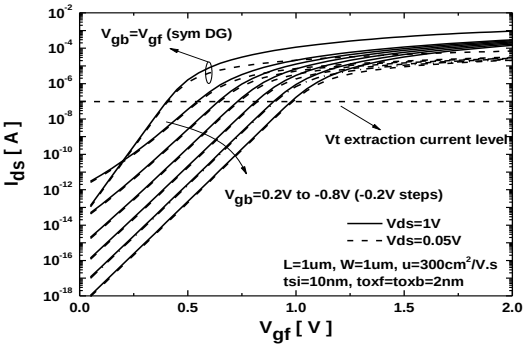


Fig.11. Drain current versus front gate voltage modulated by different V_{gb} in the independent gate DG MOSFET, compared with the symmetric DG-MOSFET.

Furthermore, a unified model for the undoped symmetric Double-Gate (DG) and Surrounding-Gate (SRG) MOS transistors is derived and verified [14]. It is shown that the solutions of the Poisson equation and the Pao-Sah current equation for DG and SRG MOSFETs can be represented by an equivalent mathematical equation.

[Iterative Solution of Potential Distribution]

Another compact DG-MOSFET model prototype called HiSIM-DG considers the volume inversion effect and solves the Poisson equation iteratively including any form of substrate doping [15]. The developed model calculates the bias dependence for not only the surface potential but also for the center potential of the silicon layer accurately. A predictive capability of silicon-layer-thickness dependence is verified by comparison to 2-D device simulation results. It is observed that the volume inversion effect prevents the DG-MOSFET from performance degradation for a reduction of device sizes. Calculated potential values are shown in Fig. 13.

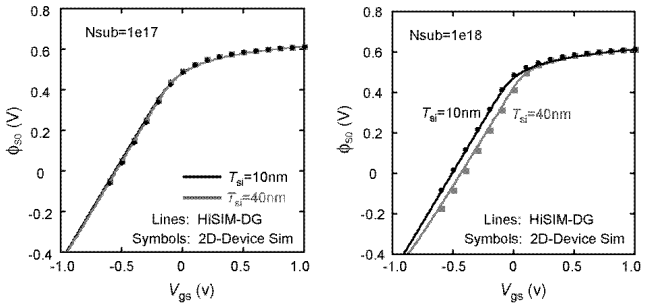


Fig. 13. Calculated surface potential values at the source side ϕ_{S0} and at the drain side ϕ_{SL} for two channel impurity concentrations.

[Derivation of a Closed-Form Equation]

We additionally deal with the closed-form solution of complete 1D Poisson's equation for the DG MOSFET without making any simplification in the constituents in space charge [16]. By integrating the Poisson equation under the gradual channel approximation and applying the symmetry condition at $x = 0$, we obtain:

$$\frac{d\varphi}{dx} = \sqrt{2A \cdot V_t \cdot \alpha + 2B \cdot V_t + 2C \cdot V_t \cdot \beta}\sqrt{e^{\varphi/V_t} - e^{\varphi_0/V_t}} \tag{7}$$

where

$$A = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q\phi_B}{kT}} \cdot e^{\frac{qV_{ch}}{kT}}, \quad B = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{-q\phi_B}{kT}} \cdot e^{\frac{-qV_{ch}}{kT}}$$

$$C = \frac{qN_A}{\varepsilon_{si}} \quad \text{and} \quad V_t = \frac{kT}{q}$$

$$\alpha(\varphi;\varphi_0) = \left(e^{-\varphi/V_t} - e^{-\varphi_0/V_t}\right) / \left(e^{\varphi/V_t} - e^{\varphi_0/V_t}\right)$$

$$\beta(\varphi;\varphi_0) = \left(\varphi/V_t - \varphi_0/V_t\right) / \left(e^{\varphi/V_t} - e^{\varphi_0/V_t}\right)$$

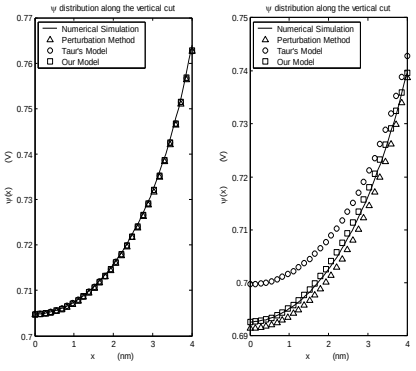
Notice that the intrinsic Fermi level in the flat band condition, E_i, is defined as the zero reference for the potential, while V_{ch}, which is the quasi-Fermi level for electrons in the given 1D cut with fixed coordinate along the channel, and V_g are all relative to the Fermi-level in the heavily doped source region.

Integrating Eq. (7), with α and β treated as constants, and meanwhile introducing a fitting parameter λ, Eq. (7) yields the following solution:

$$\varphi = \varphi_0 - 2V_t \ln\left[\cos\left(\sqrt{\frac{A}{2V_t}\alpha + \lambda\frac{B}{2V_t} + \frac{C}{2V_t}\beta} \cdot xe^{\frac{\varphi_0}{2V_t}}\right)\right] \tag{8}$$

Fig. 14 shows the comparison of the three model predicted results (our model, Taur's model and a perturbation model) and the numerical simulation data for the potential distribution profile in a DG-MOSFET, with different doping concentrations.

The fitting parameter λ reflects the relative contribution of inversion carriers compared with the ionized dopants and the minority carriers. Fig. 15 shows that λ increases with t_{si} but decreases with increasing V_g.



(a) (b)

Fig. 14 Comparison of the three model-predicted potential distributions with numerical simulation for different doping density. t_{ox}=2nm, t_{si}=8nm, V_g- V_{FB}=1.4V, V_{ch}=0.2V, (a) N_A=10^{16}cm^{-3},(b) N_A=10^{18}cm^{-3}.

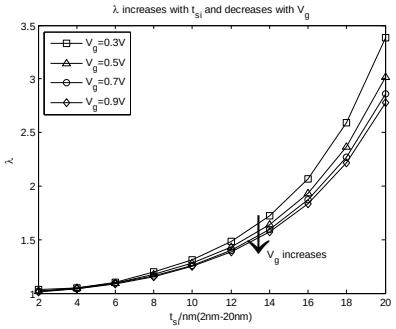


Fig. 15 The change of λ with t_{si} and V_g acting as parameter. Other parameters are t_{ox}=2nm, V_{ch}=0V, N_A=10^{18}cm^{-3}.

[Parasitics of MG MOSFETs]

Geometry-dependent parasitic components including parasitic gate capacitance and gate resistance in multi-fin-MOSFETs are modeled using a distributed RC coupling approach [17]. The accuracy of the model is verified by 2-D and 3-D device simulation. Fig. 16 shows the comparison of calculated capacitance and conductance as a function of fin spacing with 2-D device simulation results.

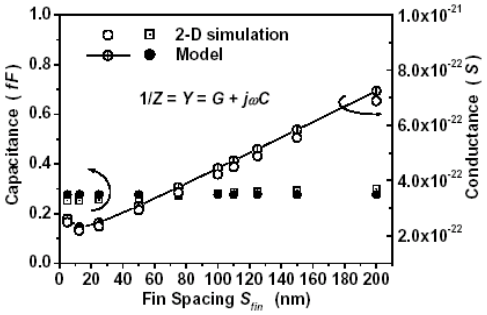


Fig. 9. Modeling of parasitic capacitances of the multi-gate MOSFET. Calculated results are also shown as a function of the finger spacing.

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2.4 XMOS Fabrication

To verify the constructed prototype models for the DG-MOSFET, real devices are also developed based on the XMOS technology [18,19], which has been under continuous refinement since more than 20 years at AIST(Japanese national institute of Advanced Industrial Science and Technology). The XMOS structure is schematically shown in Fig. 10.

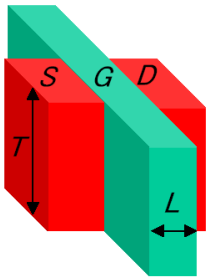

Fig. 10. XMOS structure now under fabrication at AIST(National institute of Advanced Industrial Science and Technology), Japan.

3 CONCLUSION

The development activities of NDMI (Nano Device Modeling Initiative), directed at a common modeling platform and a high quality MG-MOSFET model have been described. Our final goal is to provide a multi-gate MOSFET model by merging all our prototype results. This is performed by plugging in of the developed modular components into the platform. The subjects being undertaken are summarized in Table 1. Development of the SOI-MOSFET model has mainly the purpose to review phenomena observed in thin silicon layer devices.

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