Silicon on Ceramics - A New Concept for Micro-Nano-Integration on Wafer Level

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ABSTRACT

A new integration concept for micro-nano-integration based on a new bonding technique between nano-scaled, modified Black Silicon (BSi) and an adapted, unfired LTCC substrate is presented. The novel technique enables to combine advantages of silicon and ceramic technology, especially electrical and fluidic interconnects from nm- to mm-scale. Current bonding concepts of silicon on ceramics need joining materials like solders, adhesives or glass frits. Alternatively, silicon components can be mounted to a TCE-matched and fired LTCC by anodic bonding, which requires costly surface preparation by polishing. This step is eliminated by the use of the new technique. During a standard lamination process, a self-organized, nano-structured, grass-like silicon surface is joined with the green ceramic body. Pressure assisted sintering allows the co-firing of the composite. Dense contact between the Black Silicon surface and the ceramic, leading to a maximum average bonding strengths of 1775 N/cm², is achieved by optimization of the nano-interface and the lamination procedure. The hermeticity of the interface has been proven showing helium leak rates up to $1.9*10^{-8}$ mbar l/s. Hereby, a gas-tight interface (representing only a 10-nm leakage), which is impermeable for viruses and allows therefore biomedical use, is given. Electrical interconnects between ceramic body and silicon have been realized by means of metallized BSi penetrating into LTCC conductors. Prefabricated silicon-on-ceramic substrates with wiring and vias are compatible to a variety of semiconductor technologies for MEMS manufacturing.

Keywords: silicon on ceramic, black silicon, bonding of silicon to ceramics, wafer level packaging

1 INTRODUCTION

In the recent years, lots of applications based on nano effects and patterns have been investigated. A common difficulty to make use of nano elements in semiconductor devices is the realization of an intelligent and robust connection to the macro world. Tough mechanical, electrical or fluidic coupling of nano elements without affecting its functionality is required. A concept for micro and nano integration based on a fully silicon-ceramic wafer compound material solves this problem. The method is based on a bonding procedure between silicon and a low temperature cofired ceramic (LTCC). A LTCC tape with adapted TCE to silicon (trade name BGK [2]) is joined with a silicon wafer during a standard lamination process [1]. The self-organized, nano-structured silicon surface forms the contact with the green body. A subsequent pressure assisted sintering is utilized to co-fire the composite. This Silicon-On-Ceramic-substrate (SiCer) enables a wide range of design solutions. The functional silicon surface is bonded to prefabricated ceramic tapes with vias, wirings and fluidic channels. After sintering, the ceramic acts as a carrier system with electrical and fluidic connection. To ensure the electronical functionalities of MEMS devices, only a thin silicon layer is necessary. The separation of silicon areas can be easily done by standard silicon etching, while the ceramic works as a natural etching barrier. Consequently, the process enables system packaging on wafer level. Fig. 1 illustrates a scheme of this new concept for micro-nano-integration.

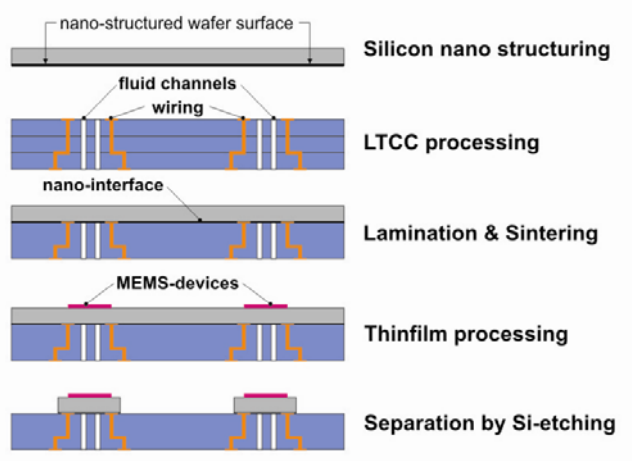

Figure 1: Work flow of the new integration concept

A number of optimization steps in silicon nano structuring and lamination procedures as well as in the adaptation of the BGK powder morphology were accomplished to realize a strong and dense contact between the Black Silicon surface and the ceramic.

2 TECHNOLOGICAL CHALLENGE

During the lamination, the nano patterned grass surface of the silicon wafer penetrates into the ductile and unfired LTCC tape. Because of the highly increased needle surface a form-fit bonding and a material connection is generated during the firing step. Therefore, the lateral shrinking of the ceramic must be avoided by the use of pressure assisted sintering.

2.1 Surface nano structuring of silicon

The nano-textured silicon surface is generated with a self-organized, lithography-free reactive ion etching (RIE) process, which leads to homogeneously distributed needles across a full wafer (Fig. 2). A parallel plate reactor (STS 320) with a cooled wafer electrode and a SF_6 / O_2 – plasma is used.

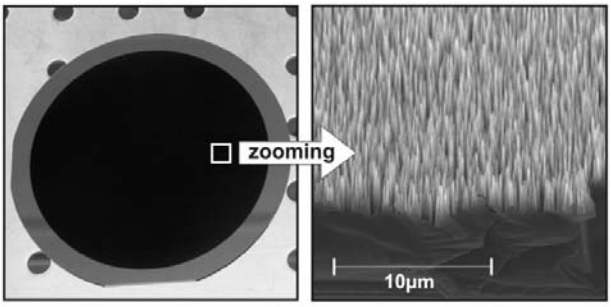

Figure 2: Homogeneously distributed BSi

Depending on the process time, needles up to 2.5 µm length can be achieved and the diameter varies from top to bottom between 5 nm to 400 nm. The needle-like structures have pitch dimensions between 100 nm and 200 nm. For an adequate penetration into the unfired, polymer-bound ceramic tape, the needles are too long and flexible (Fig. 3a). Therefore, an additional plasma treatment with Argon is accomplished for shrinking and thinning out the needles in order to adapt the needle geometry (Fig. 3b) to the powder morphology of the unfired BGK tape.

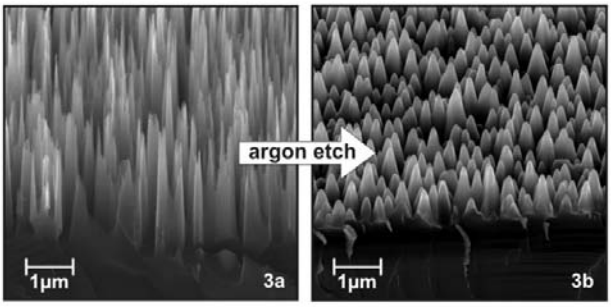

Figure 3: RIE-structured BSi before (a) and after treatment with Ar-plasma (b)

The nano-textured silicon surfaces fabricated as mentioned above can additionally be used as catalyst carrier or surfaces with tunable wetting angles or for room temperature bonding using the Velcro® principle [3]. In this way, the functionality of nano surfaces is implemented in Microsystems.

2.2 Characterization of BGK

BGK is a silicon-compatible LTCC-tape. Due to its powder composition the fired BGK has a silicon adapted thermal expansion of 3,4 ppm/K with a glass transition temperature of 590 °C (Fig. 4). The main constituents of the tape are a boro-silicate-glass, Al_2O_3 and cordierite, necessary for TCE-adaptation, as well as a polymer binder.

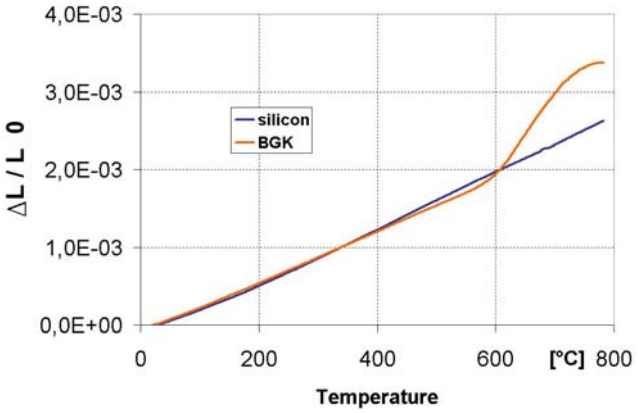

Figure 4: Dilatometer measurements of BGK and Si

BGK has a powder distribution with particle sizes of 50nm up to 2500 nm. However, the standard tape quota of fine particles is low (Fig. 5a) witch can lead to an incomplete filling of the spaces between the needles during lamination and firing, witch results in a non-hermetic interface. In a further development, higher quotas of fine particles were used in the slurry to adapt the BGK-tape (Fig. 5b).

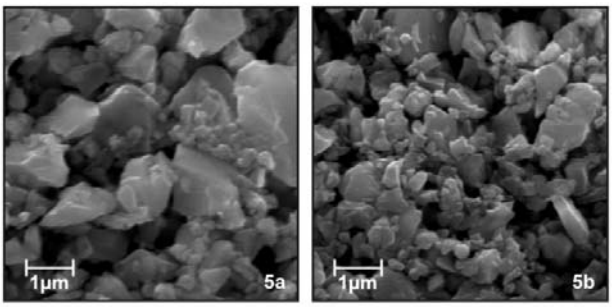

Figure 5: Powder morphology of standard BGK (a) and refined BGK (b)

2.3 Fabrication of the wafer compound

The first step of the bonding procedure is the lamination process, which brings the nano surface into a deep contact with the green BGK - tape. The needles penetrate into the polymer matrix of the green tape and the glass and ceramic particles adhere on the needle surface. Pressure, time,

temperature as well as the force rising rate are important lamination parameters and determine the bonding properties of the final compound. Therefore it was necessary to carry out a parameter variation by the use of Design of Experiments to find a lamination optimum. The lamination is carried out in an isostatic press. Pressure-assisted sintering is used to fire the compound. In a furnace press from ATV GmbH, a pressure of 0,5 MPa ensures the tight contact of silicon and ceramic during the temperature profile with a peak temperature of 850°C.

3 APPLICATION ASPECTS

3.1 Mechanical strength of the interface

A modified pull test was performed to determine the bonding strength. The bonded Silicon-On-Ceramic-substrate (SiCer) was cut into 10 mm x 10 mm squares and fixed to aluminum cylinder with epoxy resin. This assembly was pulled until the bond was teared. The analysis of more than 100 samples bonded with the adapted needle geometry of the silicon surface, leaded to an optimal parameter combination of 5.5 MPa, 25 min, 120 °C, 1 kN/min). A maximum average bonding strengths of 1775 N/cm² was determined for these parameter settings. Pressure and lamination time have the strongest influence on the process. An further improvement is achieved by the use of the refined tape. Finer particles fit better into the needle spaces and lead to a tighter interface. The bonding strength increases significantly to values above 5000 N/cm². Figure 6 shows a summary of average bonding strengths realized by common bonding techniques and the SiCer method.

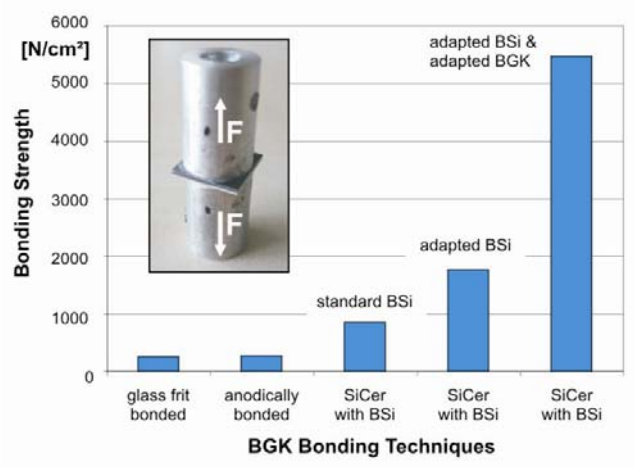

Figure 6: Average bond strength of SiCer compared with other silicon-to-ceramics bonding methods

3.2 Fluidic function

The integration of fluidic components like cavities, membranes or channels into ceramic multilayers requires optimized design and adequate process controlling. Particular the formation of hollows during the pressure assisted sintering is a very sensitive process step, because hollows can be collapsed. Test layouts with different stack sizes were used to investigate the influence of design parameters. For stacks with 7 layers, from which three tapes form cavities, hollows with dimensions up to 3.5 mm can be crack free manufactured without inlets. In order to characterize the tightness of the bond interface and the hollows, test chips with a micro fluidic vacuum chamber and different bonding frames, mounted onto an adapted vacuum flange (KF-series) were fabricated. A leak detection system, commonly used for vacuum devices, was applied to determine a helium leak rate (Fig. 7). First measurements show average leak rates of 2.8*10- 4 mbar l/s. This corresponds to a single leak with 1µm diameter which means the bonding is water-tight and a barrier for bacteria. The minimum leak rate for some samples was 1.9*10-8 mbar l/s. These interfaces were also gastight and impassable for viruses.

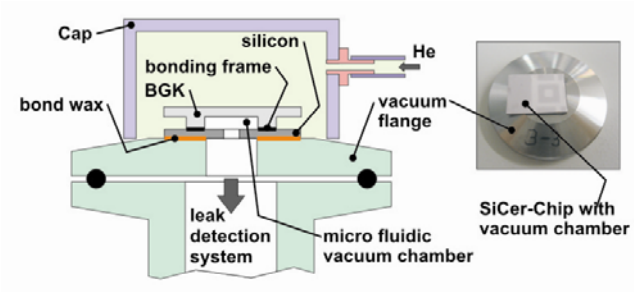

Figure 7: Test structure with leak rate setup

3.3 Electrical function

Electrical connections from the silicon component to LTCC carrier are formed, if metallized Black Silicon penetrates into LTCC metal vias. However, the metallization have to withstand the sintering at 850°C. Furthermore, the used metals should not lead to silicide formation. Figure 8 shows the fabrication. Platinum structures on oxidized BSi-needles, fabricated by a sputtering step and lift-off lithography were laminated to a prefabricated BGK-stack with gold vias (Heraeus TC 7101). After sintering, four-point-measurements were used to determine the sheet resistance of the metallized needle surface in order to calculate the transfer resistance at the interface "via/BSi". An average sheet resistance of 2,2 Ω/□ and a transfer resistance of 3,3 Ω is achieved.

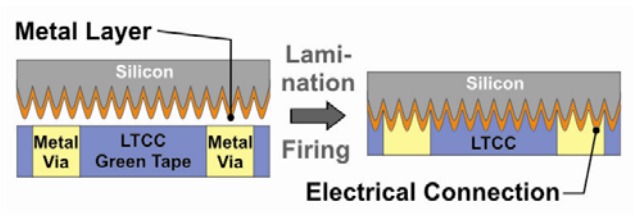

Figure 8: Assembly for electrical interconnects

3.4 System integration

To evaluate the potential of the new integration concept, a fluidic chip cooling system was chosen as a proof of concept (Fig. 9). The system consists of a ceramic carrier, which contains fluidic channels and the wiring for electrical connections. Above the channels a silicon chip with a heating structure and a measuring resistance is aligned. The needle structure forms the bond and laps additionally into the channels. It is expected that the enlarged surface improves the heat exchange.

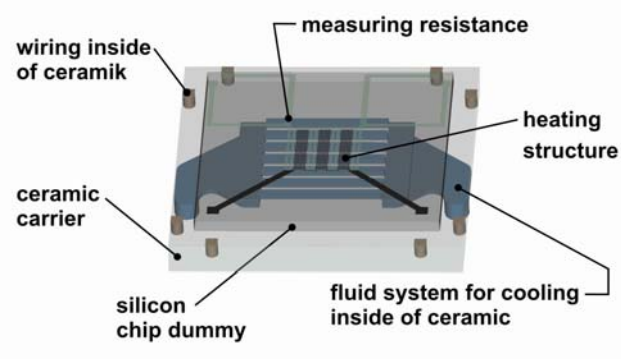

Figure 9: .Fluidic chip cooling system

All process steps have been combined in a first technological run, as depicted in figure 1. The fabrication starts with nano-structuring of the silicon wafer surface. The wafer is 100µm thick and has a diameter of 100mm. Subsequently, the manufactured substrate is covered with a 70 nm thermal oxide to prevent diffusion of metal into silicon at the interface during firing. The LTCC processing starts with cutting and punching of vias and fluid channels into the BGK-tape. After the via filling, conducting paths are screen-printed onto the top BGK-layer using a silver-platinum-paste by Heraeus (TC 7601). The prepared green body is joined with the silicon wafer with lamination parameters mentioned above. After sintering in a furnace press (ATV GmbH) the silicon MEMS processing follows. To build up the heating meander and the measuring resistance a bi-layer metallization of 25 nm chromium and 300 nm gold was patterned by means of lift off lithography. Afterwards the single silicon chips are created during a deep reactive ion etching process in an inductively coupled plasma machine. A patterned thick film resist serves as etching mask and protects the electrical components during the process. After separation of the single ceramic systems using standard wafer dicing, the silicon chips are connected electrically to the ceramic carrier by means of wire bonding. To proof the cooling concept, external pumps must be connected to the ceramic active chip cooling system. Therefore the design was fitted to an existing fluidic connector system. A prototype is depicted in figure 10.

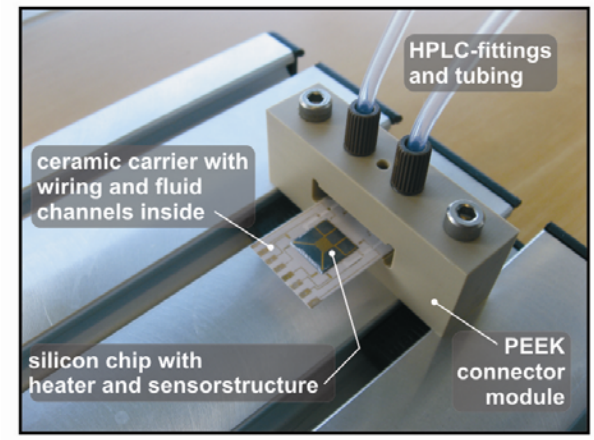

Figure 10: .Fluidic chip cooling system

4 SUMMARY

The capability of a new micro-nano integration concept based on a new silicon-ceramic wafer compound material was proven. A tight and high strength silicon-ceramic-compound was crack free fabricated in a standard wafer format of 4 inch. Electrical and thermal contacts as well as fluidic components can be fabricated from nm to mm scale in one batch using this novel integration concept.

5 ACKNOWLEDGEMENTS

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