Logicless Computational Architectures with Nanoscale Crossbar Arrays

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ABSTRACT

Modern computational architectures are reliant on basic logic circuits carrying out Boolean operations such as AND, OR, XOR, etc. Recently efforts have been made to replicate the functions of logic circuits using various nanoelectronic architectures in the form of nanoscale crossbars arrays. However, the interconnections required to be formed so as to create basic computational units such as full adders and more complex arithmetic circuits may be cumbersome to implement in nanoscale crossbars. The present article proposes an alternative computational paradigm formed from a hybrid of nanoscale crossbars and basic analog circuit elements so as to form arithmetic circuitry without the need for replicating basic logic functions.

Keywords: crossbar architectures, molecular electronics, analog computing, nanoelectronics, nanoprocessors

1 INTRODUCTION

Crossbar electronic architectures are currently under experimental investigation by start-up companies including Nantero, which has proposed carbon nanotube ribbons as mechanical switches in a crossbar arrangement [1], as well as more established corporations such as Hewlett-Packard, which has experimented with using rotaxane molecules as molecular switches between crossed nanowires [2]. Initial proposed applications have been in high density memory but, more recently, proposals for implementing basic logic structures and more complex computational structures have been made [3] and techniques are being explored to integrate crossbar architectures with more conventional CMOS circuitry [4]. However, in order to create useful computational architectures the current proposals would require interconnections between multiple sections or tiles of crossbar arrays leading to difficult design and manufacturing requirements. A simpler solution requiring only a single crossbar tile is thus desirable.

Figure 1 illustrates an example of a basic configuration for a nanoscale crossbar consisting of two arrays of orthogonally oriented parallel nanowires layers separated by a rotaxane molecular film such as described in [2] and [4]. Each intersection between the nanowires forms a rectified crosspoint equivalent to a configurable diode which can be set with either a high or low resistance state. The low resistance state may be represented of a binary value 1 while the high resistance state may be represented by a binary value 0 so that each column of the crossbar effectively stores a binary numerical value.

The primary advantage of such a crossbar architecture is that it is easily scalable to nanometer dimensions due to the simplicity of its structure using self-assembly or imprinting lithography without resorting to optical lithography or the use of any masks. The use of opposite doping between the upper and lower wiring plane generates a rectification in the current flow of the crossbar preventing feedback paths and allowing for addressing of an entire row (or column) of crossbar junctions at one time for faster reading or writing of data to the crossbar. However, the benefits of the crossbar design extends beyond the nanoscale and various proposals exist for RRAM (resistive RAM) to achieve two-terminal resistance state non-volatile crossbar memory arrays as a future replacement for SRAM and DRAM by using chalcogenide or conductive polymer materials. Table 1 provides examples of the high and low resistances states and approximate switching times for some of the materials used in the proposed designs as discussed in a variety of sources [1,2,5,6]. It is noted that in the cited sources the resistances are largely dependent on contact area with the material and thus nanoscale wire crossbars expectedly produce higher resistances than microscale wires used in GeSbTe and Cu-TCNQ resistance switches.

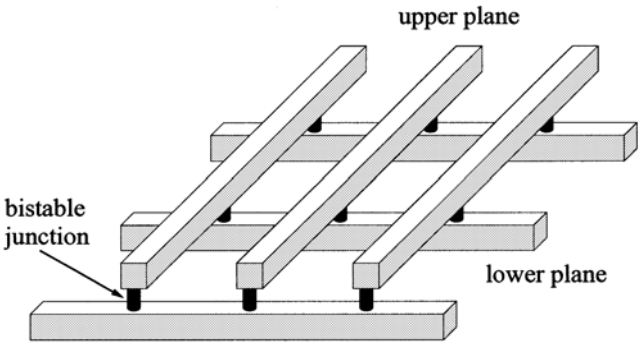

Figure 1: Nanoscale crossbar (from [4])

Resistance Switching Material	Low Resistance (On=1)	High Resistance (Off=0)	Approx. Switching Time
CNT ribbon (from [1])	112kΩ	~10GΩ	~10 ps
Rotaxane (from [2])	10^6-5x10^8Ω	>4x10^9Ω	~1 ns
GeSbTe (from [5])	6-20 kΩ	50-150 kΩ	10-30 ns
Cu-TCNQ (from [6])	~200 Ω	~2 M Ω	200 ns

Table 1: Examples of low and high resistance values and switching time of various resistance switch material.

2 LOGICLESS CROSSBAR ARITHMETIC

A circuit arrangement is illustrated in Fig. 2 for a basic arithmetic processor that used a 16x4 crossbar array connected to operational amplifier and analog-to-digital conversion circuitry. Operational amplifiers are a very basic component to many analog computing systems but have largely been rendered irrelevant in processor design due to the proliferation of digital computing over the past several decades. However, the key benefit of op-amps which make them useful for computation is that when a feedback resistance if provided between the output terminal and the inverting terminal, the generated voltage output V_{out} is a resistance weighted sum of the input voltages, V(j). This is a well known result of the conservation of current at the inverting terminal of the op-amp and is expressed as:

$$\frac{V_{out}}{R_f} = -\sum_j I(j) = -\sum_j \frac{V(j)}{R(j)} \quad (1)$$

where j is a summation index, I(j) represents the input currents, R(j) is the resistance connecting each input voltage V(j) to the inverting terminal, and R_f is the feedback resistance from the output voltage V_{out}.

Connection between a nanoscale crossbar and an op-amp such as shown in Fig. 2 may be achieved by using microscale wires for the rows of the crossbar and nanoscale wires for the columns. The resistances connecting the output of the crossbar rows to the inverting terminal provide a weighting value for each row and proper tuning of these resistances can establish a bit significance for each row. Due to the rectifying junctions within crossbar arrays the current provided by each junction of the crossbar for a particular row j can be expressed in terms of the input voltages V(i) to the columns of the crossbar as:

$$I(j) = \sum_i (V(i) - V_{rect})/(R(j) + r(i,j)) \quad (2)$$

where i is a column summation index, V_{rect} is a threshold voltage required to overcome the rectifying effect, and r(i,j) are the crossbar resistance states.

Provided that the feedback resistance is set to R and the input resistances are set to 2^j R - r, wherein r is the value of the average low resistance state for the resistance switching material, combining equations (1) and (2) produces:

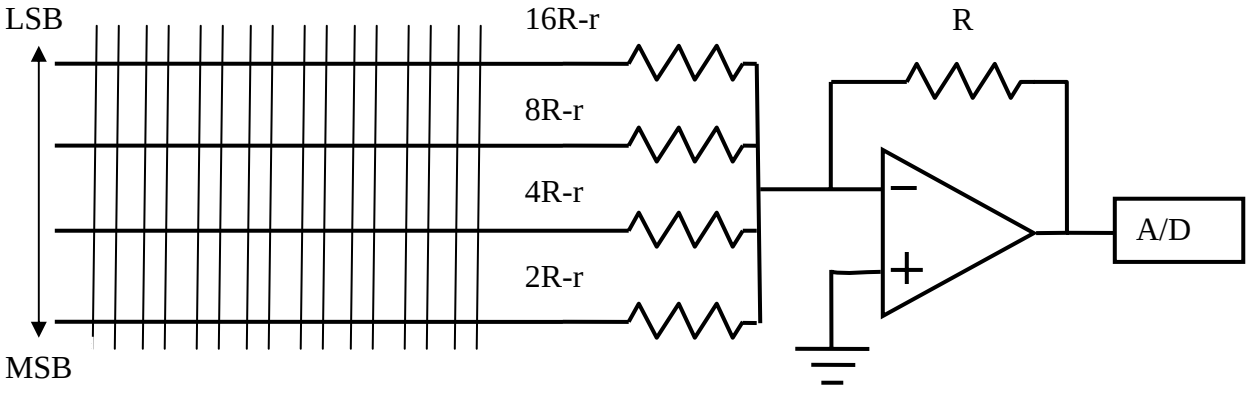

Figure 2: 16x4 crossbar with nanowire crossbar columns and microscale row wire connections to op-amp and A/D circuitry

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$$V_{out} = -\sum_{ij} \frac{R}{2^j R - r + r(i,j)}(V(i) - V_{rect}) = -\sum_{ij} T(i,j)(V(i) - V_{rect}) \quad (3)$$

where r(i,j) are the crossbar resistance states that contribute to the input resistances and T(i,j) is used to represent the overall transfer function between the op-amp output voltage and the input voltages of the crossbar.

Assuming an ideal behavior for the crossbar resistance states in which all of the low resistances are uniform in value and equal to r and all of the high resistance states are very large in comparison to R, T(i.j) may either take the value of $1/2^j$ (for r(i,j)=r) or a value close to zero (for r(i,j)>>R). The net effect of the proposed design is that if two bits in a common row are both at a low resistance state the sum increases the bit significance value so that $1/2^j+1/2^j=1/2^{j-1}$,which is equivalent to a carry operation in bit addition. Thus the selection of multiple columns of the crossbar array by a common voltage higher than V_{rect} results in an analog sum in accordance with the stored binary values of the selected columns. The provision of an analog-to-digital converter may then produce the expected digital output representing the binary sum of the stored values. The A/D resolution required for crossbars of different sizes is given by Table 2. Multiplication can similarly be performed by programming each column of the crossbar with a binary value representative of a multiplicand which is shifted between different columns and applying high or low input voltage to the crossbar in accordance with a multiplier.

Crossbar Size	Required A/D Resolution
4x4	>=6 bit
8x4	>=7 bit
16x4	>=8 bit
16x8	>=12 bit
NxM	>= ($\log_2$N+M)

Table 2: A/D conversion for crossbars of different sizes.

3 ADVANTAGES AND LIMITATIONS

The primary limitation of the proposed system for computation may be that analog circuitry typically has microsecond or nanosecond settling times whereas modern logic-based processors possess switching times of the order of picoseconds. However, the current trend of using multi-core processors demonstrates that raw speed is not the only factor when comparing computing power and the potential exists to include dozens or even hundreds of the proposed circuit design on a single chip. In addition, the proposed design offers the advantage of integrating both data storage and data processing in a single circuit. Whereas conventional logic-based processing requires several steps for transferring data between a memory circuit and a processor circuit the proposed circuitry has the potential to perform both functions so that a data retrieval operation may be achieved by selecting one crossbar column while an addition operation may be achieved by selecting two (or more) crossbar columns.

Other limitations include the requirement of a large ratio of high and low resistance states for the resistance variable material used in the crossbar. In order to produce consistent numerical results the total current produced by the high resistance states in any particular row should be significantly less than the current produced by a single low resistance state. This problem can be tempered to some degree by limiting the number of crossbar columns to be substantially less than the ratio between the high and low resistance states and by maintaining a high impedance input for any unselected columns. Fluctuation of current due to spatial or temporal changes between different r(i,j) values may also lead to inconsistent numerical results. However, by providing the weighting resistance R>>r in equation (3) the impact of variations in r may be reduced.

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