Monolithic Concept and the Inventions of Integrated Circuits by Kilby and Noyce*

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ABSTRACT

Getting history right is an important matter. It is in that spirit that this paper has been written about the invention of integrated circuits (ICs). The invention of ICs has been one of the most important inventions of the 20th century which has revolutionized mankind forever. They are used worldwide in many fields and applications: education, research, computers, medicine, internet, nanotechnology, biotechnology, government and others, and in every commercial, industrial and defense industries. Almost nothing is possible nowadays without using the ICs. Therefore it is important to know who invented them and how.

1. Introduction

All ICs manufactured and sold from the very beginning around 1960 when they had only a few transistors per chip to those today having over a billion transistors per chip have been monolithic-ICs made with Si. But what is the monolithic concept which is key for fabricating such ICs and how do these differ from the hybrid-ICs, has not been understood in the literature so far and by the laymen, non-engineering professionals and even some integrated-circuit engineers. Jack S. Kilby and Robert N. Noyce have been given the main credit for inventing the ICs, although several others also made crucial contributions. However, even Kilby's and Noyce's inventions have not been examined carefully to understand exactly what their inventions were and how they were achieved. For example, Kilby's invention[1] as demonstrated in his reduction to practice and as documented in his patent was only a hybrid-IC consisting of germanium (Ge) mesa transistors and passive devices (resistors, capacitors) on separate chips interconnected by thin metal wires dangling above the chips. The materials and technologies specified by Kilby are not, and have never been used to manufacture ICs. Several authors have erroneously credited Kilby to have invented the monolithic-IC. The purpose of this paper is to define the monolithic concept unambiguously, and to give important the historical facts of the inventions of ICs primarily by Kilby and Noyce. These facts will also prove that Noyce's invention[2] was that of a monolithic-IC, but it depended crucially on using the other inventions such as those of Lehovec[3], Hoerni[4] and Kooi[5]. Without these inventions, Noyce's invention would **no**t be feasible.

A few authors such as Kilby[1, 11, 12, 13], Rostky [6], Riordan & Hoddeson[7], Berlin[8], Braun[9] and Brock[10] have tried to tell the story of the invention of ICs. While Kilby[11] himself has given a historical account of the invention of the ICs in 1976, however he addressed and discussed the technical aspects of his invention and the patent[1] only recently[12] in 1998, and made some comments also on Noyce's invention and his basic IC patent[2]. The latter authors in references 6 - 10 do not address the technical issues of Kilby's and Noyce's IC inventions and their patents, and they have ascribed incorrectly Kilby's invention to be that of a monolithic-IC. Perhaps this may be due to their efforts more as historians without the technical precision of a scientist and engineer, rather than as contributors having first hand experience in solid state devices and IC technologies. Even Kilby's later comments[12] are incomplete at best (see section 6 of this paper).

While investigating the details of Kilby's patents, this author has received some new information about them (see section 5 of this paper) as recently as on September 26 and on November 02, 2005, from the United States Patent and Trademark Office (USPTO) [14, 15] which have not been reported in the literature previously. This clarifies the issue of the filing date of the original patent application[16] claimed repeatedly but erroneously by Kilby[1, 11,12]. The importance of clarifying this filing date, documented only recently[14, 15], lies in the fact that it proves that Kilby was incorrect to claim filing of his invention earlier than what it actually was according to the USPTO records. If such clarification was available about 40 years ago, it would have had a major impact on the early lawsuits among Kilby (Texas Instruments), Noyce (Fairchild), and Lehovec (Sprague Electric Company). However, they are not the subject of this paper.

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2. Summary of the key facts regarding the inventions of the ICs by Kilby and Noyce as documented in the literature

In order to appreciate the significance of understanding the monolithic and hybrid concepts, and distinguish between the inventions of the ICs by Kilby and Noyce from fundamental technology points of view, it is important at the outset to know what they are exactly. The key facts of these inventions as documented in the literature are summarized in Table–1.

3. Monolithic vs. hybrid concepts

We shall describe first how the "monolithic" concept has been presented in the literature so far, and then explain the difference between hybrid-ICs and the monolithic-ICs. It is important to understand this, because the "monolithic" concept used to characterize the IC invented by Kilby in the literature has been incorrect.

Riordan and Hoddeson[7] give an excellent historical account of the era from the birth of the transistor to the beginning of integrated circuits. Their last chapter is on "The Monolithic Idea", as they give concluding remarks in their book on the advent of integrated circuits. However, they ascribed erroneously the accomplishment of Kilby's reduction to practice as "The monolithic idea was finally a reality." It was not a reality completely, but it was a reality only partially and that too in a limited way. Kilby's reduction to practice was a hybrid-IC with mesa devices on two pieces of Ge, not a monolithic-IC on one chip (see section 3.1 for details). Briefly, Kilby had used mesa devices fabricated in Ge and not electrically interconnected, but they were interconnected by bonding metallic wires to the chips; they are not used in the monolithic-ICs.

Similar to the erroneous characterization of Kilby's reduction to practice of his invention described above, another research historian, Brock[10], has made similar characterization more recently on p. 18 of his book in 2006 as, "In the fall of 1958 Texas Instrument's Jack Kilby succeeded in demonstrating that the monolithic concept was a practical possibility, though he did not address the issue of yield." This erroneous characterization was re-stated on p. 26 of his book as "… the new integrated circuits that had been touted in 1959 by Texas Instruments as the first realization of the 'monolithic' circuit ideal." The issue of yield is secondary if not tertiary, in fact almost irrelevant, in Kilby's IC invention; the primary issue is that of demonstrating the monolithic concept, which Kilby did not achieve completely. Fabricating more than one mesa transistor in a single piece of Ge, which was being done routinely at Texas Instruments in 1958 and onwards, is only a part of the monolithic concept. To interconnect these transistors by wire bonding dangling above the Ge piece, as was done by Kilby, negates the very monolithic concept. Monolithic means electrically interconnect the devices (transistors, diodes, capacitors, resistors,…) on a piece of silicon or germanium by conductors which are also fabricated on the germanium or silicon, not by manually (or even mechanically) bonding the metal wires to each device. On p. 16 of his book, Brock also writes, "... Many members of the technical community were skeptical of the concept, for it too faced its own tyranny of numbers, a 'tyranny of yield.' "A fundamental tyranny which affects the yield of ICs critically in manufacturing, is the monolithic multilevel interconnection of all the devices needed in the IC. Kilby neither demonstrated nor even specified in his patent such monolithic interconnections, even in a single level, which are mandatory to fabricate the monolithic-ICs.

Another science-technology historian Berlin[8] also writes: "In the fall of 1958, a young Texas Instruments researcher named Jack Kilby set out to build an integrated circuit. By early 1959, he had built a complete circuit on a single germanium substrate. Kilby's circuit was meticulously hand assembled with a network of gold wires connecting the components to each other. The wires precluded the device from being manufacturable in any quantity, a fact of which Kilby was well aware, but his was undoubtedly an integrated circuit of sorts." Not all the "components" of Kilby's complete circuit were fabricated on a single Ge substrate. However, Berlin does credit Kilby correctly to have "built a complete circuit … meticulously hand assembled with a network of gold wires connecting the components to each other", and that it "was undoubtedly an integrated circuit of sorts". Berlin does not characterize Kilby's invention specifically to be either hybrid-IC or a monolithic-IC. However, those conversant in the state of the art, and the others after reading this paper, will agree that Kilby's invention as described by Berlin was not a monolithic-IC. Building a "complete circuit … meticulously hand assembled with a network of gold wires connecting the components to each other … (which) precluded the device from being manufacturable in any quantity" certainly does not constitute a monolithic-IC.

As it is evidenced from the above discussions that the key concept of what is "monolithic-IC" has not been understood from the early years to even now in 2006.

3.1 Hybrid-Integrated Circuits (Hybrid-ICs): In such circuits, the active devices (e.g., transistors and diodes) are fabricated singly or collectively on or from suitable semiconductors (e.g., Ge or Si). The passive devices (e.g., resistors and capacitors) could be fabricated from the same semiconductors, and/or from different materials. These devices, unpackaged or packaged, may also be mounted on or inserted in substrates having interconnects already formed in them, e. g, Printed Circuit Boards (PCBs), silk-screened ceramic substrates, glass, high-resistivity semiconductors, plastic, etc. Additional wire bonding is done between the various electrical contact regions of the devices and the pre-formed interconnects of the circuit. Such circuits with wire bonds dangling above the chips are called hybrid-ICs. These wire bonds preclude the chip from being monolithic, i. e., it is not a whole solid integral circuit.

3.2Monolithic-IntegratedCircuit (Monolithic IC)

The expressions monolithic-ICs and ICs shall be used interchangeably in this paper, except that the former may be used in particular when the monolithic aspect is to be emphasized.

In monolithic-ICs, all the active and passive devices are formed and fabricated in and on the surface of a single piece (chip) of a single crystal semiconductor, e. g., Si, wafer (substrate). But fabrication alone of the active and passive devices in the same chip in one block (monolith idea) is not enough. They must be interconnected contiguous and adherent to the insulating layer over the same body of the semiconductor to produce a solid integral monolithic-IC. If the devices are fabricated within the same body of the semiconductor, but they are interconnected by bonding wires dangling above the chip, such an IC is not a monolithic-IC anymore; it is then a hybrid-IC. This is explained in detail in the previous section 3.1.

Each wafer (now eight inch and 12 inch in diameter) has a large number of chips laid out in arrays. In monolithic-ICs, each fabrication step is done on the wafer as a whole, i. e., simultaneously on every chip on the wafer. More importantly in monolithic-ICs, each respective fabrication process step of depositions and/or growth of the various films/layers are done contiguously to the entire surface of the wafers, and the respective photolithographic masking and etching processes are used to delineate the patterns of the ICs in these films/layers simultaneously over the entire array of chips on each wafer. (The materials for contacts and interconnects are not evaporated through masks in monolithic-ICs, which were specified by Kilby[1,16] in his invention.) All the devices in each chip of the monolithic-ICs are interconnected by suitable multilevel metallization (e.g., Al) as needed by the circuit design, contiguous and adherent to the insulating layers over the entire surface of the wafer. This necessitates that all the metal interconnections must go over the insulating layers (e.g., SiO_2) from one device to another, as well as from one interconnect level to another in each chip. The p-n junction edges must be covered in situ during their fabrication by the insulating layers, so that the interconnections do not short the junctions with the adjacent regions. This is the fundamental invention of planar technology (Hoerni[4]). Another key contribution used in Hoerni's invention was by Sah[17]. He had given the experiments-based theoretical design curves for SiO_2 layer thicknesses needed to mask against dopant impurity for selective thermal diffusions in order to make planar junctions of desired geometries. This was a critical step in fabricating Hoerni's planar transistors, not recognized by others earlier. Appropriate isolation techniques (Lehovec[3]; Kooi[5]) were also used for the electrical isolation of devices and circuit elements within each chip. The entire surface of a completed monolithic-IC chip is contiguous to the surface of the single crystal semiconductor substrate. The monolithic-IC chip is one solid body, and it does not have any dangling wires bonded to different devices and regions, as it does in Kilby's hybrid-ICs.

To do all of the above in order to manufacture monolithic-ICs, the use of planar technology (Hoerni[4]) for fabricating various devices, such as transistors and diodes, is mandatory. Also, the semiconductor necessary for the planar technology is Si because of the high quality SiO_2 insulator film which is grown in situ on its surface. Ge is not suitable for this purpose because germanium oxide is not stable, so it cannot lend itself to give planar technology. Ge mesa technology and wire-bonding (used by Kilby[1,16]) for fabricating and interconnecting the devices will be extremely difficult if not impossible to use for manufacturing monolithic-ICs, especially at the billion-transistor

integration levels of today, even tens of transistors of 45 years ago in early 1960's.

The above discussions explain why Kilby's invention of the integrated circuit was a hybrid-IC, not a monolithic-IC. This will be further augmented by the discussions in the following sections, 6 and 7, to prove this conclusion unequivocally. Kilby demonstrated his invention by using Ge mesa transistors glued to a glass slide, and the devices were wire-bonded to interconnect them. These are not used in manufacturing the ICs. Noyce's invention of the integrated circuit was a monolithic-IC, not a hybrid-IC. Noyce did not reduce to practice his invention, which was written but un-witnessed in his lab notebook. However, he had specified Si planar technology, Al interconnects adherent to and going over SiO_2 layers without shorting p-n junctions, photolithography and etching techniques which are all used in manufacturing the ICs. Turning Noyce's invention into reality was done by several of his colleagues working with him during 1959-1960. The fact that Kilby did not receive any patent on IC technologies after receiving his original patent[1], suggests that he made no contributions to the Si planar technologies even after it was well established that they were mandatory for the manufacturing of the ICs. As discussed in section 6, Kilby refers only to his original patent[1] in his recent discussions[12] and to no other patents or papers by him or others. Kilby's specifications of the interconnect materials and processes in his patent[1] are also unusable in the manufacturing of the ICs.

The solar cells are not characterized as miniature ICs, because their p-n junctions and interconnections are huge in size as compared to those fabricated in transistors or even hybrid-ICs. The early workers in this field did use Si for solar cells inter-connected monolithically with Al, although their technology relatively speaking was crude. Some of them may feel entitled to be credited with the invention of the integrated circuit (e. g, see Queisser[19]). Therefore, they could also be considered as the inventors of the IC. But this is like claiming that a sledgehammer can be used to shape a diamond rather than the precision miniature tools of the diamond experts. Thus they will be ignored.

4. Sequence of relevant patents filing and issue dates

In order to understand the facts about the invention of the ICs, it is important for us to know the most relevant documents of these inventions. They are the original patents (Figs. 1 and 4) of Kilby[1] and Noyce[2] which have been used primarily in the literature, and by Texas Instruments and Fairchild corporations to claim the basic invention of ICs, as well as the original patent application of Kilby[16] and his papers[11,12] published in 1976 and 1998 respectively. Kilby's paper[13] published in 2000 before he was awarded the Nobel Prize was not a research publication, but it was a brief re-statement of the early history of the ICs already published[11] by him in 1976. Therefore it has not been listed below. The filing and the issue dates of a few relevant patents in addition to those of Kilby and Noyce are also listed in Table–2. *(They are listed chronologically with patent filing dates and public disclosures. As it is well known, listing patent filing dates and public disclosures chronologically documents the origin and sequence of conception of an invention, which is not reflected by the issue dates of the patents. The process in between the filing and the issue dates of the patent, as well as what each inventor did beyond his respective invention to advance its technology to what it is today, are also important to acknowledge and critique each contribution.)*

Key features of Saxena's patent # 3,687,722 on interconnects[20]

The key invention of this patent was to form the well-defined patterns of interconnects and contacts selectively without doing any etching of the metal films .The main purpose of listing this patent here is to give an example of the continuity of Saxena's work on interconnects and ICs from the early years to the present. It should be noted that this patent of Saxena[20] was filed on March 10, 1971, which was after Kooi's[5] patents on Local Oxidation of Silicon (LOCOS) were filed on Oct. 3, 1966, and Jun. 4, 1970. But it was granted on Aug. 29, 1972, which was well before Kooi's both patents were granted (Jul. 20, 1976; Aug. 14, 1973, respectively). Prior to Kooi's patents[5] on LOCOS process, which is used for the isolation of devices in ICs, Lehovec[3] had been awarded the patent for the p-n junction isolation of devices in ICs. Both Kooi's and Lehovec's patents were important and crucial to isolate the devices in manufacturing the monolithic-ICs.

5. Controversy over public disclosures and patent filing dates

There is no controversy over public disclosures and the patent filing dates of all of

the authors listed in Table – 2, except in the case of Kilby[1, 16]. In his patent no. 3,138,744, Kilby writes (cf: column 1, lines 55 – 57), "To that end, I have proposed in my pending application for patent, Serial No. 791,602, filed February 6, 1959, …" Saxena, while obtaining a copy of Kilby's[16] Application Serial No. 791,602, "Miniaturized Electronic Circuits and Method of Making" from the United States Patent and Trademark Office (USPTO), received the following two official responses recently:

5.1 E. Bornett[14], Certifying Officer, USPTO, to Dr. Arjun N. Saxena, "This is to certify that annexed hereto is a true copy from the records of the United States Patent and Trademark Office of those papers of the below identified patent application that met the requirements to be granted a filing date under 35USC111. Application: No. 03/791,602; Filing date: May 06, 1959." Sent by USPTO to Saxena on September 26, 2005. (See Fig. 5)

5.2 Customer Service Department[15], USPTO, to Dr. Arjun N. Saxena, "The product or service you requested cannot be fulfilled because the application #03/791,602 does not have an official filing date." Sent by USPTO to Saxena on November 02, 2005. (See Fig. 6)

The above seemingly contradictory responses from the USPTO cannot be explained. No matter what may be the problem of keeping records accurately and consistently at the USPTO, one fact is clear from the above responses**:** the official filing date of Kilby's Application No. 03/791,602 was not February 6, 1959, as claimed by Kilby[1]; instead it was May 06, 1959, which was also the filing date of Kilby's issued patent no. 3,138,744, and his other patents listed in Table-2.

It is also important to note (see Table–2) that according to the public records, no further action was taken either by Kilby or by the USPTO on Kilby's Application[16] No. 03/791,602, and no patent was ever issued for this application.

Several technology related matters in Kilby's Application[16] No. 03/791,602, such as "shaping" or "mesa" techniques prescribed in it for the fabrication and isolation of transistors and other devices, gold for interconnects, gold and aluminum evaporated through masks for ohmic contacts, etc, shall not be reviewed in detail in this paper. As it is well known to those conversant in the state of the art, these technologies are not used and will not work in manufacturing the monolithic-ICs.

6. Award of the pre-planar technology IC patents

The planar technology patents were issued to Hoerni[4] in 1962. Even though Kilby's patent[1] was issued in 1964, it is reviewed in this pre-planar section because it was filed earlier in 1959. Noyce's patent[2] was both filed and issued earlier than 1962, so it is also discussed in this section.

Kilby[1] was awarded the IC patent no. 3,138,744 (Fig.1) because of which he earned the recognition of being an inventor of ICs. Kilby's fundamental concept of his invention was stated in this patent only in part correctly (italicized here to focus on it) to suggest monolithic-ICs. For example, in his patent[1], he writes in Column 1; Lines 55–62: "… To that end, I have proposed in my pending application for patent, Serial No. 791,602, filed February 6, 1959 (Actually May 6, 1959 in Fig.1.), that *various circuit elements including diodes, transistors, and resistors all be formed within a single block of semiconductor material, thereby eliminating the necessity for separate fabrication of the semiconductor devices and the interconnections as mentioned above. …* "

The basic concept stated above was only partly consistent, also only in a limited way, with the concept of monolithic-ICs. Kilby did not specify how these devices formed within a single block of semiconductor were to be interconnected within the same block of semiconductor for a given IC, and to maintain the necessary electrical isolations of the devices and the interconnects. Also regarding the fabrication of the devices within a single block of semiconductor, Kilby did not even suggest the correct procedures in his issued patent[1] to accomplish what he had stated. The reduction to practice, and the materials and technologies specified by Kilby in his patent[1] and in the original application[16] to fabricate the devices and the interconnects were not consistent with those required for monolithic-ICs.

To explain further and re-emphasize, Kilby's specifications (text and the claims) in his original patent application no. 791,602 and the issued patent no. 3,138,744, were inconsistent with the purported invention of monolithic-ICs stated above (cf: Column 1; Lines 55 – 62). He had specified several materials and technologies which are not used, and will not work, to fabricate monolithic-ICs. The filing date of

Kilby's Application Serial No. 791,602 appears to have never been resolved, and no further actions by Kilby or USPTO were apparently taken on this patent application. However, based on the published records, no patent was ever issued on this original Application Serial No. 791,602. Further, he did not even specify in his patent no. 3,138,744 the planar technology which is mandatory to fabricate the monolithic-ICs. Even in his later critiques in "Origins of the Integrated Circuit", Kilby[12] left this question ambiguous and unanswered by concluding that "Despite these introductions, the monolithic concept remained controversial." In monolithic ICs, as described in section 3.2 above, planar technology, depositions and growth of the various interconnect and insulating films/layers are contiguous and adherent to the entire surface of the wafers, and the respective photolithographic and etching techniques are used to delineate the patterns of the ICs simultaneously over the entire array of chips on each wafer. In monolithic-ICs, mesa technology for devices is not used and the materials for contacts and interconnects are not evaporated through masks. As discussed above in sections 2 - 4 , several materials and technologies specified in Kilby's patent no. 3,138,744 are not used to fabricate monolithic-ICs.

Without going into further details in Kilby's patent, the bottom line is that his specifications for the integrated circuit consisted of a mesa transistor, whose emitter, base and collector regions were connected to passive components such as resistors and capacitors by interconnects of copper (Cu), gold (Au) and aluminum (Al) evaporated through masks over an insulating layer such as silicon monoxide. In monolithic-ICs, silicon monoxide and mesa transistors are not used, Cu, Au and Al interconnects are not evaporated through masks, and Cu and Au by themselves are not used because they do not adhere to the insulating layers. So at best, Kilby's invention claimed in his patent was an integrated circuit having mesa transistors, and the materials chosen for interconnects (except for Al for contact only to base regions) would be non-adherent and non-functional when used for a monolithic-IC structure. In the famous slide[6] showing Kilby's reduction to practice of his first integrated circuit, the transistor and passive components in two separate pieces of Ge (i. e., not fabricated in a single block of Ge – monolith idea) are glued to a glass slide, and the different regions of the transistor, capacitor and resistor are shown interconnected by dangling wires bonded to them. Thus, Kilby's invention specified in his issued patent[1] and the first integrated circuit constructed by him were that of a hybrid-IC, not a monolithic-IC.

Noyce[2] was awarded the IC patent no. 2,981,877, (Fig.4) based on his concepts for ICs, written but un-witnessed in his lab notebook, and he had not reduced them to practice by himself. However, he did specify Si planar technology and Al interconnects adherent to SiO_2 which are crucial and used in the monolithic-ICs. Such Al interconnects were not evaporated through masks to make contacts to and between various regions. In Noyce's invention, Al was deposited over the entire surface of the wafer, and photolithographic and etching techniques were used to delineate the interconnects over the entire array of the chips on the wafer simultaneously. The task of turning Noyce's IC concepts into reality was done by several of his colleagues (see brief discussions in Rostky[6] and Berlin[7]). This had caused bitter feelings and animosities among the key contributors, especially because Noyce was given the sole credit of being the "Co-inventor of ICs" with Kilby.

[Note: Saxena's role in the award of IC patent to Bob Noyce ahead of Jack Kilby is documented in two papers[24,26], therefore it is not discussed here. Kilby's lawsuit lost only partially to Noyce in contesting the award of the IC patent earlier by about 3 years and 2 months to Noyce than to him. Essentially, Noyce's specifications**,** consistent with monolithic-ICs of using Si planar technology and Al interconnects adherent to SiO_2 layers**,** prevailed. It was surprising, however, that Kilby's[1] description of his concept of ICs (cf: Column 1; Lines 55 – 62) was accepted by the USPTO. In addition, Kilby's actual specifications of the materials and technologies in the text of the patent, and more important**,** in its claims, were also accepted by USPTO. Most if not all of them were inapplicable to and inconsistent with monolithic-ICs; nevertheless the USPTO awarded the patent for the invention of ICs to Kilby[1] after reviewing it for over 5 years. Kilby also lost a patent interference suit against Lehovec[18.1, 18.2] in 1966 on the invention of p-n junction isolation of devices in ICs. As listed in Table-2, Lehovec had filed his patent independently only about 14 days earlier than Kilby, but was awarded his patent ahead of Kilby by about 26.5 months.]

7. Award of the post-planar technology IC patents and contributions to ULSICs and beyond: After Kilby[1] was awarded the IC patent no. 3,138,744, no further IC technology patents were awarded to him, even after it was well known that the planar technology, Si and Al interconnects adherent to SiO_2 were mandatory for fabricating monolithic ICs. As evidenced from the published literature and patents, Kilby did not contribute even later to the planar and other technologies which were, and are, essential to manufacture conventional and advanced monolithic-ICs such as ULSICs. However, he did obtain subsequent patents on miniature electronic calculators and in other fields, which were important contributions in their own right, but not to the invention and further development of ICs. Nevertheless, to repeat, Kilby was given the recognition of being the inventor of ICs based solely on one patent, viz., his patent no. 3,138,744. As mentioned also in section 6, even Kilby[12] refers only to his patent[1] no. 3,138,744 in his paper in 1998 on "Origins of the Integrated Circuit", and not to any other patent of his, when critically reviewing his and Noyce's fundamental inventions of the integrated circuit.

After Noyce[2] was awarded the IC patent no. 2,981,877, a few more patents were awarded to him on other process and design related issues of ICs. But no further patents were awarded to him that went beyond the present 2-Dimensional-ICs, for which Moore's Law holds[24]. Noyce did not publish any papers nor receive any patents for the interconnect technologies beyond Al, which are used today in many of the advanced 2D-ICs such as ULSICs. (Ultra Large Scale ICs) Examples of these are the use of Cu interconnects with appropriate barrier and cap layers, W (tungsten) for contact and via filling, planarization of dielectric and metal films, etc. The limitations of Moore's Law for the 2D-ICs can be removed by invoking the 3D-ICs and UPICs (Ultra Performance ICs). This is discussed in two memos of Saxena[27] given to Gordon Moore at Intel. See also two recent patents of Saxena[22, 23], and a recent paper[24].

8. Conclusion

Based on our critical and thorough review of the invention of the integrated circuits presented here, the conclusions to be drawn are as follows.

Noyce invented the concepts of monolithic-ICs in 1959 using Si planar technology, and Al interconnects. Kilby invented the concepts of hybrid-ICs in 1958/59 using Ge, mesa technology, and wire-bonded Au interconnects which were not adherent to SiO_2 layers.

The conclusions drawn here are not meant at all to be pejorative and disrespectful to Noyce, Kilby and all other contributors, or to impugn their contributions. The only objective of this author is to put all the available important facts on record. What is credible evidence depends to a certain degree, in a way similar to beauty, on the eyes of the beholder. Nevertheless, these are records in writing, and in technical English with engineering precision, not just a pleasure to the eyes.

As an example, Kilby's invention was only for the hybrid-IC, not for monolithic-IC. He had used materials and technologies which are not used at all in the monolithic-ICs manufactured and sold from day one to present. Kilby had only stated the concepts for monolithic-ICs in his patent which were partially correct, and that too in a limited way. Also, they were strikingly similar to Dummer's concepts published earlier[21]. All the specifications, drawings in Kilby's issued patent including its claims and in the original application, as well as his reduction to practice, did not support his statements and concepts for monolithic-ICs. Nevertheless, the evidence in his case was adjudged to be credible. Kilby was recognized "for his part in the invention of the integrated circuit" and was awarded the Nobel Prize in Physics in 2000, being a co-recipient, though given twice the amount of financial award than to each of the other two co-recipients (Alferov and Kroemer). Noyce's invention was for monolithic-IC, but it was based only on handwritten notes which were not even witnessed, and he did not reduce his concepts to practice. The latter was done by several of his colleagues. The evidence in his case also was adjudged to be credible, and he was credited with being the co-inventor of the monolithic-ICs. These are the facts, well established in the literature and documented by the dated patent claims. Therefore, no debate should be necessary to decide on their credibility.

Both Noyce and Kilby had acknowledged that it was a stroke of good luck for them to have invented the ICs. Good luck did play a greater role for them and their respective versions of the invention of ICs, than it did for several others who did work very hard to make the monolithic-ICs a reality in the marketplace from day one. There are many other scientists and engineers all over the world who also deserve the recognition

for their respective invaluable contributions to the invention of monolithic-ICs, and for advancing them to the ULSICs and the super-chips of today. This will require a detailed review which is not the subject of this paper.[30] However, to select a few other than Noyce and Kilby for their fundamental contributions to the invention of ICs, and singling out Moore for his contributions to take the entire industry beyond the IC invention to what it is today, the names (listed alphabetically) of Hoerni[4], Kooi[5], Lehovec[3] and Moore[28,29] should also be on top of the list.

The clap of the thunder of invention of ICs may be gone and belong only to a few. However, the thunder usually lasts momentarily or for a short duration only. But the resulting rains, akin to the invaluable contributions of many, bear the fruits and the crops for a long time to come, whether it is in the Silicon Valley and/or in the other global valleys. Certainly the invention of the ICs has borne, and continues to bear, the fruits and crops like the ULSICs to benefit all mankind. It is almost certain that the additional fruits like the 3D-ICs, UPICs, etc will also become realities in the future and benefit everybody, whether it will be in the author's and audience's lifetimes or not is of little or no consequence.

9. Acknowledgements

The author is deeply indebted to a large number of scientists and engineers, with whom he has discussed many aspects of ICs, ULSICs and beyond during the past 46 years. They have provided very helpful advice and comments. It is almost impossible to list all of them. A few key persons from the early years are as follows (listed alphabetically), to whom he is immensely grateful: Gordon Moore, (late) Bob Noyce, and Sheldon Roberts. The author is thankful to Toshiaki Masuhara for sending a copy of VLSI Systems Design[6] and nice comments on this manuscript. He also wishes to thank Kurt Lehovec, Dan Maydan, W. K. H. Panofsky, Chih-Tang Sah and Simon Sze for their help and key communications. Thanks are also due to author's daughter-in-law Mrs. Karen Saxena for her help in the preparation of the manuscript. A detailed account of the invention of ICs is planned[30].

10. References

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application that met the requirements to be granted a filing date under 35USC111."

Application: No. 03/791,602; Filing date: May 06, 1959." Sent by USPTO to Dr. Saxena on September 26, 2005; given as Figs. 5-1 and 5-2 in this paper.

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About the Author

Dr. Arjun N. Saxena is an Emeritus Professor of the Rensselaer Polytechnic Institute. He has both state of the art industrial experience and advanced academic background. He has been a Director and Professor, and established major R & D programs at Rensselaer, and at several industrial corporations. He is an inventor or co-inventor of major semiconductor technologies which are used currently in manufacturing. He has had over 40 years of experience in the multibillion dollar Si VLSI/ULSIC field, microelectronics technologies and other high-tech areas. He has served as the Consulting Editor of a book series on Microelectronics Manufacturing. He is a Life Senior Member of IEEE. A graduate fellowship has been established at Rensselaer Polytechnic Institute in his and his wife's name for

advanced research in microelectronics, because of his teaching and their substantial donation. Prior to 1960, Dr. Saxena has published in and contributed to the fields of Nuclear Shell Structure and High Energy Physics at the Institute of Nuclear Physics, India, and at Stanford University. He earned the PhD degree in Physics from Stanford and is listed in the Who's Who in the World and Who's Who in America.

Table - 1

Important Facts	Kilby	Noyce
1. What was the basic concept of the invention?	"….various circuit elements including diodes, transistors, and resistors all be formed within a single block of semiconductor material, thereby eliminating the necessity for separate fabrication of the semiconductor devices and the interconnections as mentioned above." (cf: Kilby [1]: column 1, lines 58-62). ***The basic concept stated above was only partly consistent with the concept of monolithic-ICs, and that too in a limited way. Kilby did not state nor specify how these devices formed within a single block of semiconductor were to be interconnected within the same block of semiconductor for a given IC, and assure that the interconnects and the devices were properly isolated electrically. Also regarding the fabrication of the devices within a single block of semiconductor, Kilby did not even suggest, what to say of giving, the correct procedures in his issued patent [1] to accomplish what he had stated. The reduction to practice, and the materials and technologies specified by Kilby in his patent [1] and in the original application [16] to fabricate the devices and the interconnects were not consistent with the monolithic-ICs.***	"….the present invention utilizes dished junctions extending to the surface of a body of extrinsic semiconductor, an insulating surface layer consisting essentially of oxide of the same semiconductor extending across the junctions, and leads in the form of vacuum-deposited or otherwise formed metal strips extending over and adherent to the insulating oxide layer for making electrical connections to and between various regions of the semiconductor body without shorting the junctions." (cf: Noyce [2]: column 1, lines 24 – 32). ***Noyce says it all in the very first paragraph of this patent. This is essentially how the monolithic-ICs are made.***
2. What was actually invented as described in the issued patent?	Hybrid-IC with mesa devices, not planar devices; wire-bonding of devices, not monolithic interconnects (cf: Figs. 3 & 4 of patent [1] ; Figs. 4, 5, 6 & 8 of original application [16]).	Monolithic-IC.
3. First public disclosure of invention.	Original patent application filed on May 6, 1959 (not on Feb. 6, 1959, claimed by Kilby).	US patent filed on Jul. 30, 1959. (Note that this was after Kilby's filed on May 6, 1959.)
4. Test circuit(s) defined.	Yes (phase-shift oscillator; multivibrator)	No (but done by others).
5. Reduction to practice of original invention.	Yes; Phase-shift oscillator - used a single Ge mesa transistor (not used in ICs), glued Ge to glass slide (not used in ICs), wire-bonded (not used in ICs) to 2 resistors and a capacitor; Multivibrator – used 2 Ge mesa transistors, glued Ge to glass slide, wire-bonded to 6 resistors and 2 capacitors.	No (but done by the others using Si planar technology, and Al interconnects adherent and contiguous to SiO_2, which are used in ICs).
6. Proof of the original invention.	US Patent no. 3,138,744 issued on Jun. 23, 1964; contested in courts for its delayed issue after Noyce's patent; Kilby's suit was lost partially because it was resolved that both the patents were essential for ICs; Kilby's suit against Lehovec [3, 17, 18] for p-n junction isolation was also lost (see section 6).	US Patent no. 2,981,877 issued on Apr. 25, 1961. (Note that this was much earlier than Kilby's patent issued on June 23, 1964.)
7. Contributions to planar and monolithic-IC technologies?	No	Yes; 4 US Patents since the above IC patent was issued.
8. Contributions to other advanced IC technologies, 3D-ICs and UPICs [24-26] ?	No	Co-founded Intel Corporation whose engineers are leading the world in inventing and putting into manufacturing practice the new technologies.

Table – 2

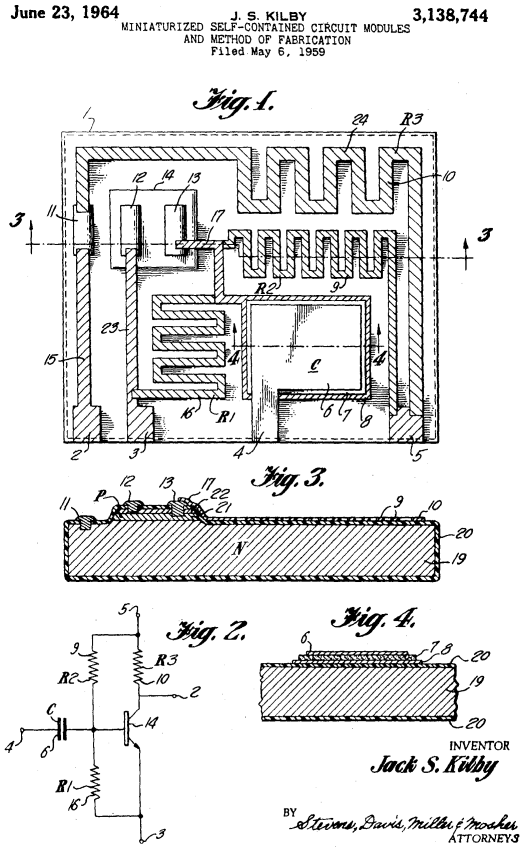
	Patent #	Filing date	Issue date
_ **Kilby [16] (ICs)**	None issued. Application Serial No. 03/791,602.	**Claimed by Kilby to be Feb. 6, 1959. (No official record [15] of this filing date. Official records show only May 6, 1959, as the filing date [14] . See Figs. 5, 6.)**	None issued.
_ **Lehovec [3] (Isolation)**	3,029,366	**Apr. 22, 1959**	April 10, 1962
_ **Hoerni [4]**	3,025,589 3,064,167	**May 1, 1959** **May 1, 1959**	Mar. 20, 1962 Nov. 13, 1962
(Planar Tech.)			
_ **Kilby**	3,072,832	**May 6, 1959**	Jan. 8, 1963
_ **Kilby**	3.115,581	**May 6, 1959**	Dec. 24, 1963
_ **Kilby [1] (ICs)**	3,138,744	**May 6, 1959**	Jun. 23, 1964 (Key patent) See Figure 1.
_ **Noyce [2] (ICs)**	2,981,877	**Jul. 30, 1959**	Apr. 25, 1961 (Key patent) See Figure 4.
_ **Kooi [5]**	3,970,486 3,752,711	**Oct. 3, 1966** **Jun. 4, 1970**	Jul. 20, 1976 Aug. 14, 1973
(LOCOS)			
_ **Saxena [20] (Interconnect)**	3,687,722	**Mar. 10, 1971**	Aug. 29, 1972
_ **Kilby[11]**	None filed (Review paper) **[Gave historical review of his IC invention.]**	**July, 1976**	(Review paper)
_ **Kilby[12]**	None filed (Technical paper) **[Made comments on his and Noyce's original patents [1, 2], "monolithic ICs", and Dummer's [21] approach to "…….. envisage electronic equipment in a solid block with no connecting wires."]**	**Mar. 31, 1998**	(Technical paper)
_ **Saxena [22] (3D-ICs & UPICs)**	6,110,278	**Aug. 10, 1998**	Aug. 29, 2000
_ **Saxena [23] (3D-ICs & UPICs)**	6,392,253	**Aug. 6, 1999**	May 21, 2002

Note: In addition to the key documents and patents of Kilby and Noyce on the invention of ICs, only a few patents of Lehovec, Hoerni, Kooi and the author are also listed in Table-2 above, because of their relevance to the invention of the original and the next generation ICs. The acronym 3D-ICs refers to 3-dimensional ICs, in which the active devices are also fabricated on a chip in the 3rd dimension above the surface of the single crystal Si wafer (henceforth referred to only as Si wafer), in addition to those fabricated in 2-dimensions on and near the surface of the Si wafer. The latter is done in all types of ULSICs being manufactured today, which are all 2D-ICs, and only the interconnections are fabricated in the 3rd dimension to interconnect the devices via multilevel interconnections. Moore's Law is applicable for only 2D-ICs[24].

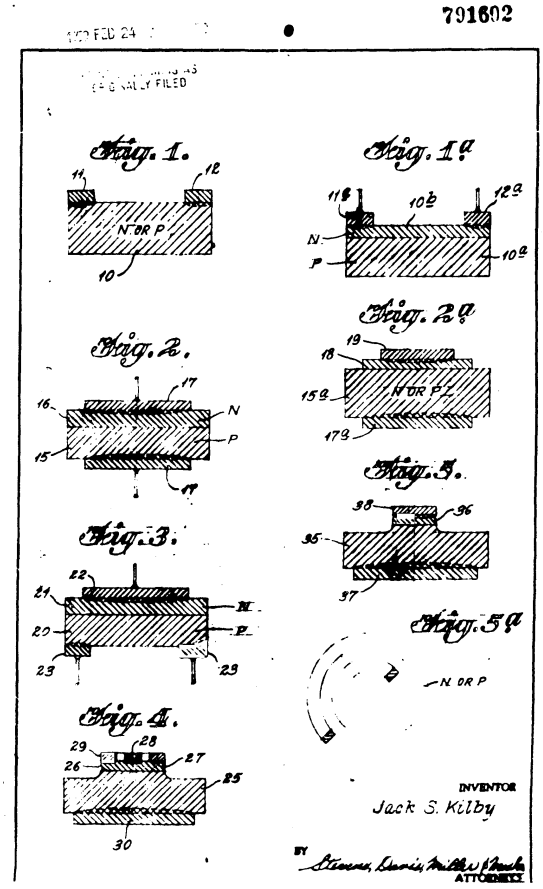
The acronym UPICs refers to Ultra Performance ICs[25], in which the active devices are fabricated on a chip using single crystals of Si and other semiconductors such as GaAs, GaAlAs, GaN, GaP, etc, in the 3rd dimension also above the surface of the Si

NSTI-Nanotech 2007, www.nsti.org, ISBN 1420061844 Vol. 3, 2007

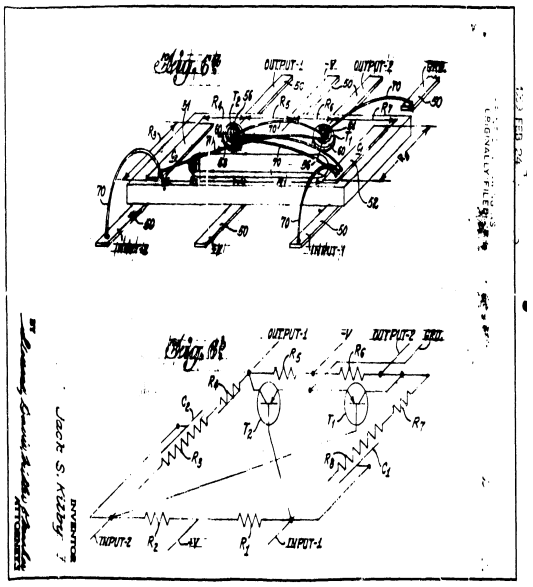
wafer, in addition to those fabricated in 2-dimensions on and near the surface of the Si wafer. All the devices in UPICs are interconnected via multilevel interconnections. In UPICs, both electrical and optical functions can be integrated monolithically.



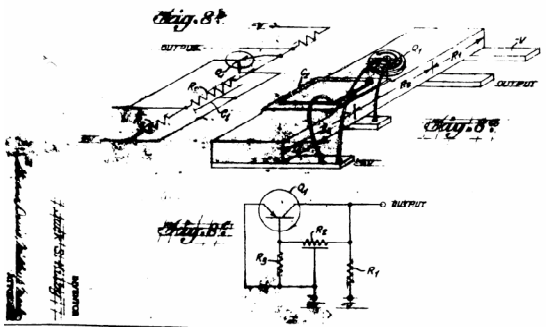
1. Figs. 1, 2, 3, & 4 of Kilby's U.S. Patent No. 3,138,744 (see ref. no. 1). Note the mesa structures in Figs. 3 & 4, instead of planar structures, used by Kilby [1] .



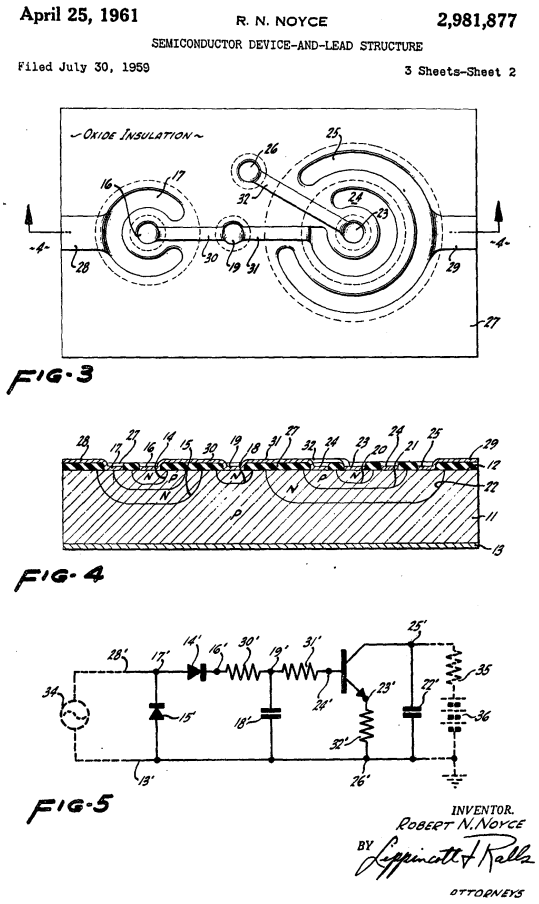
2. Figs. 1, 2, 3, & 4 of Kilby's Application No. 03/791,602 (see ref. no. 16). Note the mesa structures in Figs. 4 & 5, instead of planar structures, used by Kilby [1] .



3-1. Fig. 6 of Kilby's Application No. 03/791,602 (see ref. no. 16). Note the wire bonding in Fig. 6 instead of monolithic interconnects, used by Kilby [1] .



3-2. Fig. 8 of Kilby's Application No. 03/791,602 (see ref. no. 16). Note the wire bonding in Fig. 8 instead of monolithic interconnects, used by Kilby [1] .



4. Figs. 3, 4 & 5, of Noyce's U.S. Patent No. 2,981,877 (see ref. no. 2). Note the planar structure and the monolithic interconnects used by Noyce [2] .

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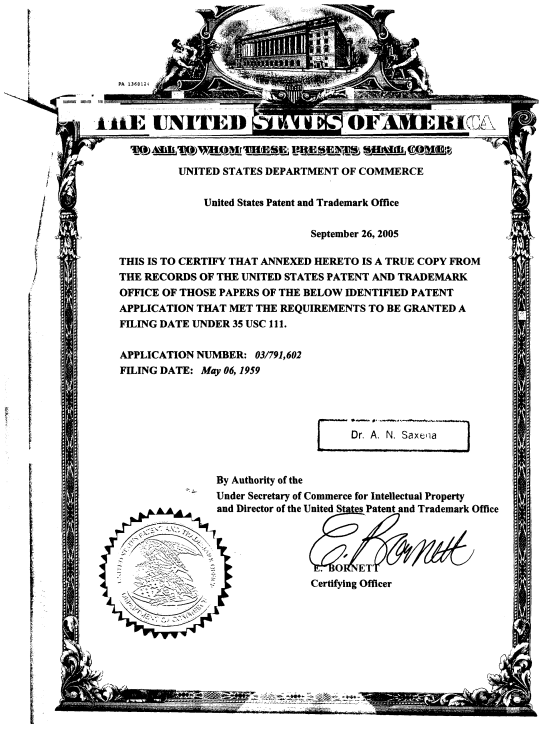

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FILING DATE: *May 06, 1959*

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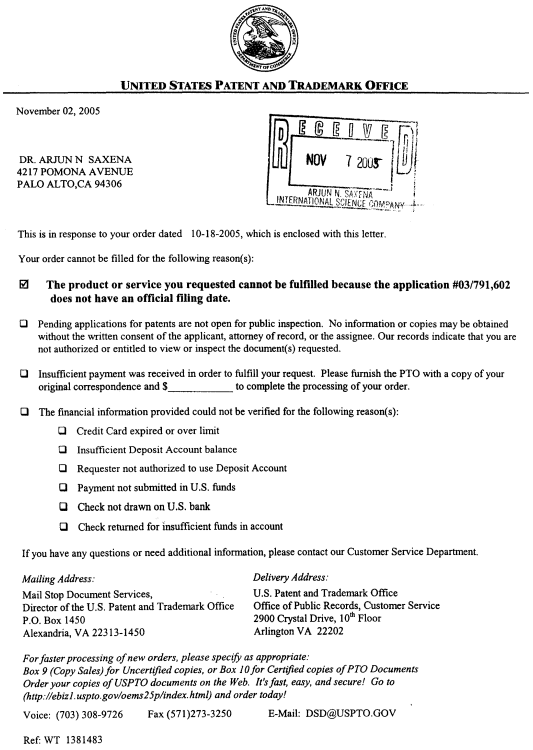

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