

# Integrating 1D Nanostructures in Devices and Circuits for Massively Parallel and Manufacturable Nanoscale Electronics and Photonics

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## ABSTRACT

A key barrier to wide-scale integration of functional nanowires in devices and systems is the difficulty in forming reproducible and efficient contacts to them. Unlike the research-based approach of sequentially connecting electrodes to individual nanowires for device physics studies, a massively parallel and manufacturable interfacing technique is crucial for reproducible fabrication of dense and low-cost nano-device arrays. We developed a novel epitaxial interfacing technique for integrating semiconductor nanowires in devices that resulted in highly reproducible and linear ohmic contacts and contributed to exceptionally low noise. We fabricated two electrically isolated and opposing vertical Si surfaces using optical lithography along with wet and dry etching and grew lateral nanowires from one surface and epitaxially connected them to the other, forming mechanically robust and electrically continuous “nano-bridges”. Both group IV and III-V nanowires were bridged between Si electrodes. Based on our current-voltage measurements and a constructed model, we calculated the specific contact resistance to be in the range of  $4 \times 10^{-6}$  Ohm-cm<sup>2</sup> for bridged Si nanowires. This value is more than 2 orders of magnitudes lower than that of research based approach of evaporating metals on semiconductor nanowires for contact formation. Individual electrical access to nano-devices without recourse to nanoprobes or tedious and expensive serial interfacing procedures has been achieved for the first time. This unique approach of massively parallel ‘in situ’ epitaxial connections open new opportunities for integration of nanowires for designing novel nano-scale electronic and photonic devices with a major improvement in the cost/performance ratio.

**Keywords:** nano-bridges, nanoprobes, massively parallel, contact.

## 1 INTRODUCTION

Future ultra-high density electronic and photonic systems will require ‘bottom-up’ synthesis technique in compliance with the remarkable trend in miniaturization with the current CMOS fabrication technology. Although much attention has been paid by the researchers worldwide for the ‘bottom-up’ technique, integration of one

dimensional (1D) nanowire structures into electronic devices and circuits remains an ongoing challenge for the research community.

Researchers have successfully synthesized 1D nanowires with various controllable features like chemical composition, morphology and electrical properties with a number of material systems [1-17]. Numerous discrete functional nanowire devices such as nano-scale FETs, [5, 18] p-n diodes [5], light emitting diodes (LEDs) [5], bipolar junction transistors [5], complimentary inverters [5], complex logic gates [3, 9] and lasers [20] have been developed. Even though noteworthy progress in the synthesis and application of nanowires has been achieved, interfacing nanowire devices with existing circuit elements has been a challenge since they were first envisioned as the building blocks of many future applications ranging from electronics and photonics to life sciences, medicine and future computers. Large scale application of nanowires has been hindered mainly due to the absence of any technique for controlled assembly of nanowires within integrated circuits.

Practice of connecting individual electrodes to nanowires is well established since the evolution of this exciting research area for the purpose of understanding device physics and exploring novel device applications. However, it is essential to develop a massively parallel and manufacturable interfacing technique with reproducible fabrication capability of industry level dense and low-cost nanodevice arrays with high throughput. The integration scheme should be universal and compatible with the existing IC processing techniques. It is also very important that the mass manufacturing technique allows precise control on the nanowire length, density per unit area, contact resistance and mechanical properties of the fabricated nanowires. Up until no reported techniques for interconnecting nanowires meet all of the above mentioned requirements and a radically different approach is intended [5, 19].

We developed ‘*nano-bridges*’- a unique mass fabrication technique that is entirely compatible with current IC fabrication processes. This article presents the novel, scalable and universal approach that will enable us to solve the long-standing issues of interfacing nanowires. In

this article we also demonstrate the growth of patterned nanostructures using metal catalyst and their contact properties.

## 2 PARALLEL ASSEMBLY OF NANOWIRES

Metal-catalyzed chemical vapor deposition (CVD) is often used for growing nanowires on semiconductor or insulating substrates like oxide or nitride. Subsequently the nanowires are interfaced to electrodes using a complex and often expensive process.

Islam *et al.* reported a novel epitaxial bridging technique for interfacing Si [21] and InP [22] nanowires between Si electrodes. In this unique approach, we first form the electrodes and then grow the nanowires from one electrode toward the other and thus form a dense array of nanowires between two electrodes. Lateral growth of nanowires was achieved between two opposing (111) oriented sidewalls. The “nano-bridges” so grown have a high surface to volume ratio and are suitable as sensitive sensor elements.

A (110) oriented silicon-on-insulator (SOI) wafer with a 5 $\mu\text{m}$  thick device layer and a 100nm thick buried oxide layer was patterned and etched using RIE to form two electrically isolated electrodes with their edges perpendicular to the <111> planes of the substrate as shown in Figure 1. The gap between electrodes was varied between 1 – 10 $\mu\text{m}$ .

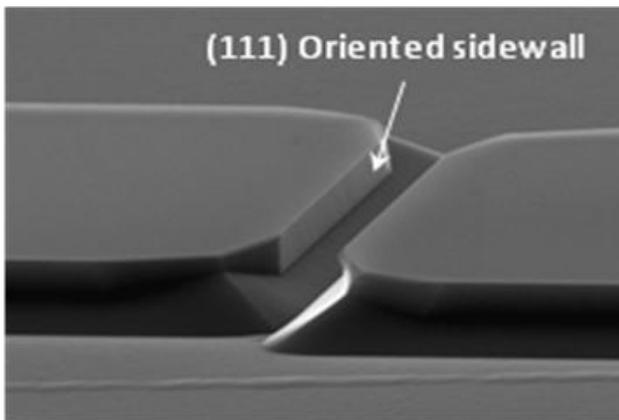


Figure 1: SEM image of a pair of isolated electrodes.

Titanium or gold on the order of 1nm was deposited by electron-beam evaporation onto the vertical surfaces of one of the etched (111) oriented grooves. The samples were annealed in hydrogen inside a chemical vapor deposition reactor to form Au-Si alloy nanoparticles or to reduce the native oxide on Ti and form  $\text{TiSi}_2$ . A mixture of  $\text{SiH}_4$  and HCl was then introduced into the hydrogen ambient to grow the nanowires at  $\sim 640^\circ\text{C}$ . Diborane ( $\text{B}_2\text{H}_6$ ) was introduced

into the chamber for doping the nanowires as p-type. The nanowires grew across the gap towards the (111) oriented face of the opposite electrode. Upon reaching the opposite sidewall, the nanowire “self-welded” by continued catalyzed decomposition and formed mechanically robust contacts. Figure 2 shows that most of the Ti-nucleated Si nanowires were misoriented and tapered requiring considerable optimization. Unlike the Ti-catalyzed nanowires, most Au-nucleated nanowires are straight and  $\sim 70\%$  of them intersect the opposing sidewall at an angle of  $90^\circ \pm 0.5^\circ$  as shown in Figure 3. The strength of the nanowire contact is indicated by the nanowires often breaking along their length, rather than at the interface. Aluminum (Al) contact pads were then deposited on the Si electrodes after resist patterning, oxide etch, Al deposition and lift-off process. The devices were then annealed at  $450^\circ\text{C}$  in forming gas.

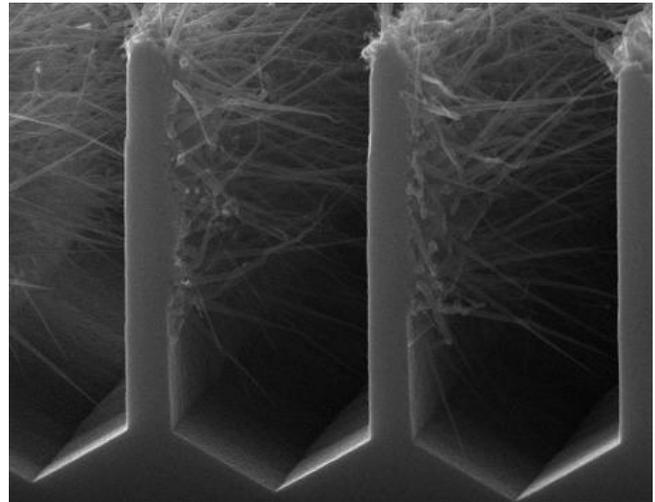


Figure 2: Cross-section SEM micrograph of epitaxial nanowire growth from (111)-oriented sidewall surface using Ti catalysts. Most of the nanowires are misoriented and tapered.

A four-probe measurement setup with a DC voltage sweep from -5V and +5V yielded a linear current-voltage (I-V) characteristics indicating the ohmic nature of the nanowire/electrode interface for the Si nano-bridges.

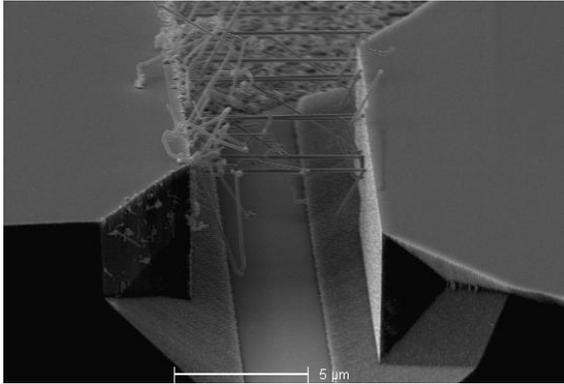
## 3 CONTACT RESISTANCE

As shown in Figure 3b, the total measured resistance of a bridged nanowire device is a sum of the contact resistance ( $R_{\text{contact}}$ ), nanowire resistance ( $R_{\text{NW}}$ ) and the resistance of the electrode region ( $R_{\text{electrode-region}}$ ) as summarized by the equation below.

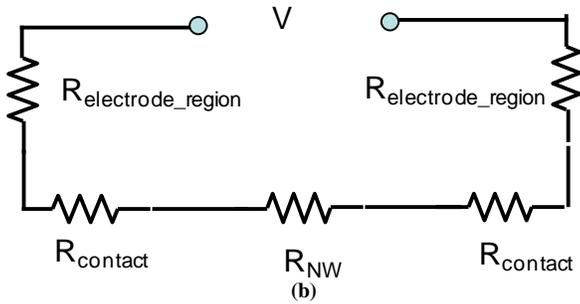
$$R_T = 2R_{\text{electrode-region}} + 2R_{\text{contact}} + R_{\text{NW}} \quad (1)$$

Contact resistance ( $R_{\text{contact}}$ ) is defined as the resistance at the interface of the nanowire and the Si electrodes. An SEM

micrograph of an actual contact of a nanowire impinging end is shown in Figure 4. Analytical modeling of this resistance is challenging it depends on the quality of the contact. Moreover, the two contacts at the ends of a nanowire grown using a Vapour-Liquid-Solid (VLS) process are asymmetric in behavior. The tip or the impinging end is the dominant contributor to the nanowire contact resistance.



(a)



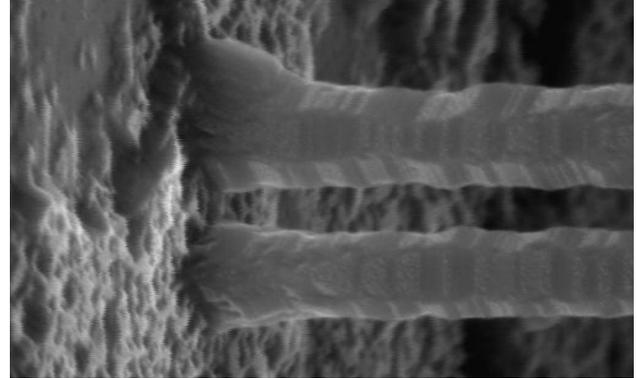
(b)

**Figure 3:** (a) “Nano-Bridges” across electrically isolated electrodes. The nanowires grow from left to right in these SEM views. Au-nucleated nanowires grown mostly perpendicular to the (111) sidewalls. (b) Equivalent circuit realization of the resistances contributing to the total measured resistance in a bridged nanowire.  $V$  is the applied external bias voltage.

We developed an empirical model to estimate the impact of contact resistance for bridged nanowire structures based on the I-V data from our Si nano-bridges. We found that the contact resistance depends on the effective conducting cross-section area of the nanowire, i.e., it is influenced by the presence of surface charge induced depletion layer on the nanowire surface. We also see that the contact resistance becomes significant as the wire diameter is scaled. We estimated specific contact resistance to be in the range of  $4 \times 10^{-6}$  Ohm-cm<sup>2</sup> for bridged Si nanowires. This value is more than 2 orders of magnitudes lower than that of research based approach of evaporating metals on semiconductor nanowires for contact formation.

Commonly adopted techniques of contacting the nanowires placed on insulating substrate with evaporated metals often lead to Schottky barriers at the interface which

are hard to overcome. Bridged Si nanowires have demonstrated highly linear contact characteristics along with potential benefits of their good mechanical robustness, and ease of integration with Si technology. These unique attributes of the epitaxially interfaced nano-bridges position them as attractive choice for realization of mass-manufacturable 1D nanoscale devices.



**Figure 1:** An SEM of an actual contact of the nanowire to the Si electrode. Contact quality has a significant bearing on  $R_{\text{contact}}$ .

## 4 CONCLUSION

We have demonstrated a self-assembled massively parallel fabrication technique for integrating 1D nanostructures compatible with the conventional IC processing methods. This new methodology will open new windows in using nanowires to design varieties of electronic and photonic devices. We have also investigated nanowire-electrode contact properties, which are very crucial for low power and high speed applications. Individual electrical access to a large number of nanowire devices without recourse to nanoprobes or tedious and expensive serial interfacing procedures is achieved using our bridging integration technique. We are now employing our massively parallel ‘*in situ*’ epitaxial connection method to implement the interfacing of nano-devices in most widely used semiconductor materials including Si, Ge, SiGe, SiGeC, GaAs, InP and ZnO. Growth conditions, doping techniques and wafer processing methods are also explored to understand and optimize nanowire-bulk connections, and consequently to facilitate mass-manufacturing of nanodevice. Novel devices with innovative and known quantum effects are being designed and studied with the goal of making them an integral part of future nano-scale electronics and photonics. The results of our work will lead to unprecedented device density in integrated circuits, ultimately making the nanowire based devices a commercial reality with a major improvement in the cost/performance ratio.

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