Compact Capacitance Model of LDMOS for Circuit Simulation

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ABSTRACT

A new capacitance model for LDMOS (Lateral Double Diffused MOS Transistor) is proposed. The effect of lateral non-uniform channel doping on capacitance characteristics is included. Overlap region capacitance modeling is properly handled and the two stages in Cgg curve are well modeled. The distributed RC network has substantial effect on LDMOS capacitance characterization due to the non-symmetric structure of LDMOS and its implication on modeling is discussed. The new capacitance model is validated with measurement data.

Keywords: LDMOS, capacitance model, Cgd, overlap capacitance, non-uniform doping

1 INTRODUCTION

LDMOS technologies are widely used for various high voltage applications such as switch-mode power supplies and power amplifiers [1, 2]. One of the major advantages of LDMOS is it's compatibility to conventional CMOS technologies thus the ease of integration with low-voltage CMOS circuits [3]. Optimal design of power circuits based on LDMOS requires accurate high-voltage LDMOS models for circuit simulation which aim to well describe the device characteristics including both DC and AC behaviors over a wide range of transistor geometries, operating voltages and operating frequencies.

Until recently, it has been a common practice to use sub-circuit model called macro model in high-voltage circuit simulation due to the lack of accurate and physical compact LDMOS model available in commercial circuit simulation tools [4-6]. While macro models can usually fit I-V data well [7], it often has difficulty in fitting C-V data. However, the capacitance model accuracy, especially for Cgd, is critical for predicting dynamic behaviors of LDMOS circuits in switching transition. This is even more important for RF applications in which accurate capacitance modeling is even critical for circuit simulation. The Cgd modeling in LDMOS is complicated due to the unique process flow and device structure of the LDMOS devices. Specifically, the existence of large gate-to-drain overlap region contributes a big part to Cgd, and the lateral non-uniform doping of channel also plays an important role in the Cgd characteristics.

In this paper, using a typical LDMOS structure, the capacitance components and their bias dependencies are analyzed. Special considerations for a compact LDMOS capacitance model are given in the non-uniform channel doping, the gate-to-drain overlap capacitance as well the distributed RC network effects. The model scalability is also discussed. Finally the capacitance model is further validated with the measurement data.

2 MODEL DESCRIPTION AND RESULTS

In this section, a typical LDMOS structure is provided as the basis of the analysis and model development. Then modeling approaches for different aspects of LDMOS capacitance features are given in each sub-section. Finally, model fitting results with measurement data are provided.

2.1 Typical LDMOS Structure and Electrical Characteristics

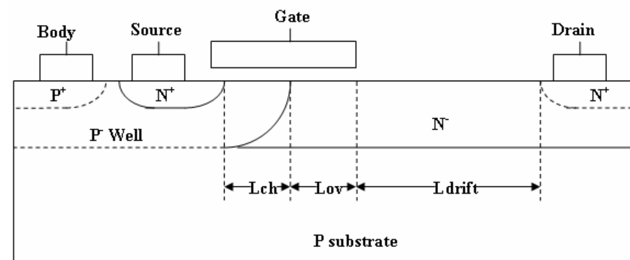


Figure 1: Typical LDMOS structure.

Figure 1 shows the typical N-channel LDMOS structure used in this study. Compared with conventional MOSFET devices, the LDMOS has the following unique features:

1. The channel length Lch of the LDMOS device is defined by the P-Well and N-Well formation, i.e. the P-Well underneath the gate.
2. The doping in the channel region is highly laterally non-uniform as a result of the existence of P-Well and N-Well regions.
3. There is a significant gate-to-drain overlap region Lov between the gate and the drain because of the overlaping between the gate and the N-Well region.
4. The LDMOS device is non-symmetric between the source and drain due to the introduction of drift

region Ldrift and the gate-to-drain overlap region Lov on the drain side only.

5. Vth of the LDMOS device mainly depends on the doping level of the channel region Lch, while the drain current is significantly modulated by the overlap region Lov and the drift region Ldrift on the drain side.
6. The unique LDMOS structure yields different device scaling effects as compared to that in standard CMOS devices

2.2 Non-uniform Channel Doping Effects

Due to the fact that the channel of LDMOS is formed by lateral diffuction of P-Well (for N-type LDMOS), channel doping is highly non-uniform in both lateral and vertical direction. This causes complicated capacitance behavior of the channel region. At Vds=0, When Vgs increases from sub-threshold region to above threhold region, drain end of the channel will be inverted before source channel part, due to the fact that drain side doping level is lower than source side. This part of channel charge contributes completely to Cgd. As Vgs increases further, source end of the channel is inverted as well. Then channel charge will be partitioned to both source side and drain side. The change of partition of channel charge to drain side or source side has effect on Cgd and Cgs behavior during the transition. Specifically, this two stages inversion results in the increase of Cgd at early stage, and then drop of Cgd as well as increase of Cgs in second stage. So, properly modeling of the lateral non-uniform doping effect is important in accurate predicting Cgd/Cgs behavior.

To model the lateral non-uniform doping effect in LDMOS, position dependent Vth is introduced as:

$$V_{th}(x) = V_{fb}(x) + \phi_b(x) + \frac{\sqrt{2qN_{ch}(x)\varepsilon_{xi}\phi_b(x)}}{C_{ox}} \quad (1)$$

In which, lateral channel doping Nch(x) is assumed to be Gauss distribution:

$$N_{ch}(x) = N_S \times \exp\left(-\frac{x^2}{4x_0}\right) \quad (2)$$

Where N_S is doping concentration at source end of the channel and x_0 is characteristic length.

2.3 Overlap Capacitance Modeling

As shown in Figure 1, there is a significant gate-to-drain overlap region near the drift region at the drain side. This reduces the electric field near the boundary of the drain and the channel at high Vds biases. Physically, the LDMOS near the drain side is more like a depletion-mode N-channel MOSFET which is always in series with another enhancement-mode N-channel MOSFET in the channel region.

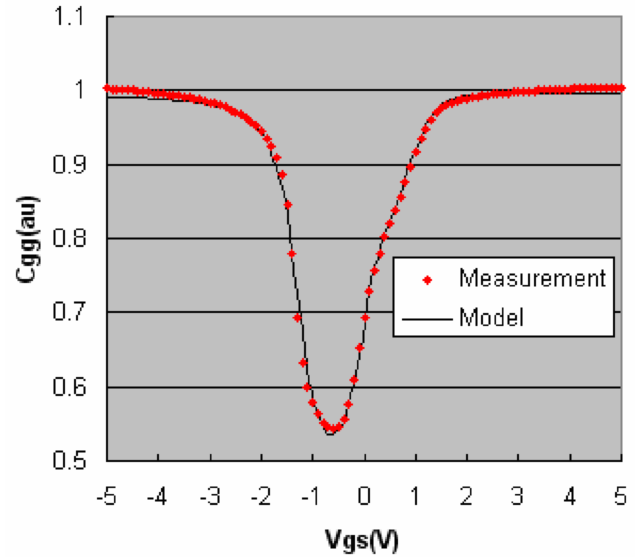


Figure 2: The two stages curve in Cgg near threshold region. Symbols are measurements and line is model result

In this paper, it is proposed to use a P-channel MOSFET structure to model the capacitance in the overlap region near the drain side. This P-channel MOSFET is also in series with the same enhancement-mode N-channel MOSFET in the channel region. In this approach, the accurate capacitance modeling of Cgd under negative Vgd bias is then achieved, since this is important for transient simulation of LDMOS switching from off-state to on-state. Consequently, the channel region of the device is mainly controlled by Vgs, while the overlap region of the device is mainly controlled by Vgd. In off-state, the channel region is in accumulation or depletion, while the overlap region is in inversion or depletion, depending on the relative voltage difference between the gate and the drain. It is worth mentioning that the inversion charge of the overlap region under a negative Vgd bias should also be associated with the body node, since they are electrically connected with the accumulation layer or depletion layer of the body. As Vgs further increases, the channel region goes from depletion to inversion, while the overlap region starts from inversion, through depletion to accumulation, as the drain side voltage usually decreases as the Vgs increases above the threshold voltage. At this time, the depletion and accumulation charges in the overlap region should be associated to the drain, since those charges are electrically connected through the drift region.

Because of the overlap capacitance, Cgg curve could have a step-like shape near the threshold region. As shown in Figure 2, Cgg curve near the threshold region exhibits two stages with the first one contributing from the overlap capacitance and the second one resulting from the channel region.

2.4 Distributed RC Network Effect Due to Non-Symmetry of LDMOS

Yet another important unique issue in LDMOS capacitance modeling is the distributed RC network effect due to the non-symmetry of the device structure.

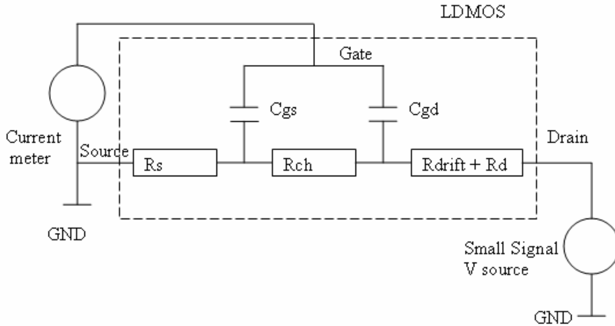


Figure 3: AC equivalent circuit to illustrate RC network effect on LDMOS capacitance measurement and modeling

Figure 3 gives the AC equivalent circuits for LDMOS Cgd measurement. During measurement, a small signal is applied to drain side, and the gate current is measured, then Cgd is calculated from the measured gate current and the voltate amplitude and phase of the small signal applied on drain side. As shown in figure 3, the Cgd value got in real measurement is not the actual Cgd value provided in model. Instead, it is an effective one given by:

$$C_{gd}^{eff} = \frac{R_{ch} + R_s}{R_{total}} \times C_{gd} + \frac{R_s}{R_{total}} \times C_{gs} \quad (3)$$

And:

$$C_{gs}^{eff} = \frac{R_{ch} + R_{drift} + R_d}{R_{total}} \times C_{gs} + \frac{R_{drift} + R_d}{R_{total}} \times C_{gd} \quad (4)$$

In which:

$$R_{total} = R_s + R_{ch} + R_{drift} + R_d \quad (5)$$

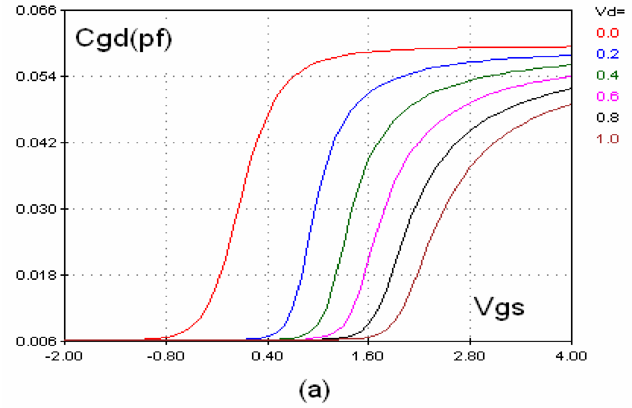
In symmetric MOSFET devices, there is no R_{drift}, and $R_s = R_d$. At zero Vds bias $C_{gd} = C_{gs}$ holds. From equation (3) and (4), we can get:

$$C_{gd}^{eff} = C_{gd} \quad (6)$$

And:

$$C_{gs}^{eff} = C_{gs} \quad (7)$$

However, in non-symmetric devices like LDMOS, such a condition doesn't hold true any more even at zero Vds bias. Careful considerations need to be given when modeling the Cgd/Cgs characteristics so that the models can fit measurement data accurately and physically. Figure 4 gives various Cgd curves with and without the drift region resistance involved.



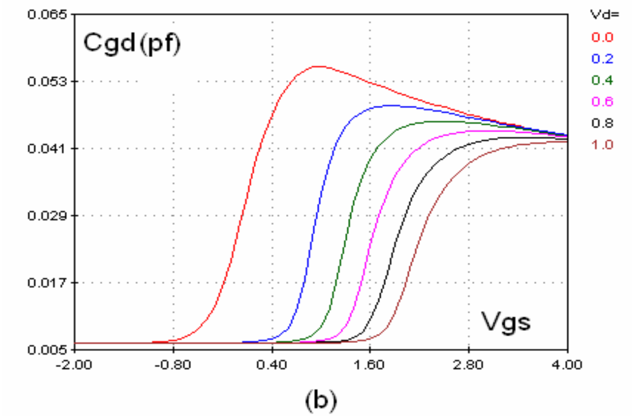


Figure 4: Cgd simulation results for (a) without the drift region resistance and (b) with the drift region resistance.

2.5 Model Scalability

A good capacitance model should be able to fit into a variaty of data for the devices with various structures and geometries. This requires good scalability for the model.

Since LDMOS channel is formed by lateral diffusion of well region, its channel length is usually the same for all devices in the same process. So, scalability of the model with the channel length is not as critical as that in standard MOSFET models. However, the width of channel region, overlap region and drift regions can vary as required by driving capability. Besides, in the LDMOS device design, the length of the overlap region is often optimized to achieve the best trade-off between breakdown voltage and device performance. Therefore, the scalability of the capacitance model with the width and length for the overlap region is very important. Although the drift region length and width seem not affecting the capacitance behaviors of LDMOS directly, it has important effects on the resistance in the drift region thus the capacitance behaviors through the RC network effect discussed in last subsection.

2.6 Model Validation

The present LDMOS model was further verified by the measurements of LDMOS devices.

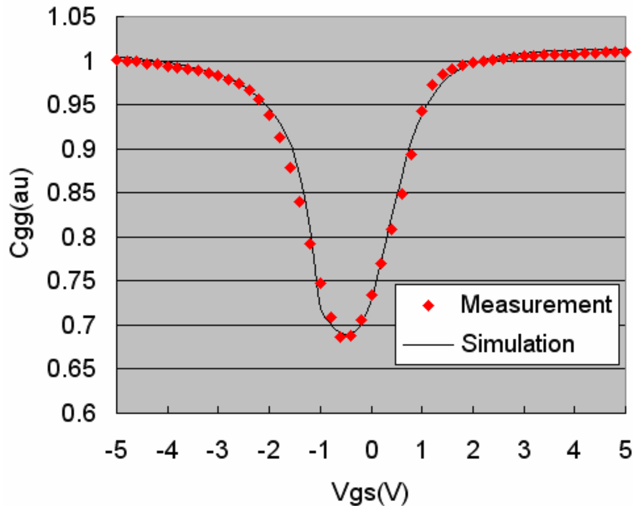


Figure 5: Model validation for Cgg: symbols are measurement data (arbitrary unit) and line is model result.

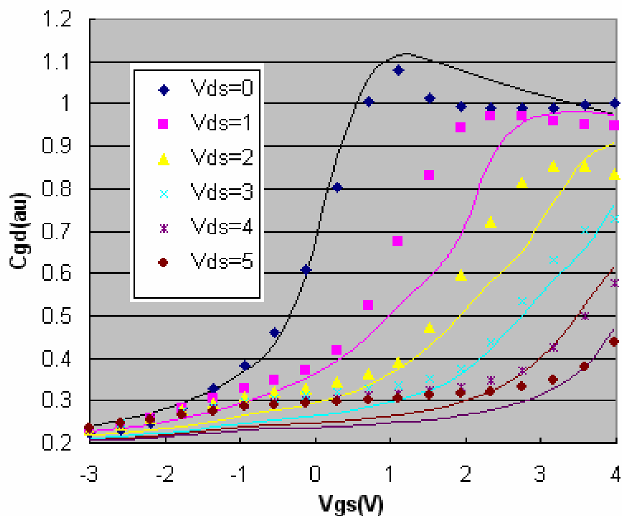


Figure 6: Model validation for Cgd: symbols are measurement data (arbitrary unit) and line is model result

Figure 5 shows another set of measured Cgg data compared with the model results. In this set of data, the two-stage Cgg curve near threshold region is not obvious. That is because that in this technology, the length of the overlap region of the LDMOS device is relatively smaller than the channel length. Comparing with the fitting results as shown in Figure 2, it can be seen that the present model can fit well for both devices with either long or short overlap region, which again demonstrates good scalability of the capacitance model.

Figure 6 gives the Cgd results for the same LDMOS device. It is shown that at zero Vds bias, the Cgd value drops after the device is turned on. This phenomenon is more profound than that at bigger Vds biases. This is expected since at higher Vds biases, the depletion region becomes deeper in the overlap region as well as in the channel region near the drain side. Therefore, Cgd contribution from the overlap region and the channel region near the drain side is weaker. It can be seen from Figure 6 that this phenomenon is well predicted by this capacitance model.

3 CONCLUSIONS

In this paper, LDMOS capacitance behaviors are presented. Special considerations necessary for an accurate capacitance modeling are analyzed. Laterally non-uniform channel doping is an important issue to be included in the compact capacitance model, which is unique for the LDMOS structures. The overlap region charge model is important for accurate prediction of Cgg and Cgd behaviors. Distributed RC network effects on LDMOS characterization and modeling are analyzed for the first time. Finally, scalability of the LDMOS model is discussed. Two stages in Cgg curve and drop in Cgd curve are well modeled. The accuracy and fitting capability of the model presented in this work are verified using measurement data.

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