

# Theory and Modeling Techniques used in the PSP Model

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## ABSTRACT

This paper describes theoretical foundation and details of the new compact modeling techniques used in the advanced surface-potential-based compact MOSFET model PSP, jointly developed by the Pennsylvania State University and Philips Research. Specific topics include surface potential equation, generalized symmetric linearization method and non-uniformity of the vertical impurity profile.

**Keywords:** MOSFET, compact model, surface potential, PSP model

## 1 Introduction

The PSP model is the advanced surface-potential-based model jointly developed by the Pennsylvania State University and Philips Research and selected by the Compact Modeling Council as a new standard MOSFET model for the next generation of MOSFETs. General features of the model and its verification for a variety of 180 nm, 130 nm and 90 nm processes have been discussed in [1–3]. The model has been also verified for 65 nm process. In this work we concentrate on the theory and modeling techniques used in the formulation of PSP.

## 2 Surface Potential

Surface potential,  $\psi_s$  is usually evaluated in the gradual channel approximation that consists of neglecting the lateral field gradient term in the Poisson equation. The resulting one-dimensional equation can be easily integrated in the case of a MOS capacitor where the electron's imref is position independent. However, integration of Poisson equation in MOS transistor cannot be performed exactly since the closed form expression for the positional dependence of the minority carrier imref is unavailable. Following the development of the first  $\psi_s$ -based model in the work of Pao and Sah [4], several alternative forms have been suggested for the Surface Potential Equation (SPE). All versions of the SPE reported in the literature can be written in the form

$$(V_{GB} - V_{FB} - \psi_s)^2 = \gamma^2 \phi_T \{ \exp(-u) + u - 1 + (n_b/p_b) k_n [\exp(u) - u - 1 - \chi(u)] \} \quad (1)$$

and differ by the choice of function  $\chi(u)$ . Here,  $\psi_s$  is referenced to bulk,  $\gamma$  is the body factor,  $\phi_T = k_B T/q$

is the thermal potential,  $V_{FB}$  is the flat-band voltage,  $u = \psi_s/\phi_T$ ,  $n_b$  and  $p_b$  denote the bulk concentrations of electrons and holes respectively, and  $k_n = \exp(-V_n/\phi_T)$ , where  $V_n$  is the so called channel voltage formally defined as the imref splitting normalized to  $q$ . The surface potential at the source side ( $\psi_{ss}$ ) and at the drain side ( $\psi_{sd}$ ) are then given implicitly by setting  $V_n$  equal to  $V_{SB}$  and  $V_{DB}$  respectively.

In the original formulation [4]

$$\chi(u) = u (k_n^{-1} - 1) . \quad (2)$$

The resulting SPE is still widely used today, but is problematic in the narrow gate bias region close to the flat-band voltage where the right hand side of (1) becomes negative. In [5–7] the problem was traced to the position dependence of the minority carrier imref not included in the original derivation of the SPE. Since at present it is impractical to include imref position dependence in the closed-form MOSFET model, most compact models (with the exception of SP [8] and PSP [1]) use empirical alternative form [5]

$$\chi(u) = 0 \quad (3)$$

free of the complications associated with (2). Before proceeding further, note that the modified SPE is neither more nor less physical than the original formulation and is selected for the sake of mathematical convenience. In this regard, it is useful to observe that only for  $V_n = 0$ , i.e. for  $k_n = 1$  (MOS capacitor) equation (1) becomes exact.

An important observation regarding the original SPE and its subsequent modifications is that these modifications do not appreciably affect the output device characteristics, transconductances and transcapacitances. Indeed, the term  $\chi(u)$  affects only minority carrier contribution to the surface field and (except for the narrow gate bias region near the flat-band voltage) is negligible until the inversion layer begins to form. But once it happens,  $\chi(u) \ll \exp(u)$  and is insignificant once again (see [6] for further details). Hence, to some extent, one can select the function  $\chi(u)$  in a way most convenient for the compact model development. For example, it is possible to impose an additional condition  $\partial \psi / \partial V_{GB} = 0$  for  $V_{GB} = V_{FB}$ , where  $\psi = \psi_{sd} - \psi_{ss}$  is the surface potential variation across the channel. This allows one to set  $\psi = 0$  in the accumulation region  $V_{GB} \leq V_{FB}$  without loss of continuity.

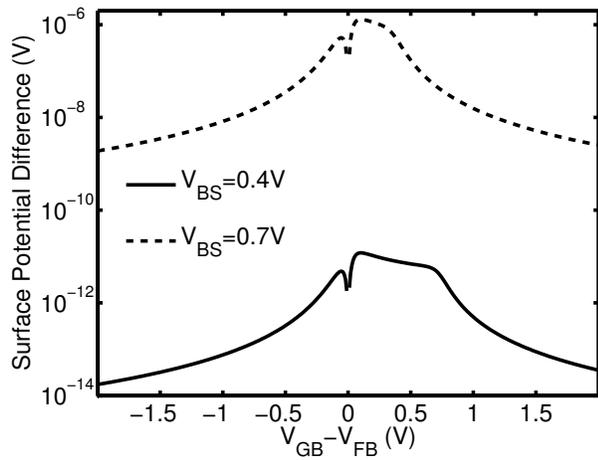


Figure 1: The difference in surface potentials calculated numerically from Eq. (3) and Eq. (4), for  $V_{BS} = 0.4$  V and 0.7 V.  $N_{SUB} = 5 \cdot 10^{17} \text{ cm}^{-3}$  and  $t_{ox} = 2$  nm.

One possible choice of  $\chi(u)$  that accomplishes this [9] is adopted in PSP:

$$\chi(u) = u^2 / (u^2 + 2) . \quad (4)$$

To the model user the change from (3) to (4) is invisible, since both forms produce identical device characteristics.

The surface potentials computed numerically for two choices of  $\chi(u)$  are presented in Fig. 1. The results confirm that the choice of  $\chi(u)$  has negligible effect on the device characteristics and is a matter of convenience. Only the results for forward biased source-substrate junctions are presented since for  $V_n \leq 0$  the difference is totally negligible. As far as the actual computation of the surface potential is concerned, PSP uses advanced non-iterative algorithm replacing that developed for the SP model [8] and having the advantage of remaining valid for high forward biases [9,10]. Typical results shown in Fig. 2 indicate the accuracy of better than 1 nV for forward biases up to 0.85 V. Naturally, this accuracy figure applies to the case when both numerical (“exact”) solution and analytical approximation use the same form of  $\chi(u)$  given by Eq. (4). Adaptation of this approximation to SPE with  $\chi(u)$  given by (3), yields similar results shown in Fig. 3. Analytical algorithm is adopted in PSP in order to eliminate the internal iterative loops and corresponding convergence issues.

One advantage of the surface-potential-based formulation is an accurate reproduction of  $g_m/I_d$  ratio. Typical results for two corners of the 90 nm based technology are shown in Figs. 4 and 5. In addition, as shown in Fig. 6, PSP model accurately reproduces higher order transconductances  $g_m^{(i)} = \partial^i I_{DS} / \partial V_{GS}^i$  that are important in advanced analog and RF designs.

### 3 Symmetric Linearization

Linearization of the bulk charge as a function of the voltage drop in the channel or as a function of the surface

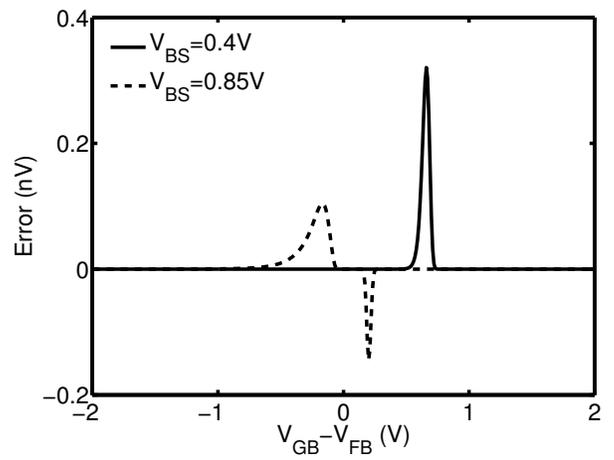


Figure 2: The error in surface potential calculated from analytical approximation developed for Eq. (4);  $N_{SUB} = 5 \cdot 10^{17} \text{ cm}^{-3}$  and  $t_{ox} = 2$  nm.

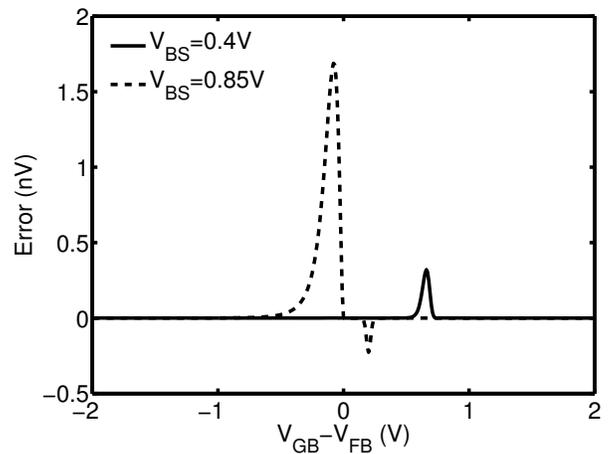


Figure 3: The error in surface potential calculated from analytical approximation developed for Eq. (3);  $N_{SUB} = 5 \cdot 10^{17} \text{ cm}^{-3}$  and  $t_{ox} = 2$  nm.

potential is a common feature of all advanced MOSFET models enabling relatively simple expressions for the terminal charges suitable for use in circuit simulations. Traditional implementations of this technique are known to violate essential symmetry of the device model with respect to the source-drain interchange. To overcome this problem, PSP relies on symmetric linearization method (SLM), in a form developed in [11,12] that is particularly suitable for the  $\psi_s$ -based formulation of compact MOSFET model. SLM as developed in [11,12] does not include the velocity saturation effects. The latter was included in [8] within the SP model context. Other versions of SLM were also used in [13] and [14]. In the PSP model the description of velocity saturation follows that of MM11 [15] and is particularly suitable for the analysis of harmonic distortion in RF applications. This requires reproduction of higher order drain conductances shown in Fig. 7. Hence it became necessary to formulate SLM in a way that is compatible with the velocity saturation

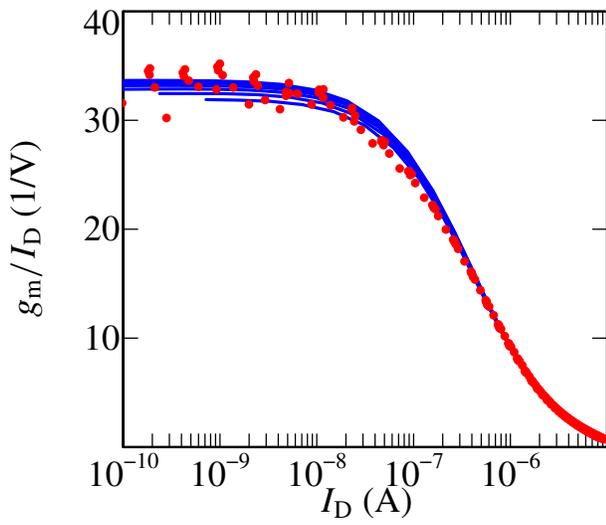


Figure 4:  $g_m/I_D$  versus drain current for  $V_{DS} = 0.025$  V,  $V_{BS} = 0$  to  $-1.2$  V, and  $V_{GS} = 0$  to  $1.2$  V,  $T = 25$  °C and  $W/L = 10$   $\mu\text{m}/10$   $\mu\text{m}$ ;  $n$ -channel MOSFET. Solid lines represent PSP and symbols correspond to the test data.

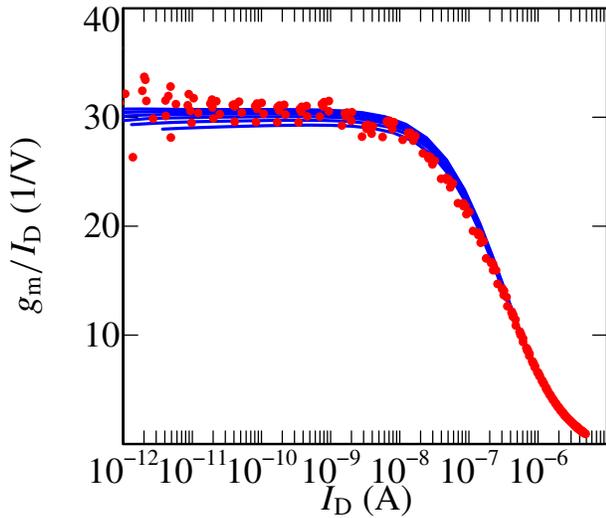


Figure 5:  $g_m/I_D$  versus drain current for  $V_{DS} = 0.025$  V,  $V_{BS} = 0$  to  $-1.2$  V, and  $V_{GS} = 0$  to  $1.2$  V,  $T = 25$  °C and  $W/L = 0.12$   $\mu\text{m}/0.1$   $\mu\text{m}$ ;  $n$ -channel MOSFET. Solid lines represent PSP and symbols correspond to the test data.

model used in [14–16]. This is done as follows. The fundamental approximation for the inversion charge density  $q_i$  per unit channel area remains unchanged:

$$q_i = q_{im} - \alpha(\psi_s - \psi_m), \quad (5)$$

where  $\alpha$  denotes linearization coefficient,  $q_{im}$  is the inversion charge density at the surface potential midpoint, and  $\psi_m = (\psi_{ss} + \psi_{sd})/2$ . The drain current becomes

$$I_{DS} = \frac{\mu_{\text{eff}} W q_{im}^*}{\sqrt{1 + (E_y/E_c)^2}} \frac{d\psi_s}{dy}, \quad (6)$$

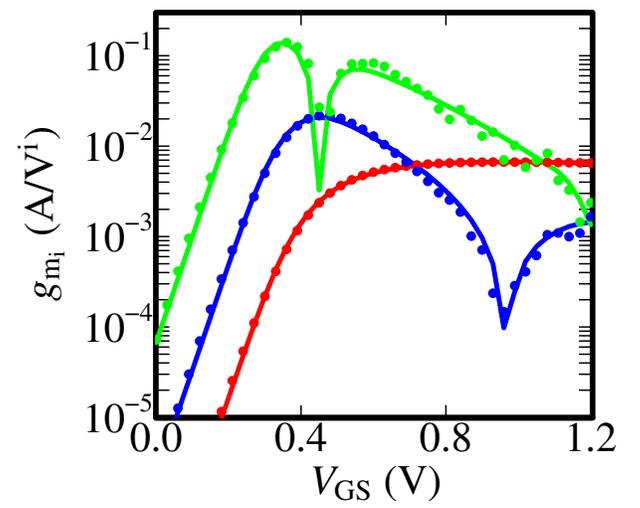


Figure 6: Higher order transconductance  $g_{m_i}$  versus gate-source bias for  $V_{DS} = 1.2$  V,  $V_{SB} = 0$  V,  $T = 25$  °C and  $W/L = 10$   $\mu\text{m}/0.12$   $\mu\text{m}$ ;  $n$ -channel MOSFET;  $i = 1$  (lower curve),  $2$  (middle curve) and  $3$  (upper curve). Solid lines represent PSP and symbols correspond to the test data.

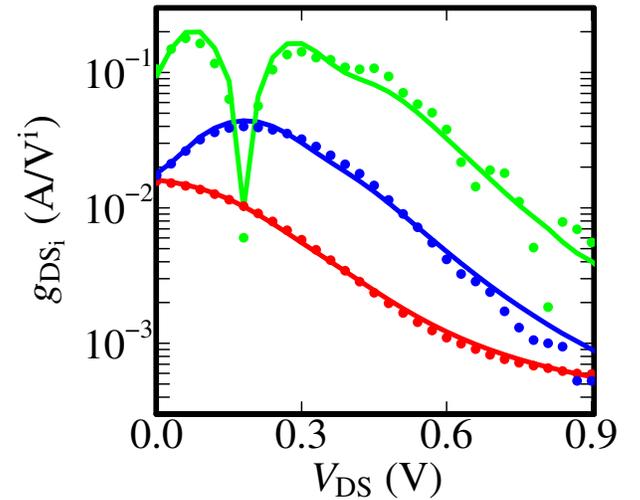


Figure 7: Higher order conductances  $g_{DS_i}$  versus drain-source bias for  $V_{GS} = 1.2$  V,  $V_{SB} = 0$  V,  $T = 25$  °C and  $W/L = 10$   $\mu\text{m}/0.12$   $\mu\text{m}$ ;  $n$ -channel MOSFET;  $i = 1$  (lower curve),  $2$  (middle curve) and  $3$  (upper curve). Solid lines represent PSP and symbols correspond to the test data.

where  $\mu_{\text{eff}}$  is the effective mobility,  $W$  is the channel width,  $E_y$  is the lateral electric field,  $E_c = v_{\text{sat}}/\mu_{\text{eff}}$  and  $q_{im}^* = q_{im} + \alpha\phi_T$ . Following the analysis in [14–16]

$$I_{DS} dy = \mu_{\text{eff}} W q_i - \frac{I_{DS}^2}{2W^2 v_{\text{sat}}^2 q_i} d\psi_s. \quad (7)$$

After integration,

$$I_{DS} = \mu_{\text{eff}} \frac{W}{L} \psi \left( \bar{Q} - \frac{I_{DS}^2}{2W^2 v_{\text{sat}}^2 \bar{Q}} \right), \quad (8)$$

where  $L$  is the channel length,

$$\bar{Q} = \frac{1}{\psi} \int_{\psi_{ss}}^{\psi_{sd}} q_i d\psi_s \quad (9)$$

and

$$\bar{Q} = \psi \left( \int_{\psi_{ss}}^{\psi_{sd}} \frac{d\psi_s}{q_i} \right)^{-1}. \quad (10)$$

In symmetric linearization method, according to (5), (9),  $\bar{Q} = q_{im}$ . For the sake of simplicity, we follow [14] and set  $\bar{Q} = \bar{Q}$ . This approximation, as well as the one involved in obtaining (7) from (6) is responsible for the empirical bias dependence of saturation velocity included in PSP.

Solving (8) with respect to  $I_{DS}$  yields

$$I_{DS} = \frac{\mu_{eff}}{G_{vsat}} \frac{W}{L} q_{im}^* \psi, \quad (11)$$

where

$$G_{vsat} = \frac{1}{2} \left[ 1 + \sqrt{1 + 2(\theta_{sat} \psi)^2} \right] \quad (12)$$

and  $\theta_{sat} = \mu_{eff}/(v_{sat} L)$ . For p-channel transistor (11), (12) remain valid but with

$$\theta_{sat} = \frac{\mu_{eff}}{v_c L \sqrt{1 + \mu_{eff} \psi / (Lv_c)}}. \quad (13)$$

Apart from leading to a relatively simple expression for the drain current, SLM yields an explicit form of the  $\psi_s(y)$  dependence:

$$\psi_s(y) = \psi_m + H \left[ 1 - \sqrt{(2 \psi / HL)(y - y_m)} \right], \quad (14)$$

where  $y_m = \frac{L}{2} \left( 1 + \frac{\phi}{4H} \right)$  and

$$H = \frac{q_{im}^*}{(\alpha G_{vsat})} \left[ 1 + \frac{1}{2} \frac{\theta_{sat} \psi}{G_{vsat}} \right]^2. \quad (15)$$

Comparison with [11] and [8] indicates that the functional form of the  $\psi_s(y)$  dependence is not sensitive to the details of the velocity field dependence, which only enters through the position-independent variable  $H$ .

The verification of the SLM has been performed in [11] and [12] by comparison with the charge-sheet model (CSM) [17] for the worst case scenario of long-channel MOSFET. Here we extend the verification by comparing symmetrically linearized CSM directly with Pao-Sah model. The results shown in Fig. 8 indicate the accuracy of symmetrically linearized CSM as computationally efficient representation of Pao-Sah model.

Application of SLM to MOSFET charge model has been discussed previously. In particular, it leads to complete symmetry of the charge sheet model with respect to the source-drain interchange. Here we point out that PSP charge model satisfies reciprocity conditions  $C_{GB} = C_{BG}$  and  $C_{GD} = C_{DG}$  for the special case of  $V_{DS} = 0$ . Typical results shown in Fig. 9 serve as further validation of the symmetric linearization method. The slight

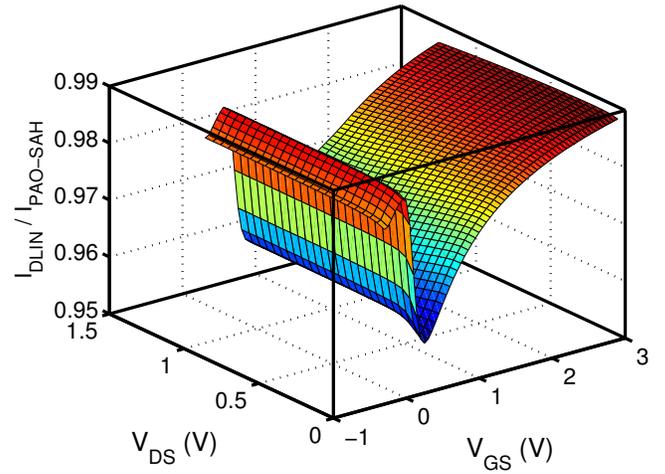


Figure 8: Ratio of drain currents for symmetrically linearized CSM  $I_{DLIN}$  and Pao-Sah model  $I_{PAO-SAH}$  for  $V_{BS} = 0$  V,  $T = 27^\circ\text{C}$ ,  $W/L = 2$ ,  $t_{ox} = 2$  nm,  $N_{SUB} = 5 \cdot 10^{17}$  cm<sup>-3</sup>,  $\mu = 400$  cm<sup>2</sup>/s,  $V_{FB} = -1$  V.

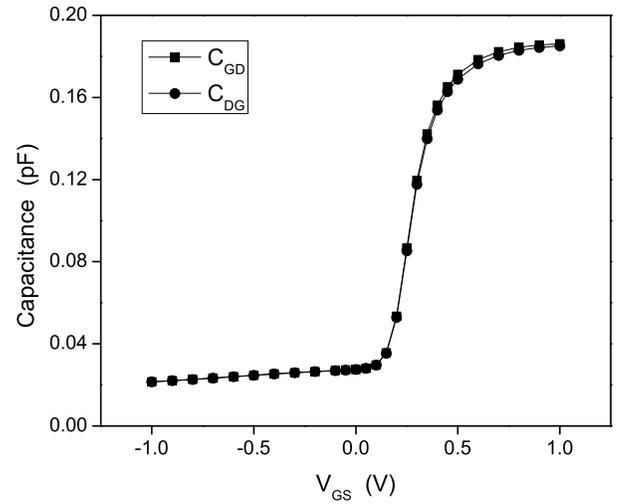


Figure 9: Gate bias dependence of  $C_{GD}$  and  $C_{DG}$  for  $W/L = 10 \mu\text{m}/2 \mu\text{m}$  and  $t_{ox} = 1.5$  nm

difference between  $C_{GD}$  and  $C_{DG}$  in the strong inversion region is produced by the charge-sheet approximation (cf. [16]) and is inconsequential for the model applications.

## 4 Retrograde Profile

There is presently considerable interest in MOSFETs with the so called “retrograde” doping profile in the direction normal to the Si/SiO<sub>2</sub> interface. Conceptually, the problem is well understood and can be reduced to computing the surface potential as a function of the gate bias in a vertically non-uniformly doped device. A simplified method of modeling of the non-uniformly doped MOS devices using bias dependent “effective” doping has been considered in [18] and in a more complete form

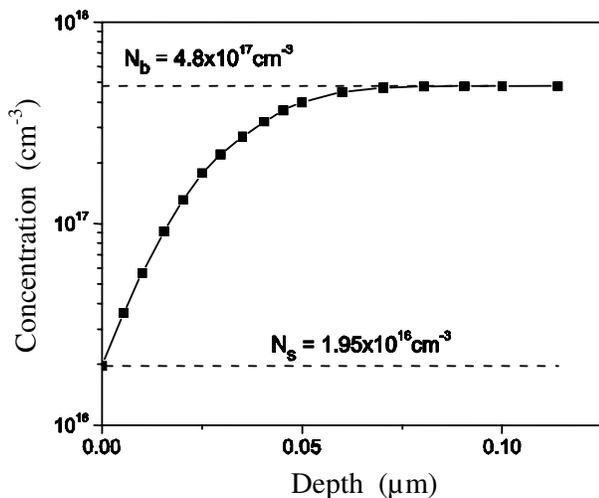


Figure 10: Retrograde doping profile.

in [19]. It still requires extensive computations that are not conducive to circuit design applications.

In [20] a more powerful method has been developed in which the actual profile is approximated by a step function leading to analytical expression for the effective impurity concentration as a function of surface potential. Further applications of this technique were reported in [21] and [22]. An important advantage of the approach taken in [20] is that the problem of modeling the vertical impurity profile non-uniformity is decoupled from other short-channel effects and is presented in a form that does not necessarily assume that the surface potential is pinned at twice the bulk potential level.

This method is, however, not directly applicable to  $\psi_s$ -based models. Indeed, such models are invariably based on the first integral of the Boltzmann-Poisson equation that is solved under assumption that the impurity concentration does not depend on the surface potential [4]. This section contains a new version of the method developed in [20] that has the same physical content but is compatible with the  $\psi_s$ -based approach.

A typical retrograde impurity profile is shown in Fig. 10 [23]. The surface ( $N_s$ ) and bulk ( $N_b$ ) concentrations differ by an order of magnitude so that the effect of the non-uniform doping on  $C(V)$  characteristics is pronounced and is readily seen in Fig. 11. In particular, using uniform impurity profile with either  $N_{SUB} = N_s$  or  $N_{SUB} = N_b$  results in  $C(V)$  curves that differ significantly from the  $C(V)$  curve obtained by numerical solution of Poisson equation with the non-uniform impurity distribution shown in Fig. 10.

A better result is achieved by still considering MOS capacitor with bias-independent uniform doping density but using least square fit to select the optimal value of  $N_{SUB}$  denoted as  $N_{opt}$ . Nevertheless, even in this case the difference between the actual  $C(V)$  curve and that of the uniformly doped capacitor is greater than what is acceptable in modern compact models. The essential physics of the problem is the increase of the width of

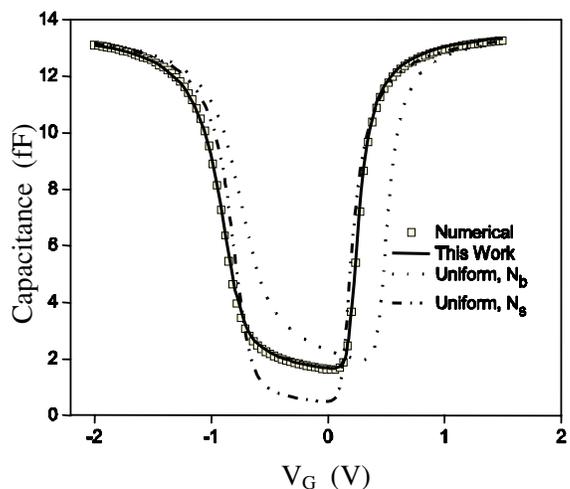


Figure 11: Capacitance-Voltage characteristics for different impurity profiles; oxide thickness  $t_{ox} = 2.5$  nm.

the space-charge region with the gate bias  $V_G$ . For the retrograde impurity profile, this implies the increase of the doping concentration at the edge of the space-charge region. Hence, it is plausible that the effect of the non-uniformity can be modeled by introducing the fictitious gate bias dependence of the substrate doping. In other words, instead of the actual device with position dependent doping, we substitute the uniformly doped capacitor, but with the doping level  $N_{SUB} = N(V_G)$  which is an increasing function of the gate bias. For such a capacitor the surface potential is determined from (1), but with  $\gamma = \gamma(V_G)$  for the body factor.

While computing the surface potential corresponding to a given bias  $V_G$ , inclusion of the  $\gamma(V_G)$  dependence is inconsequential:  $N_{SUB}(V_G)$  and  $\gamma(V_G)$  are fixed. This analysis also makes it clear why  $N_{SUB}(\psi_s)$  dependence obtained in [20] is difficult to use directly in the  $\psi_s$ -based models. Indeed, while the underlying physics is well reproduced by either  $N_{SUB}(\psi_s)$  or  $N_{SUB}(V_G)$  description, only the latter allows one to retain the well-developed solution methods for the surface potential equation (1).

It remains to demonstrate the accuracy of the proposed approach. A particular form of the bias dependence of the effective doping used in this study is given by [1, 10]

$$N_{SUB} = N_0 \left[ 1 + \frac{D_N}{2} \left( V_G - V_N + \sqrt{(V_G - V_N)^2 + \epsilon} \right) \right] \quad (16)$$

As shown in Fig. 12, expression (16) describes the gradual increase of the effective doping with the applied voltage motivated by physical consideration. Parameters  $N_0$ ,  $D_N$ ,  $V_N$  and  $\epsilon$  are selected by the least square fit to the numerically evaluated  $C(V)$  characteristic. As shown in Fig. 11, the result is an accurate reproduction of the MOS  $C(V)$  curve. This justifies the use of a particular form of the  $N_{SUB}(V_G)$  dependence given by (16). More complex forms of the  $N_{SUB}(V_G)$  dependence may be introduced as well, including the upper limit of the effective doping.

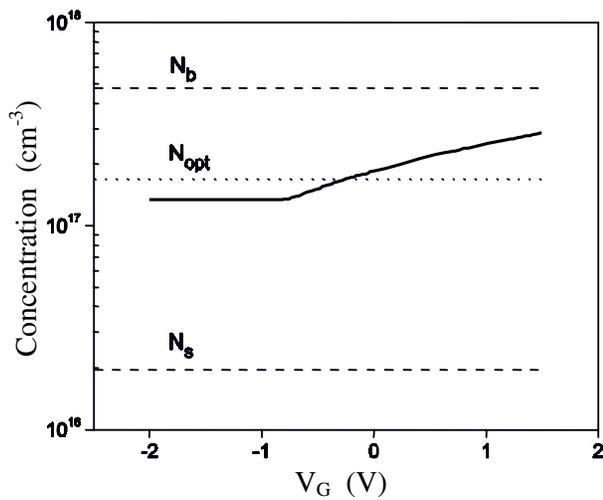


Figure 12: Gate bias dependence of the effective substrate impurity concentration;  $N_0 = 1.35 \cdot 10^{17} \text{ cm}^{-3}$ ,  $D_N = 0.5$ ,  $V_N = -0.75 \text{ V}$ ,  $\varepsilon = 0.001$ . Solid line represents Eq. (16).

## 5 Conclusion

We have presented some of the theory and modeling techniques that have led to the development of the PSP model. New solutions of several long-standing problems of compact modeling allow one to expand physical content of the model without prohibitive increase in the computational complexity. In particular, symmetric linearization method is reformulated to include different forms of velocity-field dependence used in the compact modeling applications. Further details are presented in [3, 10, 24].

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