A computationally efficient method for analytical calculation of potentials in undoped symmetric DG SOI MOSFET

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ABSTRACT

In order to build an analytical model of an undoped symmetric DG SOI MOSFET devices, an accurate but rather difficult method was used by S. Malobabic et.al. [1]. In that paper, the authors have used a complicated Lambert function for the potential calculation and smoothing parameters without physical meaning. Starting from their model, the purpose of this paper is to show an original, simple and efficient analytical method for the computation of electrostatic potentials of the silicon film of such MOSFET novel device as a function of the gate to source voltage. Then, the total channel carrier charge will be computed from the silicon surface potential solution. Results from our proposed model will be compared to those obtained in the literature.

Keywords: DG SOI MOSFET, analytical modeling, silicon electrostatic potential

1 INTRODUCTION

In the last few decades, the CMOS devices and their technologies have been scaling down continuously until the short channel effects limited device performances as follows [2]: 1. band to band tunneling current increased in source/substrate and drain/substrate junctions, 2. leakage currents increase due to drain induced barrier lowering (DIBL), 3. increased gate induced drain leakage, 4. increased direct tunneling current from the gate to the substrate through the gate oxide. In this context the double-gate SOI MOSFET appeared as a promising alternative solution to the above device drawbacks. This new device are characterized by the following attractive features in terms of [3]: 1) light doping of the channel reducing the mobility degradation due to elimination of impurity scattering; 2) good control of short channel effects because of reduced influence of the drain voltage on the channel charge; 3) ideal subthreshold slope due to elimination of substrate doping; 4) increased electrostatic control due to gate voltage applied on both sides; 5) increased current drive capability due to volume inversion [4] of the entire silicon film. However, some challenges still exist for the application of DG SOI MOSFET in novel circuits due to 3D technological complexity and ultra thin silicon film needed for the associated SOI transistor fabrication.

Another important aspect concerning the development of next generation of CMOS devices consists of the continuation of the efforts to the understanding and modeling of the behavior of DG MOSFET devices. Due to the low doping in the silicon substrate [4], the Maxwell-Boltzmann statistics can be used for the evaluation of the charge carriers. For the first time, Y. Taur [5] has proposed the analytical calculation of Poisson's equation in the silicon film where only one type of mobile charge is present. Thus, he has solved the Poisson's equation, considering only mobile electrons in the channel. An important step in the analytical modeling of DG SOI MOSFET has been done by S. Malobabic et.al. [1] where the influence of the applied voltage along the channel on the mobile charge in the silicon film is introduced. In their paper, the Lambert function has been used for the calculation of the surface electrostatic potential in the silicon. Unfortunately, their approach is mathematically very complicated and uses smoothing parameters without physical meaning.

The main target of our paper is to introduce a simple method for the calculation of that surface electrostatic potential in silicon film and, thus, making unnecessary the application of Lambert function in a symmetrical DG SOI MOSFET device. Our approach consists of the calculation of the Poisson's equation and associated boundary conditions which is leading to a transcendental equation for the derivation of electrostatic potential in the center of the silicon film. Having known the electrostatic potential in the center of the film, one can easily calculate the sheet density of electrical charge carrier in the silicon.

2 GENERAL CONCEPTS

Figure 1 shows an undoped symmetric Double Gate SOI MOSFET structure which will be one-dimension ($1D$) analytically analyzed, in this paper. As it is depicted in the picture, the current flows only on the y direction, the one on the x direction being neglected. The novel device presents the symmetry property, according to which both gates have the same work function, oxide thickness and the same applied voltage on their terminals.

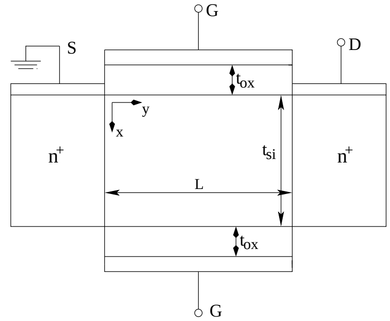

Figure 1: Double Gate SOI MOSFET structure.

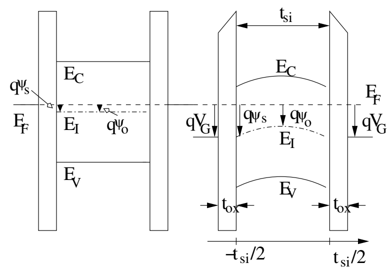

Figure 2: Diagram bands of DG SOI MOSFET.

Figure 2a depicts the corresponding energy bands diagram of DG SOI MOSFET at thermal equilibrium in which the Fermi level is maintained constant along the vertical direction (x direction) due to the consideration of midgap electrode (Fermi level of the gate electrode falls in the middle of the silicon bandgap) and no voltage is applied on the dual gate transistor. In addition, no electric current is flowing on the x direction. The Figure 2b represents the energy band diagram when a gate voltage is applied with the effect of the bands bending on both sides of silicon film. One can see that a part of the gate voltage falls on the gate dielectric. In the absence of the drain-source voltage, there is no current in the structure and the Fermi level remains constant in the whole structure but becomes closer to the silicon conduction band and, thus, the entire silicon film volume is in the inversion. The above assumption of volume inversion has been proved, for the first time, by Balestra and Cristoloveanu [4].

Another hypotheses model is the fact that the silicon film is thick enough so that the quantum confinement effects are not taken into account. As shown above, as silicon film is nearly intrinsic the Maxwell-Boltzmann statistics is used for the charge carriers evaluation in silicon.

In agreement with the above assumptions and when the minority carriers (holes) are neglected due to volume inversion supposition, the starting point of the analytical model consists of calculation of Poisson's equation as in [5], [1]:

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\varepsilon_{si}} \cdot e^{\frac{q\psi}{kT}} \quad (1)$$

with the following boundary conditions:

$$\frac{d\psi}{dx}|_{x=0} = 0 \quad (2)$$

$$V_{GS} - V_{FB} = \psi|_{x=\frac{t_{si}}{2}} + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \cdot \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}} \quad (3)$$

where: Ψ represents the electrostatic potential in the silicon body, V_{FB} is the flat-band voltage, V_{GS} - gate to source voltage, t_{si} - silicon thickness, t_{ox} - oxide thickness ($2nm$ throughout the paper), ε_{si} - electrical permittivity of the silicon, ε_{ox} - electrical permittivity of the silicon dioxide, k - Boltzmann constant, T - temperature, n_i - intrinsic charge carrier concentration of silicon.

The boundary condition (2) shows the idea of the maximum electrostatic potential present in the central part of silicon film, while the boundary condition given by relation (3) is the continuity of the normal electrical displacement at the interface between silicon and SiO_2.

From the first integration of Poisson's equation, one can derive the electric field in silicon film:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{si}} \cdot [e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}]} \quad (4)$$

and the electrostatic potential is computed by making the second integration of it:

$$\psi(x) = \psi_0 - \frac{2kT}{q} \cdot ln[\cos(b \cdot e^{\frac{q\psi_0}{2kT}} \cdot x)] \quad (5)$$

while the amount b is: $\quad$ b $= \sqrt{\frac{q^2 n_i}{2\varepsilon_{si} kT}}$ and ψ_0 represents the electrostatic potential at the central point of silicon body.

When $x = \frac{\pm t_{si}}{2}$ and by using the relation (5), the electrostatic potential at the surface of silicon film (ψ_s) is derived:

$$\psi_s = \psi_0 - \frac{2kT}{q} \cdot ln\{\cos[b \cdot e^{\frac{q\psi_0}{2kT}} \cdot \frac{t_{si}}{2}]\} \quad (6)$$

Also, at the surface of the silicon body, the electric field, is given by (4) replacing x with $\frac{\pm t_{si}}{2}$. Thus, from the second boundary condition (3), an important equation related to the applied gate voltage and the electrostatic potential is computed:

$$V_{GS} - V_{FB} = \psi_s + \frac{\varepsilon_{si} t_{ox}}{\varepsilon_{ox}} \cdot \sqrt{\frac{2kTn_i}{\varepsilon_{si}} \cdot [e^{\frac{q\psi_s}{kT}} - e^{\frac{q\psi_0}{kT}}]} \quad (7)$$

Because we consider midgap electrode, $V_{FB} = 0V$ throughout the paper.

In addition, the sheet density of mobile charge can be calculated by using the surface silicon electrostatic potential:

$$Q = 2 \cdot \varepsilon_{si} \frac{d\psi}{dx}|_{x=\frac{t_{si}}{2}} \qquad (8)$$

3 DESCRIPTION OF OUR METHOD AND RESULTS

Our method consists of the determination of the electrostatic potential in the center of silicon body by means of the relations (6) and (7) as follows. We introduce the potential ψ_s in the relation (7) and we get a transcendental equation that relates the applied gate-to-source voltage and electrostatic potential in the middle of the silicon film as it is written below:

$$V_{GS} - \psi_0 = a \cdot e^{\frac{q\psi_0}{2kT}} \cdot |\tan(y)| - \frac{2kT}{q} \cdot ln\{\cos(y)\} \qquad (9)$$

where the amounts a and y are:

$$a = \frac{t_{ox} \cdot \sqrt{2\varepsilon_{si} kT n_i}}{\varepsilon_{ox}}; \quad y = b \cdot e^{\frac{q\psi_0}{2kT}} \cdot \frac{t_{si}}{2} \qquad (10)$$

By analyzing the relation (9), we see that there are some limitations in the variation of ψ_0 electrostatic potential introduced by the definition domain of the functions involved in that transcendental equation. Thus, from the condition of the existence for the logarithm function ($cos(y) > 0$) we get the variation domain for y amount which is $y \in [-\frac{\pi}{2}; +\frac{\pi}{2}]$. From the definition of the amount y, we can easily observe that the variation of y is in $y \in [0; +\frac{\pi}{2}]$. If we consider the fact that we work with positive electrostatic potentials (n channel DG SOI MOSFET), then we obtain the following variation range for ψ_0:

$$\psi_0 \in (0; \psi_{0m}]; \qquad (11)$$

where ψ_{0m} is derived for $y = +\frac{\pi}{2}$. Making these calculations, we obtain the following equation for ψ_{0m}:

$$\psi_{0m} = \frac{2kT}{q} \cdot ln(\frac{\pi}{t_{si} \cdot b}) \qquad (12)$$

As an example, for $t_{si} = 20nm$ and the room temperature $T = 300K$, we get $\psi_{0m} = 0.462V$, while for $t_{si} = 5nm$, we obtain $\psi_{0m} = 0.5341V$.

It is worth to note that the maximum electrostatic potential in center of the silicon body depends on the thickness of the silicon film and does not depends on the applied gate-to-source voltage.

By solving the equation (9), we can obtain the value of the electrostatic potential at the middle of silicon film for each applied gate-to-source voltage. By considering the variation domain for ψ_0 in the range $(0; \psi_{0m}]$, from equation (9) one can obtain the variation domain for V_{GS}. In our case, we have chosen for V_{GS} value ranging from $0.2V$ to $1.5V$ in order to assure that only electrons play a role in a Poisson's equation, on one hand, and, on the other hand, to let V_{GS} to be much higher than the threshold voltage for a good current drive of the DG SOI MOSFET transistor.

At this point, because the limits of both gate-to-source voltage and electrostatic potential in the middle of the silicon film are found, the transcendental equation (9) is solved with graphical method. For that matter, the relation (9) is divided into two functions: f and g, both of them depending on V_{GS}, and ψ_0 and the difference between them is denoted h as follows:

$$f = V_{GS} - \psi_0 \qquad (13)$$

$$g = a \cdot e^{\frac{q\psi_0}{2kT}} \cdot |\tan(y)| - \frac{2kT}{q} \cdot ln\{\cos(y)\} \qquad (14)$$

$$h = f - g \qquad (15)$$

For each value of V_{GS} in the above domain, ψ_0 is allowed to vary from 0 to the ψ_{0max} and, when h tends to zero, we obtain the ψ_0 for that V_{GS} value. The above described algorithm is implemented in the Matlab code. In order to prove its efficiency and applicability, an example is given in Figure 3, where the two functions f and g are represented in respect to ψ_0 for $V_{GS} = 0.5V$. From that figure, we see that the intersection point of the functions f and g ($h = 0$) represents the solution of the transcendental equation (9) which tells us that the electrostatic potential at the center of silicon film is $0.4353V$, when the applied gate-to-source voltage is $0.5V$. This example shows us that for each applied gate to source voltage in the above range, a corresponding value of ψ_0 is obtained in the same way.

Then the electrostatic potential at the surface of the silicon film is calculated from relation (6). Thus, we show in Figure 4 the dependence of ψ_0 and ψ_s as a function of V_{GS} for different silicon thicknesses: $5nm$ and $20nm$. One can see that electrostatic potential in the central silicon film is pinned at a constant value depending on the t_{si}, in agreement with Y. Taur's results [5]. In addition, one can observe that the surface electrostatic potential is gradually increasing as a function of applied gate-to-source voltage.

In Figure 5, we show similar results obtained by S. Malobabic et.al. [1] based on complex Lambert function and smoothing parameters without physical meaning. By comparing our data from Figure 4 with those given

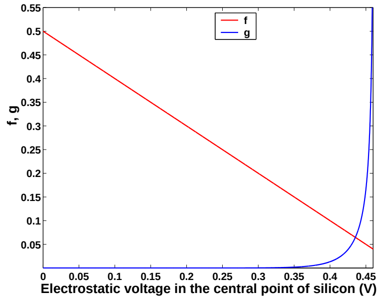

Figure 3: Intersection of the two function f and g when $V_{GS} = 0.5V$.

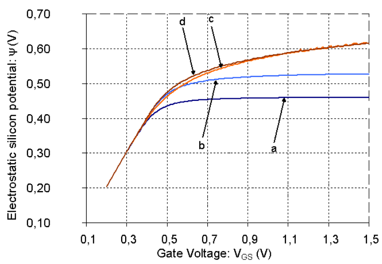

Figure 4: Solution ψ_s and ψ_0 with our method where: a. Central electrostatic potential for $t_{si} = 20nm$; b. Central electrostatic potential for $t_{si} = 5nm$; c. Surface electrostatic potential for $t_{si} = 20nm$; d. Surface electrostatic potential for $t_{si} = 5nm$;

by S. Malobabic et.al. in Figure 5, one can see that we have obtained practically the same results but in our case using a simple method.

Once the surface silicon electrostatic potential has been obtained, the total channel carrier charge induced in the channel is then calculated by using the relation (8) and, thus, the Figure 6 presents its dependence as a function of the gate voltages. From this figure, a threshold voltage of $0.4V$ for the DG SOI MOSFET with the material and geometrical parameters defined in the text.

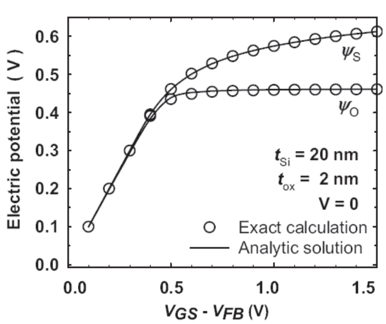

Figure 5: Solution ψ_s and ψ_0 with Lambert function [1].

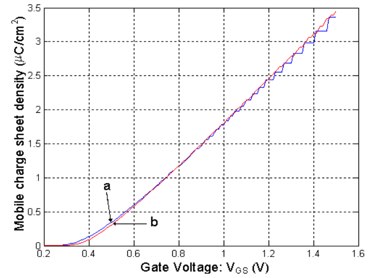

Figure 6: Dependence of the carrier charge per unit area induced in the channel as a function of gate voltages for: a. $t_{si} = 20nm$ and b. $t_{si} = 5nm$

4 CONCLUSIONS

An original, simple and efficient analytical method has been proposed for the computation of electrostatic potentials of the silicon film in an undoped symmetric DG SOI MOSFET device, starting from the analytical approach of Poisson's equation. Our procedure is based on mathematical computations implemented in the Matlab code. Our method could replace other complex approaches based on Lambert function and smoothing factor without physical meaning which were previously used for the same electrostatic potential calculation [1]. Continuing on the same direction, the total channel carrier charge was calculated suggesting a possible method of the threshold voltage variation.

REFERENCES

[1] S. Malobabic, A. Ortiz-Conde, F. J. Garcia Sanchez, "Modeling the Undoped-Body Symmetric Dual-Gate MOSFET", Proc. of the fifth IEEE International Caracas Conference on Devices, Circuits and Systems, ICCDCS, Punta Cana, RD, pp. 19-25, 2004.

[2] S. Thompson, P. Packan, M. Bohr, "MOS Scaling: Transistor Challenges for the 21st Century", Intel Technology Journal, 1998.

[3] E. Rauly, O. Potavin, F. Balestra, C. Raynaud, "On the subthreshold swing and short channel effects in single and double gate deep submicron SOI-MOSFETs", Solid-State Electronics, vol. 43, pp. 2033-2037, 1999.

[4] F. Balestra, S. Cristoloveanu et al., "Double gate silicon on insulator transistor with volume inversion: A new device with greatly enhanced performance", IEEE Electron Device Lett., vol. EDL-8, pp. 410, 1987.

[5] Y. Taur, "An analytical Solution to a Double-Gate MOSFET with Undoped Body", IEEE Electron Device Lett, vol. 21, pp. 245-247, 2000.