A Unified Parameter Extraction Procedure for Scalable Bipolar Transistor Model Mextram

H.-C. Wu, S. Mijalković and J. N. Burghartz

Delft University of Technology, HiTeC
Mekelweg 4, LB01.490, Delft 2628 CD, the Netherlands, hc.wu@ewi.tudelft.nl

ABSTRACT

In this paper, a unified parameters extraction procedure for temperature and geometry scalable bipolar transistor model Mextram has been demonstrated using an example of high-speed SiGe HBT technology. The essential feature of the proposed methodology is a direct extraction of the temperature and geometry parameters from the measured electrical characteristics and the model parameters are extracted only once for a single reference temperature and geometry.

Keywords: scalable model, bipolar devices, SiGe HBT, Mextram, Verilog-A

1 INTRODUCTION

With the complexity and variety of bipolar technologies, the geometry scaling is typically not part of the bipolar model descriptions and the geometry scaling is performed apart from the model parameter extraction [1]. Various auxiliary tools have been developed to extract geometry scaling parameters based on certain geometry scaling equations, process data and sets of single device parameters at different geometries. However, such a heterogeneous parameters extraction procedure could be in some cases inefficient due to the switching between different tools. Moreover, the resulting scalable model might accumulate the error originating from individual parameter extraction steps in different tools.

In order to overcome the above mention deficiencies, a unified procedure to extract electrical, temperature and geometry parameter directly from measured electrical data within the same extraction environment is proposed in this paper. It is particularly implemented and tested for the standard bipolar transistor model Mextram [2].

2 PHYSICS OF TEMPERATURE AND GEOMETRY SCALING IN SCALABLE MEXTRAM MODEL

2.1 Temperature Scaling

There are 14 temperature parameters in Mextram model. The physics behind these parameters are based on the mobility and bandgap scaled with temperature at emitter(E), base(B), collector(C) and substrate(S) region. Fig.1 shows temperature parameters in Mextram including mobility (A*) and bandgap (V*, D*) temperature parameters at each region respectively. The device temperature (T) for scaling is usually normalized to a reference temperature (T_R) as:

$$t_N = \frac{T}{T_R}, \tag{1}$$

where t_N is the normalized temperature. Each temperature scalable parameter P is a function of t_N as:

$$\frac{\mathrm{P}}{\mathrm{P_{ref}}} = \begin{cases} 1, & T = T_R. \\ f(t_N), & T \neq T_R. \end{cases} \tag{2}$$

Where $f(t_N)$ is physical temperature scaling equation of different parameter. When T is other than T_R, P is scaled to that evaluated temperature. The temperature scaling rule for each P is part of the Mextram model equations so it will not be derived here.

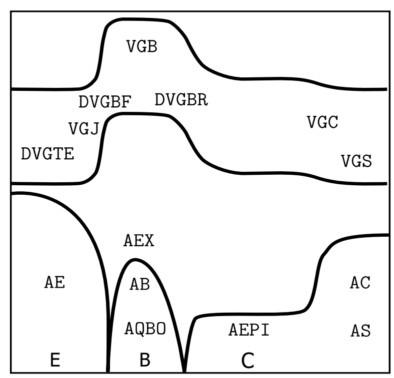

Figure 1: Temperature scaling parameters, which is based on bandgap and mobility variation over temperatures, in Mextram model.

2.2 Geometry Scaling

The physical quantities in a bipolar transistor that scales with geometry can be separated into three categories including I) current and charge, II) ratio of current and charge and III) parasitic resistance. There are normally three PN junctions (E-B, B-C and C-S) in a bipolar transistor. Fig.2 shows the top view and cross-section of a PN junction, which can be separated into bulk, sidewall and corner components depending on the shape of the junction area. The electrical model parameter P that describe current or charge scales with area of the junction can be described by following expression [3],

$$\mathrm{P} = \underbrace{P_A^{''} W_{eff} L_{eff}}_{\text{Bulk}} + \underbrace{P_W^{''} W_{eff} + P_L^{''} L_{eff}}_{\text{Sidewall}} + \underbrace{P_C^{''}}_{\text{Corner}} . \tag{3}$$

Where $P_A^{''}$, $P_W^{''}$, $P_L^{''}$ and $P_C^{''}$ are the constant geometry parameters that account for bulk, width, length and corner contributions, respectively. $W_{eff} = W + dW$ and $L_{eff} = L + dL$ are effective electrical width and length of the junction while W and L are the drawn sizes of the junction in the layout. dW and dL are the offset between electrical (W_{eff}, L_{eff}) and drawn (W, L) geometry. If dW and dL are constant, (3) can be expressed in terms of W and L as:

$$\mathrm{P} = P_A^{'} WL + P_W^{'} W + P_L^{'} L + P_C^{'}. \tag{4}$$

Where $P_A^{'}$, $P_W^{'}$, $P_L^{'}$, and $P_C^{'}$ are composite of geometry parameters in (3). If (4) can be further expressed in the same form as temperature parameters, *i.e.*: a reference parameter as pre-factor times its scaling equations. Both temperature and geometry parameters can have the same extraction methodology. Just as temperature is normalized to a reference temperature, P, W, and L in (4) are normalized to $\mathrm{P_{REF}}$ and its reference geometry (W_{ref}, L_{ref}) as:

$$\frac{\mathrm{P}}{\mathrm{P_{ref}}} = P_A \frac{WL}{W_{ref} L_{ref}} + P_W \frac{W}{W_{ref}} + P_L \frac{L}{L_{ref}} + P_C. \tag{5}$$

Now, P_A, P_W, P_L and P_C are the normalized geometry parameters. However, (5) is not the most compact form for geometry scaling since the constant corner term is in both reference and evaluated geometries. It can be removed by following substraction:

$$\frac{\mathrm{P} - \mathrm{P_{ref}}}{\mathrm{P_{ref}}} = P_A \left(\frac{WL}{W_{ref} L_{ref}} - 1 \right) + P_W \left(\frac{W}{W_{ref}} - 1 \right) + P_L \left(\frac{L}{L_{ref}} - 1 \right) \tag{6}$$

Re-arranging (6), the geometry scaling equation becomes:

$$\frac{\mathrm{P}}{\mathrm{P_{ref}}} = 1 + P_A \left(\frac{WL}{W_{ref} L_{ref}} - 1 \right) + P_W \left(\frac{W}{W_{ref}} - 1 \right) + P_L \left(\frac{L}{L_{ref}} - 1 \right), \tag{7}$$

which is the most compact form for geometry scaling. When $W = W_{ref}$ and $L = L_{ref}$ in (7), the evaluated electrical parameter P is equal to reference electrical parameter $\mathrm{P_{ref}}$ as is in temperature scaling equations.

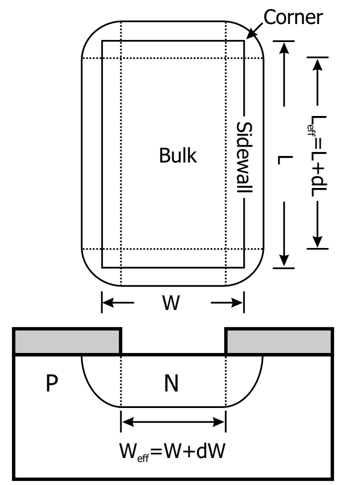

Figure 2: Top view and cross-section of a PN diode.

Some of the scalable model parameters represent the ratio of current and charge. For example, the ratio of total base charge to B-C junction capacitance (CJC) defines the forward early voltage (VEF). As a results, VEF scales as:

$$\frac{\mathrm{P}}{\mathrm{P_{ref}}} = \frac{1 + P_{A1}(\frac{WL}{W_{ref}L_{ref}} - 1) + P_{W1}(\frac{W}{W_{ref}} - 1)}{1 + P_{A2}(\frac{WL}{W_{ref}L_{ref}} - 1) + P_{W2}(\frac{W}{W_{ref}} - 1)} \frac{+P_{L1}(\frac{L}{L_{ref}} - 1)}{+P_{L2}(\frac{L}{L_{ref}} - 1)}. \tag{8}$$

Only the geometry parameter in the numerator of (8) is extracted here because the denominator is extracted from scaling of CJC.

Parasitic resistance models current flows path from external to intern node. There are three types of parasitic resistance in a bipolar transistor including vertical, lateral and both vertical and lateral resistance. For resistance that models vertical current flow path, it scales with reciprocal of (7) as reciprocal of the current. For resistance that models lateral current flow path, it scales with the effective square of the flow path as:.

$$\mathrm{P} = R_{sq} \left(\frac{W_{eff}}{L_{eff}} + C \right), \tag{9}$$

where R_{sq} is the sheet resistance of square and C models the constant corner effect. The reference based scaling equation of (9) will be:

$$\frac{\mathrm{P}}{\mathrm{P_{ref}}} = 1 + P_A \left(\frac{\frac{W}{W_{ref}} + P_W}{\frac{L}{L_{ref}} + P_L} - \frac{1 + P_W}{1 + P_L} \right). \quad (10)$$

For resistance that models both vertical and lateral current flow path, it is modelled as vertical and lateral resistance in series which is a combination of (7) and (10).

3 IMPLEMENTATION AND RESULTS

Since the temperature scaling equations and parameters are part of the standard Mextram model already, only the geometry scaling equations and parameters has to be added in the scalable model. It can be done easily by extending the standard Mextram model implementation in Verilog-A [4] with additional geometry scaling module and parameters. The Verilog-A model can be employed within IC-CAP [5] environment using Agilent ADS simulator [6] and corresponding Verilog-A compiler. Parameter extraction for the scalable Mextram model is demonstrated using a high-speed SiGe HBT technology [7]. Fig. 3 shows the available device geometry matrix for parameter extraction. To extract temperature and geometry parameters in IC-CAP, the measuring temperature and geometry of each device under test have to be added in the measured data files as additional input parameters.

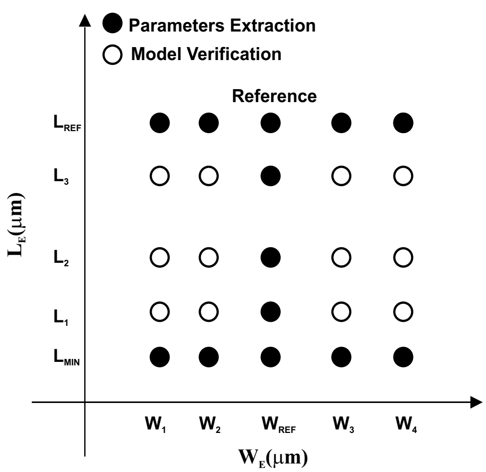

Figure 3: Geometry matrix for the scalable model parameters extraction.

Fig. 4 shows flow chart of a unified temperature and geometry parameter extraction procedure for the scalable model implemented as an IC-CAP model file. The parameter extraction starts from a reference device. A good choice of the reference device is relative large geometry in order to have area, sidewall and corner available but not too large to have self-heating effect even in low current region. As a result, the reference device is chosen to have the width in the middle and the maximum length in the matrix shown in Fig. 3. The drawn emitter width (W_E), length (L_E), sheet resistance of internal and external base, epi-collector doping level and epi-collector thickness is specified as technology parameters for initial parameters calculation to help numerical optimizer to find the optimal parameter values during parameter extraction. The electrical parameters are extracted for the reference geometry following standard procedure [8] going from low current towards high current related parameters. In the mean time, the temperature parameters are extracted before high current parameters to accurately model the temperature rise from self-heating at high current region. The mobility temperature parameters A* is determined from a database of mobility temperature parameter vs. doping concentration [9]. The bandgap temperature parameters V* and D* are determined from the variation of measured electrical data over temperatures [8]. Fig. 5 shows a setup for the extraction of a temperature parameter from temperature dependent Gummel plots.

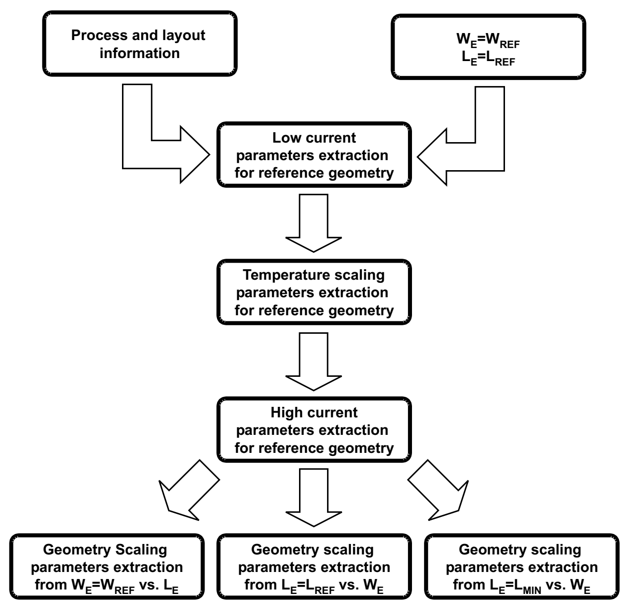

Figure 4: Flow chart of a unified parameter extraction procedure in the IC-CAP model file.

After the extraction of reference and temperature parameters, geometry parameters can be extracted from the same measurement data at (a) $L_E = L_{REF}$ vs W_E, (b) $W_E = W_{REF}$ vs L_E and (c) $L_E = L_{MIN}$ vs W_E as marked in Fig. 3. It usually just takes two to three repeat sequence of extraction for optimizer to find P_A, P_W and P_L. Fig. 6a, 6b and 6c show resulting plots of cut-off frequency (F_T) vs. collector current (I_C) after high current and transit time geometry parameter extraction.

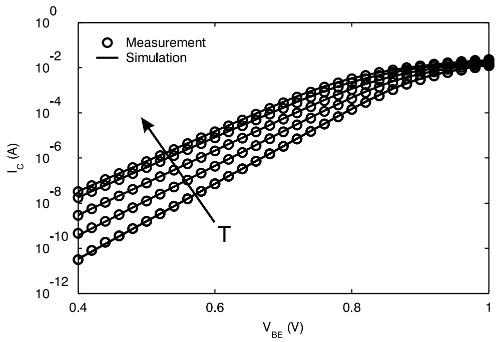

Figure 5: Extraction of "VGB" from measured collector current I_C at $W_E = W_{REF}$, $L_E = L_{REF}$ and $T = 25,\ 50,\ 75\ 100,\ 125,\ 150\ °C$.

The essential feature of the unified extraction procedure is a direct extraction of the temperature and geometry parameters from the measured electrical characteristics and the model parameters as reference parameters are extracted only once for a reference geometry. The whole extraction procedure is integrated in the single environment, which save time in verification of the final scalable model results with measured data.

4 CONCLUSION

In this paper, a unified parameter extraction procedure is proposed for a scalable model Mextram. It is implemented within an IC-CAP model file using an example of high-speed SiGe HBT technology as a practice. No additional tool is needed for temperature and geometry parameter extraction. As a result, the scalable model library generation is more efficient and the accuracy is increased with the proposed parameter extraction approach.

REFERENCES

[1] H.-C. Wu, S. Mijalkovic and J. Burghartz, "Parameters Extraction of a Scalable Mextram Model for High-Speed SiGe HBTs," 2004 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Montreal, Canada, pp. 140-143.

[2] J. C. J. Paasschens, W. J. Kloosterman, "The Mextram Bipolar Transistor Model - Level 504," Philips Research Laboratories, Eindhoven.

[3] H.C. de Graaff and F.M. Klaasen, *Compact Transistor Modeling for Circuit Design*, New York: Springer-Verlag, 1990.

[4] H.-C. Wu, S. Mijalkovic, J.G. Macias and J.N. Burghartz, "Mixed Compact and Behavior Modeling Using AHDL Verilog-A," 2003 IEEE International Workshop on Behavioral Modeling and Simulation, San Jose, CA, USA, pp. 139-143.

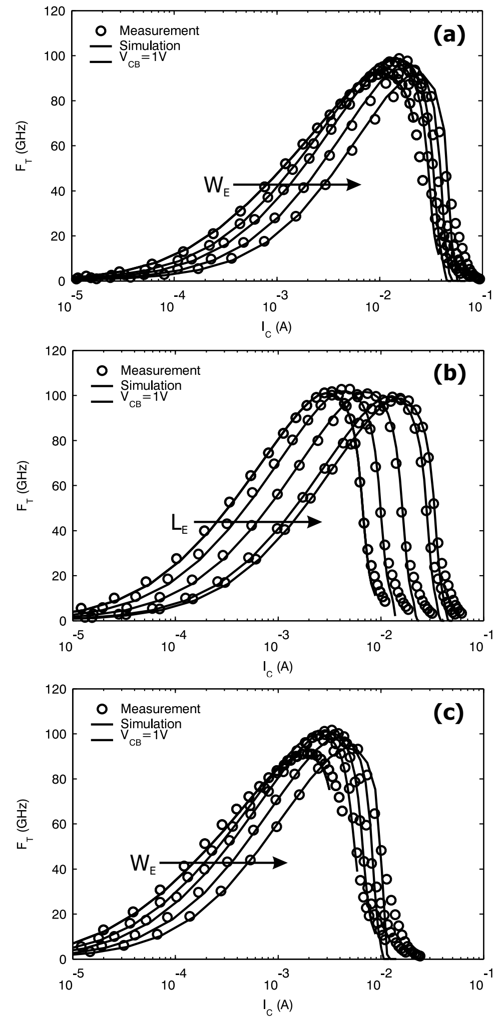

Figure 6: Measurement and simulation results of F_T vs I_C at (a)$L_E = L_{REF}\ vs.\ W_E \uparrow$, (b) $W_E = W_{REF}\ vs.\ L_E \uparrow$, (c) $L_E = L_{MIN}\ vs.\ W_E \uparrow$ and $T = 25\ °C$.

[5] "IC-CAP 2004", Agilent Technology.

[6] "Advenced Design System 2005A", Agilent Technology.

[7] J.C.-H. Lin et al., "State of Art RF/Analog Foundry Technology," IEEE Bipolar/BiCMOS Circuits and Technology Meeting, pp. 73-79. 2002.

[8] J. C. J. Paasschens, W. J. Kloosterman and R.J. Havens, "Parameter Extraction for the Bipolar Transistor Model Mextram - Level 504," Philips Research Laboratories, Eindhoven.

[9] D. B. M. Klaassen, "A unified mobility model for device simulation-II. temperature dependence of carrier mobility and lifetime," Solid-State Elec., Vol. 35, No.7, pp. 961-967, 1992.