Numerical Simulation of Drain-Current Transients and Current Compression in GaN MESFETs

H. Takayanagi, K. Itagaki and K. Horio

Faculty of Systems Engineering, Shibaura Institute of Technology
307 Fukasaku, Minuma-ku, Saitama 337-8570, Japan, horio@sic.shibaura-it.ac.jp

ABSTRACT

Transient simulations of GaN MESFETs are performed in which a three-level compensation model is adopted for a semi-insulating buffer layer, where a shallow donor, a deep donor and a deep acceptor are considered. Quasi-pulsed I-V curves are derived from the transient characteristics, and are compared with steady-state I-V curves. It is shown that so-called current compression is more pronounced when the deep-acceptor density in the buffer layer is higher and when an off-state drain voltage is higher, because trapping effects become more significant. It is suggested that to minimize current compression in GaN-based FETs, an acceptor density in a semi-insulating GaN layer should be made low.

Keywords: GaN, FET, deep level, current compression

1 INTRODUCTION

GaN-based FETs are now receiving great attention because of their potential applications to high power and high temperature microwave devices [1]. However, slow current transients are often observed even if the drain voltage or the gate voltage is changed abruptly [2]. This is called drain lag or gate lag, and is problematic in circuit applications. The slow transients mean that dc current-voltage (I-V) curves and RF I-V curves become quite different, resulting in lower RF power available than that expected from dc operation [1,2]. This is called power (current) compression. These are serious problems, and there are many experimental works reported on these phenomena. However, only a few theoretical works have been reported for GaN-based FETs [3,4], although several numerical analyses were made for GaAs-based FETs [5-8]. Therefore, in this work, we have made systematic transient simulations of GaN MESFETs in which deep levels in a semi-insulating buffer layer are considered, and studied how the slow current transients and the current compression are affected by deep-level densities in the buffer layer and by an applied drain bias [9,10].

2 PHYSICAL MODEL

Fig.1 shows a device structure analyzed here. The gate length \( L_G \) is set to 0.3 \( \mu \)m. As a model for the semi-insulating buffer layer, we use a three level compensation model which includes a shallow donor, a deep donor and a deep acceptor. Some experiments show that two levels (\( E_C - 1.75 \) eV, \( E_C - 2.85 \) eV) are associated with current compression in GaN-based FETs with a semi-insulating buffer layer [2], so that we use energy levels of \( E_C - 2.85 \) eV (or \( E_C + 0.6 \) eV) for the deep acceptor and of \( E_C - 1.75 \) eV for the deep donor. Other experiments show shallower energy levels for the deep donor [11,12], and hence we vary the deep donor’s energy level (\( E_{DD} \)) as a parameter. Here, the deep-donor density (\( N_{DD} \)) and the deep-acceptor density (\( N_{DA} \)) are typically set to \( 5 \times 10^{16} \) cm\(^{-3}\) and \( 2 \times 10^{16} \) cm\(^{-3}\), respectively. The shallow-donor density in the buffer layer \( N_{Di} \) is set to \( 10^{15} \) cm\(^{-3}\).

Basic equations to be solved are expressed as follows.

1) Poisson’s equation

\[
\nabla^2 \psi = -\frac{q}{\varepsilon} (p-n+N_D+N_{Di}+N_{DD}^- - N_{DA}^-) 
\]

2) Continuity equations for electrons and holes

\[
\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - (R_{n,DD} + R_{n,DA}) 
\]

\[
\frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot J_p - (R_{p,DD} + R_{p,DA}) 
\]

where

\[
R_{n,DD} = C_{n,DD} N_{DD}^+ n - e_{n,DD} (N_{DD}^+ - N_{DD}^-) 
\]

\[
R_{n,DA} = C_{n,DA} (N_{DA}^- - N_{DA}^+) n - e_{n,DA} N_{DA}^- 
\]

\[
R_{p,DD} = C_{p,DD} (N_{DD}^- - N_{DD}^+) p - e_{p,DD} N_{DD}^+ 
\]

\[
R_{p,DA} = C_{p,DA} N_{DA}^- p - e_{p,DA} (N_{DA}^- - N_{DA}^+) 
\]
3) Rate equations for the deep levels

\[
\frac{\partial}{\partial t}(N_{DD} - N_{DD}^+) = R_{n,DD} - R_{p,DD} \tag{8}
\]

\[
\frac{\partial}{\partial t}N_{DA} = R_{n,DA} - R_{p,DA} \tag{9}
\]

where \(N_{DD}^+\) and \(N_{DA}\) represent ionized densities of deep donors and deep acceptors, respectively. \(C_T\) and \(C_P\) are the electron and hole capture coefficients of the deep levels, respectively, and the subscript (DD, DA) represents the corresponding deep level.

The above basic equations are put into discrete forms and are solved numerically. We have calculated the drain-current responses when the drain voltage \(V_D\) and/or the gate voltage \(V_G\) are changed abruptly.

### 3 SLOW CURRENT TRANSIENTS

Fig.2 shows calculated drain-current responses when the drain voltage \(V_D\) is raised abruptly from 0 V to 20 V or when \(V_D\) is lowered from 20 V to 6 V, where the gate voltage \(V_G\) is kept constant (0 V). Here, three cases with different \(E_C - E_{DD}\) are shown. When \(V_D\) is raised, the drain currents overshoot steady-state values, because electrons are injected into the buffer layer, and deep traps there need certain time to capture these electrons. On the other hand, when \(V_D\) is lowered, the drain currents remain at low values for some periods and begin to increase slowly, showing drain lag behavior. This is due to the slow response of deep donors. It is understood that the current responses begin to increase as the deep donors begin to emit electrons, and hence the response is faster for shallower \(E_{DD}\). In fact, the current rise time is roughly consistent with the deep donor's electron-emission time constant given by \(1/e_n,DD\), which becomes \(3.9 \times 10^{-3}\) s and \(9.8 \times 10^{-3}\) s for \(E_C - E_{DD} = 0.5\) eV and 1.0 eV, respectively. The above overshoot and undershoot behavior is also reported experimentally in GaN MESFETs and HEMTs [2],[3].

We have next calculated a case when \(V_D\) and \(V_G\) are both changed abruptly. Fig.3 shows calculated turn-on characteristics (\(E_C - E_{DD} = 1.0\) eV) when \(V_G\) is changed from the threshold voltage \(V_{th}\) to 0 V. The off-state drain voltage \(V_{Doff}\) is 20 V, and the parameter is the on-state drain voltage \(V_{Don}\). The characteristics are similar to those in Fig.2, and hence the change of \(V_D\) is essential in this case. Fig.4 shows calculated \(I_D-V_D\) curves. In this figure, we plot by point (x) the drain current at \(t = 10^{-6}\) s after the gate voltage is switched on. This is obtained from Fig.3, and this curve corresponds to a quasi-pulsed \(I-V\) curve with pulse width of \(10^{-6}\) s. (We are also plotting other quasi-pulsed \(I-V\) curves when only \(V_D\) is changed (cf. Fig.2), which reflect overshoot and undershoot.) It is seen that the drain currents in the pulsed \(I-V\) curve are rather lower than those in the steady state. This clearly indicates that the current compression could occur due to the slow response of deep levels in the semi-insulating buffer layer. This type of current reduction is commonly observed experimentally in GaN-based FETs.
4 CURRENT COMPRESSION

4.1 Dependence on Deep-Acceptor Density

We have studied dependence of calculated $I$-$V$ curves and drain-current responses on the deep-level densities ($N_{DD}$, $N_{DA}$) in the buffer layer. We have found that these characteristics are almost independent of $N_{DD}$ under a condition that $N_{DD}$ is higher than $N_{DA}$ and $E_C - E_{DD}$ is the same, and that these are mainly determined by $N_{DA}$. This is because in this condition, the ionized deep-donor density $N_{DD}^+$, which acts as an electron trap, becomes nearly equal to $N_{DA}$ under equilibrium [5]. Hence, we will show $N_{DA}$ dependence of the characteristics.

Fig.5 shows calculated $I_D$-$V_D$ curves of GaN MESFETs with $N_{DA} = 5 \times 10^{15}$ cm$^{-3}$ or $10^{17}$ cm$^{-3}$, where $N_{DD}$ is $2 \times 10^{17}$ cm$^{-3}$ and $E_C - E_{DD}$ is 0.5 eV. The solid lines are steady-state $I$-$V$ curves. The dashed lines are quasi-pulsed $I$-$V$ curves (pulse width of $10^8$ s) derived from the calculated turn-on characteristics, as mentioned before. It is seen that the steady-state drain currents are higher for lower $N_{DA}$. This is because the current via the buffer layer becomes larger for lower $N_{DA}$ due to less steep barrier at the active layer-buffer interface. It is also clearly seen that the current reduction in the pulsed $I$-$V$ curves is more pronounced for higher $N_{DA}$. This is because, as mentioned before, the ionized deep-donor density $N_{DD}^+$, which acts as an electron trap, becomes nearly equal to $N_{DA}$ under equilibrium, and hence the trapping effect (or the resulting current compression) should become more pronounced for higher $N_{DA}$.

Fig.6 shows a comparison of ionized deep-donor density $N_{DD}^+$ profiles between (a) $N_{DA} = 5 \times 10^{15}$ cm$^{-3}$ and (b) $N_{DA} = 10^{17}$ cm$^{-3}$. The left is for the off state ($V_D = 20$ V, $V_G = V_{th}$) and the right is for an on state ($V_D = 6$ V, $V_G = 0$ V). In the off state, $N_{DD}^+$ in the deep area of buffer layer is lower (negative space-charge densities are higher) than in the on state for the both cases, and hence the current reduction or current compression occurs. But the difference of $N_{DD}^+$ between off and on states is an order of $10^{15}$ cm$^{-3}$ for the case of $N_{DA} = 5 \times 10^{15}$ cm$^{-3}$ and of $10^6$ cm$^{-3}$ for the case of $N_{DA} = 10^{17}$ cm$^{-3}$, and hence the current compression becomes weaker for lower $N_{DA}$. Here, it should be mentioned that for lower $N_{DA}$, the current compression could be weakened, and the threshold voltage shifts toward negative bias because of the higher current density via the buffer layer. Therefore, there may be a trade-off relationship between reducing the current compression and obtaining sharp current cutoff.

4.2 Dependence on Off-State Drain Voltage

Next, we describe dependence of off-state drain voltage $V_{D_{Off}}$ on the current compression. Figs.7 and 8 show calculated steady-state $I_D$-$V_D$ curves and quasi-pulsed $I$-$V$ curves (with pulse width of $10^8$ s) as a parameter of $V_{D_{Off}}$, which are derived from calculated turn-on characteristics as described before. In Fig.7, $N_{DD} = 5 \times 10^{16}$ cm$^{-3}$, $N_{DA} = 2 \times 10^{16}$ cm$^{-3}$.
$E_C - E_{DD} = 0.5 \text{ eV}$, and in Fig. 8, $N_{DD} = 2 \times 10^{17} \text{ cm}^{-3}$, $N_{DA} = 10^{17} \text{ cm}^{-3}$, $E_C - E_{DD} = 0.5 \text{ eV}$. It is seen that for higher $V_{Doff}$, the drain currents in the pulsed $I$-$V$ curves become lower at a given $V_G$, indicating that the current compression is more pronounced for higher $V_{Doff}$.

Fig. 9 shows (a) electron density profiles and (b) $N_{DD}^+$ profiles in the off state for the two cases, corresponding to Fig. 8. The left is for $V_{Doff} = 40 \text{ V}$, and the right is for $V_{Doff} = 100 \text{ V}$. It is seen that for higher $V_{Doff}$, electron densities in the buffer layer become higher particularly under the gate and the gate-to-drain region, because electrons are injected into the buffer layer by the applied drain bias. These electrons are captured by the deep donors, and hence $N_{DD}^+$ becomes lower there for higher $V_{Doff}$. Hence, when $V_G$ is switched on and $V_D$ is lowered from higher $V_{Doff}$, the drain current remains at a lower value. Therefore, the current compression is more pronounced for higher $V_{Doff}$. This tendency is also reported experimentally in AlGaN/GaN HFETs [13].

5 CONCLUSION

Transient simulations of GaN MESFETs have been performed in which a three level compensation model is adopted for the semi-insulating buffer layer, where a shallow donor, a deep donor and a deep acceptor are considered. Quasi-pulsed $I$-$V$ curves have been derived from the transient characteristics. It has been shown that the current compression is more pronounced when the deep-acceptor density in the buffer layer is higher and when the off-state drain voltage is higher, because the change of ionized deep-donor density becomes larger and hence the trapping effects become more significant. The above buffer-trapping effects may be similar to trapping effects in an undoped GaN layer in AlGaN/GaN HEMTs. Therefore, it is suggested that to minimize current compression in GaN-based FETs, an acceptor density in a semi-insulating GaN layer should be made low.

REFERENCES