# Random Dopant Induced Fluctuations of Characteristics in Deep Sub-micron MOSFETs

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## ABSTRACT

As the gate length of MOSFET devices shrinks down below 100 nm, the fluctuation of major devices parameter, namely, threshold voltage ($V_{TH}$), subthreshold swing, drain current ($I_D$) and subthreshold leakage current due to influences of processes variations becomes a serious problem. Random dopant fluctuation is one of the problems. In this work, we theoretically examine the fluctuation effects of random dopant on the threshold voltage and drain current variation in single-gate (MOSFET), SOI and double-gate MOSFETs. In the numerical simulation of the threshold voltage variation, the drift-diffusion and density gradient models are considered to describe transport phenomena with quantum effects of devices. Random dopant induces drain current and threshold voltage lowering. The reduction becomes larger with channel length is scaling down. From the results, $V_{TH}$ can be controlled by thin channel DG-MOSFET and SOI devices. However, thin channel may reduce $I_D$. Thus, structure of devices needed to be optimized. The fluctuation of device characteristics caused by random dopant cannot be neglected. From the fabrication point of view, we concluded that the random dopant fluctuation of device characteristics could be controlled in the design of SOI and DG-MOSFET.

***Keywords***: MOSFET, double-gate, SOI, threshold voltage, quantum mechanical effects, random dopant fluctuation, simulation.

## 1 INTRODUCTION

Short channel effects, subthreshold slope, current-voltage characteristics and quantum effects, are the most interesting topics in the recent years while semiconductor devices are scaled into deep sub-micron dimensions [1-2]. Among the characteristics of devices, the threshold voltage ($V_{TH}$) and the drain current ($I_D$) are the two crucial one, which determine the operation of a device. The former one corresponds to the onset of inversion channel build-up, which means the starting of the devices operation. Hence, it has to be estimated accurately. Threshold voltage not only determines the MOSFET's operation characteristics but also judge the function of designed circuit. Therefore, plenty of works focus on studying the definition of $V_{TH}$, how to extract $V_{TH}$ or model $V_{TH}$ analytically, how to control the $V_{TH}$ or how to design an optimal device according to $V_{TH}$. The later one, which is the drain current of a device, is the flow of electrons from the source to the drain is controlled by the voltage applied to the gate. Drain current determines the signal presented by the devices. As the scale of integrated circuit moving form VLSI to ULSI, large current is necessary to reduce the RC delay.

However, when the gate channel length of MOSFET devices shrinks down below 100 nm, the fluctuation of threshold voltage and drain current due to influences of processes variations becomes a serious problem [3]. The fluctuation in conjunction with the scaling of the supply voltage may seriously the functionality, performance and yield of the corresponding systems. Random dopant fluctuation is one of the problems [3-7]. Therefore, as scaling size of devices and developing of new transistor architecture, the random dopant fluctuation may be required to avoid so as improving the device integration. In this study, we examine the influence of random dopant fluctuation on $V_{TH}$ and $I_D$ for single-gate metal-oxide-semiconductor field-effect transistor (MOSFET), silicon-on-insulator (SOI) and double-gate MOSFET (DG-MOSFET) with different channel lengths ($L_G$) and silicon film thickness ($T_{si}$). From the simulated scenario, we will try to find a suitable designing rule for deep sub-micron devices. The remaining content of this study is given as follows. Sec. 2 briefly explains the simulation models and the computational method. Sec. 3 shows the simulation results and discussion. Sec. 4 draws the conclusion.

## 2 QUANTUM MECHANICAL MODEL

According to related studies, quantum effects must be considered in simulation for semiconductor devices, which channel length are smaller than 0.1 $\mu$m. In this study, the drift-diffusion and density gradient models are considered to describe transport phenomena with quantum effects of devices. In principle, the Schrödinger equation coupled with classical model is the most accurate way to solve the carrier concentration. However, it is computationally expensive. Quantum correction models are suggested to instead of the Schrödinger equation. Among quantum

correction models, the density-gradient model is considered a better approximation than that of the Hänsch, van Dort model, and MLDA models [8-13]. Therefore, density-gradient method is chosen to couple with the classical, which is the drift-diffusion model in this work. The model is given as follows. Firstly, the three governing equations of drift-diffusion model are listed as follows. The Poisson equation is

$$\nabla\varepsilon\cdot\nabla\psi=-q\left(p-n+N_D-N_A\right), \tag{1}$$

where $\varepsilon$ is the electrical permittivity, $q$ is the elementary electronic charge, $n$ and $p$ are the electron and hole densities, and $N_D$ and $N_A$ are the number of ionized donors and acceptors, respectively. The other two equations are continuity equations, which are

$$q\frac{\partial n}{\partial t}-\nabla\cdot\mathbf{J_n}=-qR\,, \tag{2}$$

$$q\frac{\partial p}{\partial t}+\nabla\cdot\mathbf{J_p}=-qR\,, \tag{3}$$

where $\mathbf{J}_n=-qn\mu_n\nabla\phi_n$ and $\mathbf{J}_p=-qp\mu_p\nabla\phi_p$ are the electron and hole current densities. $\mu_n$ and $\mu_p$ are the electron and hole mobility, and $\phi_n$ and $\phi_p$ are the electron and hole quasi-Fermi potentials.

To include quantization effects in a classical device simulation, a simple approach is to introduce an additional potential, such as quantity $\Lambda$, in the classical density formula, which reads:

$$n=N_C\exp\left(\frac{E_F-E_C-\Lambda}{k_BT}\right), \tag{4}$$

where $N_C$ is the conduction band density of states, $E_C$ is the conduction band energy, and $E_F$ is the electron Fermi energy. The density-gradient approach may be derived from the one particle Wigner function and obtained the additional, non-classical, quantum correction term $\Lambda$, which is given as

$$\Lambda=-\frac{\gamma\hbar^2}{12m}\frac{\nabla^2\sqrt{n}}{\sqrt{n}}\,, \tag{5}$$

where $\hbar$ is the reduced Planck constant, $m$ is the density of states mass, and $\gamma$ is a fitting factor.

The Gummel scheme is employed to solve the model. The computing procedure is described as follows. Firstly, the stop criteria, mesh, output variables and simulated devices are chosen. Next step is solving the Poisson equation with density-gradient correction modified potential iteratively. After the Poisson equation is convergent, continuity equations are solved. Then, we'll check the whole system converges or not. If the whole system converges, then stop computing. Otherwise, the Poisson equation and continuity equations should be solved again until the whole system equations converge. This scheme makes sure the solution will be self-consistent.

Furthermore, the definition of threshold voltage employed in this study is the Gm maximum method. The method firstly find out the gate voltage at the maximum of Gm, then make a tangent line of the drain current – gate voltage ($I_D$-$V_G$) curve at the gate voltage. Finally, extrapolated intercept of the tangent line to the $V_G$-axis; the extrapolation is defined as $V_{TH}$.

## 3 NUMERICAL RESULTS AND DISCUSSIONS

In this work, we examine the fluctuation effects of random dopant on the threshold voltage and drain current variation in single-gate MOSFET, SOI and DG-MOSFETs, which are illustrated in Fig. 1. In the numerical studies, the simulated oxide thickness ($T_{ox}$) is 3 nm, channel length ($L_G$) are 35, 40 and 50 nm, Si film thickness ($T_{si}$) are 10 and 20 nm and source/drain doping concentration is $1\times10^{20}$ $cm^{-3}$. The uniform channel doping concentration ($N_A$) is $1\times10^{18}$ $cm^{-3}$. Random number is generated from 0.01 to 50 uniformly and the cases are simulated by ISE-DESSIS ver. 10.0.

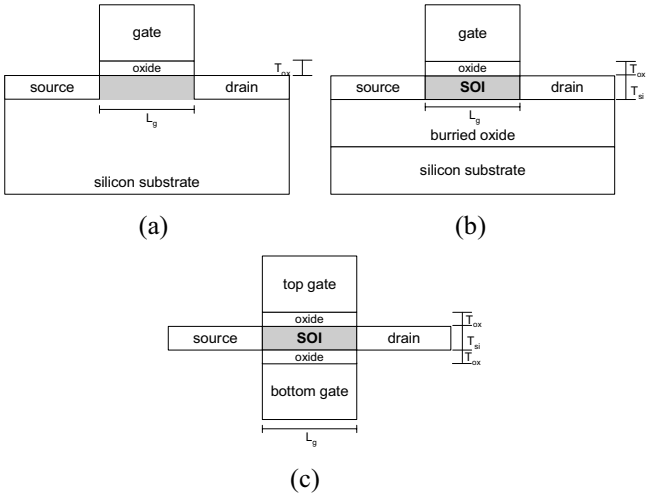



Figure 1. Simulated devices (a) single-gate MOSFET; (b) SOI and (c) double-gate MOSFET, the gray region is the random dopant region.

Figures 2 and 3 compare drain current of three kinds of devices with $L_G$ = 50 and 35, respectively. Figures 4~6 illustrate simulated results of $I_D$-$V_G$ curves for MOSFETS, SOI and DG-MOSFET with uniform and random dopant concentration. $V_{TH}$ fluctuation for devices with different $L_G$ and $T_{si}$ are shown in Fig. 7.

From Fig.2, DG-MOSFET with $T_{si}$ = 10 nm presents the best performance of all because the $I_D$ is the largest and the $I_D$-$V_G$ curve presents an acceptable $V_{TH}$. $I_D$ of the SOI with $T_{si}$ = 10 nm is as small as it of MOSFET. However, $V_{TH}$ of the MOSFET is the largest one, which means that the MOSFET presents the worst performance among the simulated devices. That is, the MOSFET needs a large applied voltage to turn on, but induces a small drain current. SOI and DG-MOSFET present better operational properties

than MOSFET does. For both SOI and DG-MOSFET, if $T_{si}$ is thicker, $I_D$ becomes larger and $V_{TH}$ becomes smaller. On the other hand, if $T_{si}$ becomes thinner, $I_D$ becomes smaller and $V_{TH}$ is larger. According to Figs. 2, 3and 7, we find that $I_D$ becomes larger, but $V_{TH}$ becomes smaller while $L_G$ becomes smaller. $V_{TH}$ drops because of the short channel effects. As $L_G$ = 35 nm, $I_D$ of SOI with $T_{si}$ = 10 nm becomes the smallest one. Since $V_{TH}$ of the MOSFET and DG-MOSFET and SOI with $T_{si}$ = 20 nm are too small so that they cannot present good on/off operation in a circuit. Besides, $V_{TH}$ of them varies largely, which is impossible to be used in a designed circuit. Among the devices, DG-MOSFET and SOI with thin channel thickness are promising for CMOS technology at channel length below 50 nm. The results agree with our previous results [14], that is, $V_{TH}$ can be controlled by the channel thickness of DG-MOSFET and SOI devices.

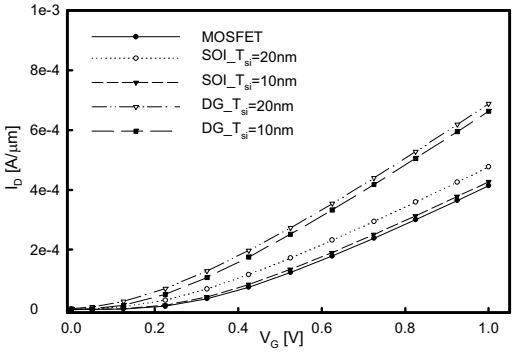



Figure 2. Simulated $I_D$-$V_G$ curves for devices with $T_{ox}$=3nm, $N_a$=$10^{18}$ $cm^{-3}$, $L_G$=50nm for $V_G$ = 1.0V, $V_D$=1.0V.

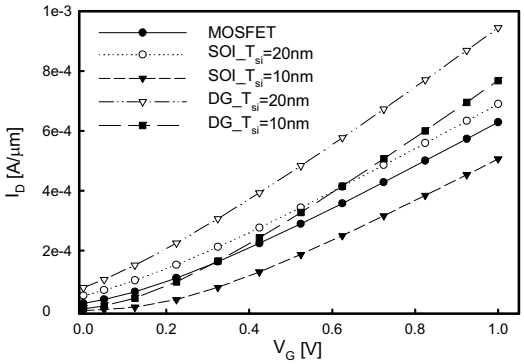



Figure 3. Simulated $I_D$-$V_G$ curves for devices with $T_{ox}$=3nm, $N_a$=$10^{18}$ $cm^{-3}$, $L_G$=35nm for $V_G$ = 1.0V, $V_D$=1.0V.

Figures 4~6 report the $I_D$-$V_G$ curves of devices with uniform and random dopant (UD and RD). From the figures, random dopant induces drain current lowering and threshold voltage enlarging. The reductions of $I_D$ of devices are given as follows. MOSFET is about 10%. SOI with $T_{si}$ = 10 nm is about 9%~12% and SOI with $T_{si}$ = 20nm is about 7%~11%. DG-MOSFET with $T_{si}$ = 10 nm is about 3%~5% and DG-MOSFET with $T_{si}$ = 20 nm is about 2%~5%. While channel length is longer, the variation caused by random dopant becomes larger. The smallest influence of random dopant, which is 2%~5%, is the DG-MOSFET with $T_{ox}$=3nm, $T_{si}$=10nm, $L_G$=35nm. $I_D$ reduction rate caused by random dopant of single-gate MOSFET almost keeps in the same percentage in all size of devices. Among MOSFET, SOI and DG-MOSFET, the influence of random dopant fluctuation on DG-MOSFET is the smallest, especially in a thin channel thickness device.

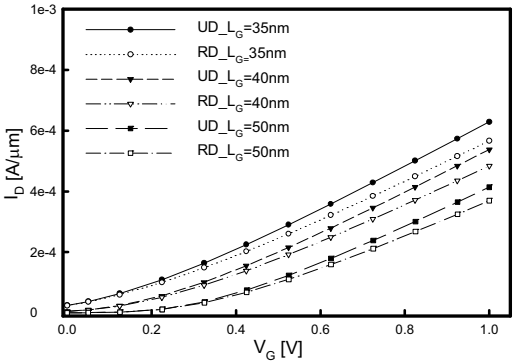
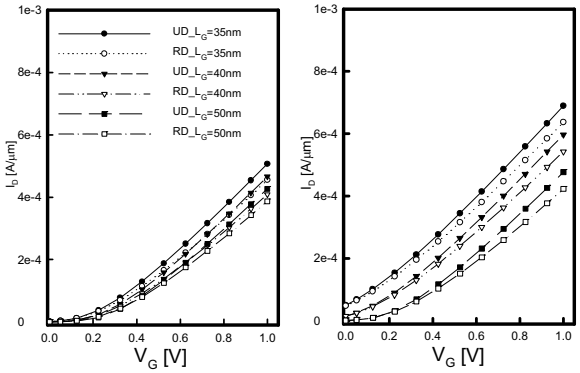
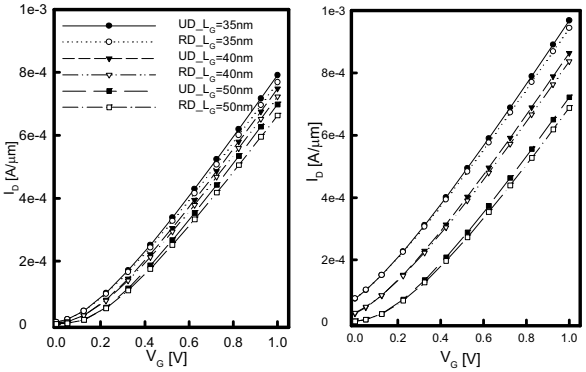



Figure 4. Simulated uniform and random dopant $I_D$-$V_G$ curves for MOSFETs with $T_{ox}$=3nm, $N_a$=$10^{18}$ $cm^{-3}$, $L_G$=50nm for $V_G$ = 1.0V, $V_D$=1.0V.




(a) (b)

Figure 5. Simulated uniform and random dopant $I_D$-$V_G$ curves for SOI with $T_{ox}$=3nm, $N_a$=$10^{18}$ $cm^{-3}$, $L_G$=50nm, $V_G$ = 1.0V, $V_D$=1.0V for (a) $T_{si}$=10nm and (b) $T_{si}$=20nm.




(a) (b)

Figure 6. Simulated uniform and random dopant $I_D$-$V_G$ curves for DG-MOSFETs with $T_{ox}$=3nm, $N_a$=$10^{18}$ $cm^{-3}$, $L_G$=50nm, $V_G$ = 1.0V, $V_D$=1.0V for (a) $T_{si}$=10nm and (b) $T_{si}$=20nm.

Threshold voltage variation with channel length and dopant fluctuation is illustrated in Fig. 7. Since random dopant induces drain current lowering, threshold voltage enlarges when random dopant is considered. The increment of $V_{TH}$ caused by random dopant is about 0.01 V for SOI and MOSFET. $V_{TH}$ variation of DG-MOSFET is only about 0.005 V. We may draw a brief conclusion herein, i.e., the operational properties of DG-MOSFET with a thin channel thickness are not sensitive to random dopant effects.

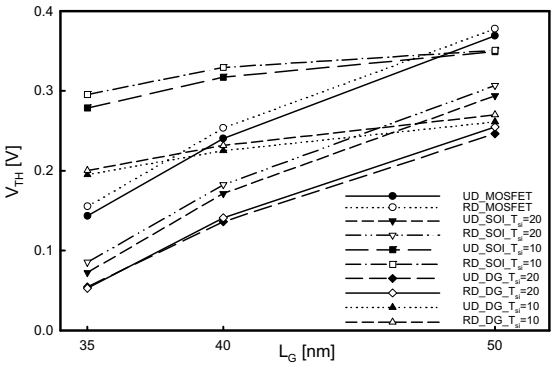



Figure 7. $V_{TH}$ curves for devices with uniform and random dopant concentration for $V_G$ = 1.0V, $V_D$=1.0V.

## 4 CONCLUSION

We have performed an investigation of $I_D$ and $V_{TH}$ variation with random dopant for single-gate MOSFET, SOI and double-gate MOSFET. The fluctuation of device characteristics cause by random dopant cannot be neglected while device simulation. Generally, a 5%~12% fluctuation of drain current exists. Among the three kinds of devices, SOI and DG-MOSFET with thin channel thickness are promising for CMOS technology at channel length below 50 nm. In this study, the simulated single-gate MOSFET is not with optimal designs of channel doping profile. A device with optimal channel engineering may present a better performance. In addition, the $V_{TH}$ and $I_D$ of DG-MOSFET with a thin channel thickness are not sensitive to random dopant effects. From the fabrication point of view, the unavoidable variation of manufacturing process may induce the fluctuation of device properties in deep sub-micron regime. DG-MOSFET may provide a solution for the difficult position .

## 5 ACKNOWLEDGEMENTS

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