Investigation of Local-Strain Effect of the Nano-Scale Triple Gate Si/SiGe and SiNx/Si Stacking MOS Transistor

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ABSTRACT

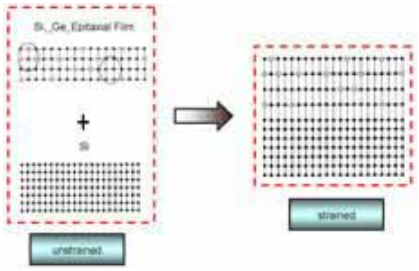
The tensile strained Si, based on the lattice misfit between Si and SiGe, gives higher speed and higher drive current for the metal oxide silicon field effect transistors. Based on the strained Si technology, a tri-gate CMOS transistor is further applied in the current leakage control and chip performance enhancement. Moreover, the "highly-tensile" silicon nitride capping layer is also applied for the strained Si applications. The stress from the silicon nitride capping layer is uniaxially transferred to the NMOS channel through the source-drain region to create tensile strain in NMOS channel.

This paper proposes a finite element method analysis to study the strain distribution of small island size (<200nm) of Si/SiGe strained silicon based tri-gate CMOS transistor and the "highly-tensile" SiN_x/Si stacking devices. In the tri-gate CMOS transistor case, the simulation results show that the bending effect from the edge can significantly affect the strain on the surface of the Si channel layer, and a compressive strain or reduced tensile strain occurs at the edge of the Si channel layer. Moreover, the results also indicate that the length of the Si/SiGe channel and the thickness of the Si/SiGe stack layers show significant effects of the strain distribution on the surface of the Si channel layer. In terms of the "highly-tensile" SiN_x/Si analysis, the results show that the "highly-tensile" silicon nitride could provide beneficial tensile strain for the channel of the NMOS transistor to enhance the device speed.

Keywords: Finite element method, strained silicon, silicon germanium, silicon nitride, lattice mismatch, thermally induced stress.

I. INTRODUCTION

New materials with enhanced electrical properties are desired for the ultra large scale integration (ULSI) process, but the cost and time to develop such new materials are often much higher than they are anticipated, and sometimes not affordable. Recently the local strain effect has attracted great attention for enhancing the properties of existing materials and provides a simple way to generate "new" materials. The tensile strained Si, based on either the lattice misfit between Si and SiGe[1], or the mechanical stress[2] gives high speed[3] and high drive current[4,5] for the metal oxide silicon field transistors (MOSFET). The continuous scaling of the ULSI devices and the various function devices on the same chip for system-on-chip applications, make it necessary to manipulate and design the strain condition on a local nano- or micro- meter area, with different conditions on Si wafers. As shown in Fig.1, when silicon is strained by Si/SiGe stacking, the electron mobility is enhanced by 23%.

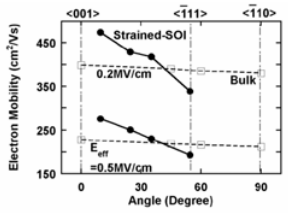


(a)

Silicon's lattice : $a_s = 5.431$ Å
Germanium's lattice : $a_g = 5.658$ Å
$Si_{1-x}Ge_x$'s lattice : $a_e = a_s*(1-x)+a_g*x$
According to the Vegard's law[6]:
Lattices mismatch :

$$f = \frac{a_e - a_s}{a_s} = 0.042 \cdot x$$

Fig.1(a): Lattice (mesh) diagram of the Si/SiGe stack

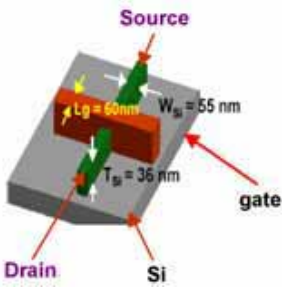


(b)

Fig.1(b): The electron mobility of strained-SOI MOSFETs has the maximum value along the <001> direction, and the mobility enhancement against that of the (110) bulk MOSFETs amounts to 23%[5]

At present, the advanced CMOS fabrication process towards to the 90nm scale. The conventional strain partition rule of Si/SiGe layers[6] used for large island size (>10 μm) is no more adequate for small island size (<200nm) due to the significant local-strain effect of the edge lattice distortion. Besides of the usage of Si/SiGe layer, a silicon nitride film with "highly-tensile" stress could be used for strained silicon application. The residual stress of silicon nitride film comes from the LPCVD or PECVD deposition, and it composes of two parts, intrinsic deposition stress and thermal stress[7]. The intrinsic deposition stress is athermal and develops at deposition temperature based on the deposition conditions, while the thermal stress develops on cooling from the deposition temperature as a result of the film-substrate CTE mismatch. By depositing a layer of silicon nitride on the surface of NMOS channel, the silicon on the surface would be strained, and therefore increase the speed and drive current.

The finite element method[8,9] can provide a numerical simulation to solve the global/local stress-strain behaviors, and can be used in future device design and fabrication. Two cases, the Si/SiGe strained silicon based tri-gate CMOS transistor and the "highly-tensile" SiNx/Si stacking devices with finite island sizes, are studied in this investigation (Fig2). An interesting edge bending phenomenon is discovered that has a significant effect on the small area island. These results are particularly important for small area devices in the future of the ULSI process.



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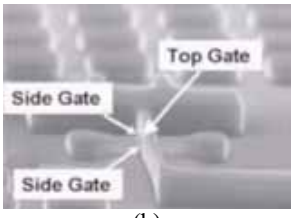

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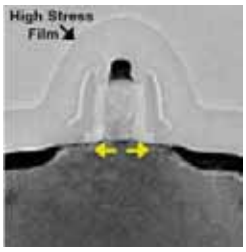


(c)

Fig.2: (a) Fully-depleted (FD) tri-gate CMOS transistors[10]. (b) Photo of a 30-nm tri-gate transistor[10]. (c) Photo of the "highly-tensile" SiN_x/Si strained NMOS channel[11].

II. FUNDEMENTAL THEORY OF FINITE ELEMENT METHOD

Using the principle of minimum potential energy, one can generate the equations for a typical static constant-strain finite element. The total potential energy is a function of the nodal displacements x, y and z such that $\pi_p = \pi_p$ (x, y, z). Here the total potential energy is given by

$$\pi_p = U + \Omega_b + \Omega_p + \Omega_s \tag{1}$$

where U, Ω_b, Ω_p and Ω_s represent the strain energy, the potential energy of the body force, the potential energy of the concentrated load and the potential energy of the distributed load, respectively. The above equation can be rewritten as a finite element integrated form:

$$\pi_p = \frac{1}{2}\iiint_V \{d\}^T[B]^T[D][B]\{d\}dV - \iiint_V \{d\}^T[N]^T\{X\}dV - \{d\}^T\{P\} - \iint_S \{d\}^T[N_S]^T[T_S]dS \tag{2}$$

where d represents the nodal vector, B is the strain-displacement matrix, D is the modulus of the elasticity matrix, N is the shape function matrix, X is the nodal displacement vector, P is the external load vector and T is the traction force matrix. The minimization of total potential energy with respect to each nodal displacement requires that

$$\frac{\partial \pi_p}{\partial \{d\}} = \left(\iiint_V [B]^T[D][B]dV\right)\{d\} - \iiint_V [N]^T\{X\}dV - \{P\} - \iint_S [N_S]^T[T_S]dS = 0 \tag{3}$$

namely,

$$\iiint_V [B]^T [D][B]dV)\{d\} = \iiint_V [N]^T \{X\}dV + \{P\} + \iint_S [N_S]^T [T_S]dS \quad (4)$$

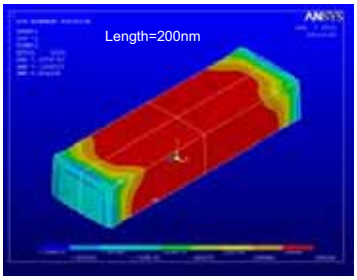
The Cauchy strain tensor for the updated Lagrangian description after a deformation u can be expressed as:

$$\varepsilon_{ij} = \frac{1}{2}\left(\frac{\partial u_i}{\partial x_j} + \frac{\partial u_j}{\partial x_i}\right) \quad (5)$$

Therefore, once d is obtained, the strain vector can be solved by ε = B d.

III. TRIPLE GATE SI/SIGE MOS TRANSISTOR STRAIN ANALYSIS USING FINITE ELEMENT METHOD

Fully-depleted (FD) tri-gate CMOS transistors with 60 nm physical gate lengths on SOI substrates have been fabricated by Intel (shown in Fig. 2(c)). The tri-gate design cuts down on current leakage by improving the electrostatics and short channel characteristics of the transistor. It can switch on and off much faster because of the design of raised source and drain structure for low resistance, and consumes far less power than conventional transistors. To increase the electron mobility, the FD tri-gate CMOS transistors can use strained-silicon at the surface of the channel covered by tri-gate.



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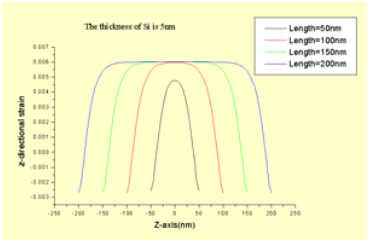

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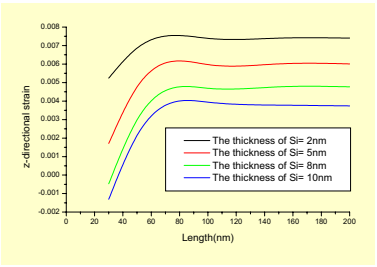

(c)

Fig.3: (a) The strain distribution of tri-gate CMOS transistor channel, and the strain distribution along z direction at the surface of silicon layer of various CMOS channel length (b), and silicon layer thickness (c).

Here we built a tri-gate CMOS transistor channel FE model (before the gate coverage material was deposited), shown in Fig3. An equivalent thermal expansion technique was applied to simulate the tensile strained silicon caused by the lattice misfit between Si and SiGe. According to the finite element method analysis, for a small island size, the bending effect from the edge can significantly affect the strain on the surface of Si channel layer, and a compressive strain or reduced tensile strain occurs at the edge of the Si channel layer (Fig 3(a)). This result indicates that, if the location of the MOS device on the top Si layer is not appropriately designed, the MOS device may be exposed to a compressive strain area, and so, on the contrary, reduce its speed. It is also pointed out that the conventional strain partition rule predicting a uniform tensile strain on the Si channel layer would not be suitable for a small island of strained silicon. Moreover, the simulation results also indicate that the length of the CMOS transistor channel (Fig. 3(b)) and the thickness of silicon layers (Fig 3(c)) show significant effects of the strain distribution on the surface of the Si channel layer. In the issue of the length of the CMOS transistor channel, it could be concluded that the length should be more than 100nm to extend the tensile strained area. In terms of the thickness of silicon layers, it is recommended that the thinner of the silicon layers, the more tensile strain is applied on the surface of silicon layers.

IV. SIN_X/SI STACKING MOS TRANSISTOR STRAIN ANALYSIS USING FINITE ELEMENT METHOD

A "highly-tensile" silicon nitride capping layer is also utilized to make strained silicon to improve the NMOS transistor performance. It consists of two different parts of residual stresses. The intrinsic deposition stress, which is tensile, develops at deposition temperature based on the deposition conditions, and the thermal stress develops on

cooling from the deposition temperature as a result of the film-substrate CTE mismatch.

In this research, there is a two-steps approach to simulate the silicon nitride deposition and its induced residual stress, shown in Fig. 4. First we introduced a pre-stress on the silicon nitride layer as the intrinsic deposition stress at deposition temperature (about $400°C$), and then cooled down to room temperature. The results show that the maximum x-directional strain of NMOS channel is 0.6% as the model is given 1GPa of the pre-stress under a temperature loading of -400K. Furthermore, the fabrication cost of the "highly-tensile" SiN_x is lower than that of the Si/SiGe stacking. Therefore, it could be concluded, the "highly-tensile" silicon nitride could not only provide beneficial tensile strain for the channel of the NMOS transistor to enhance the device speed, but also show the cost effective advantage for the fabrication.

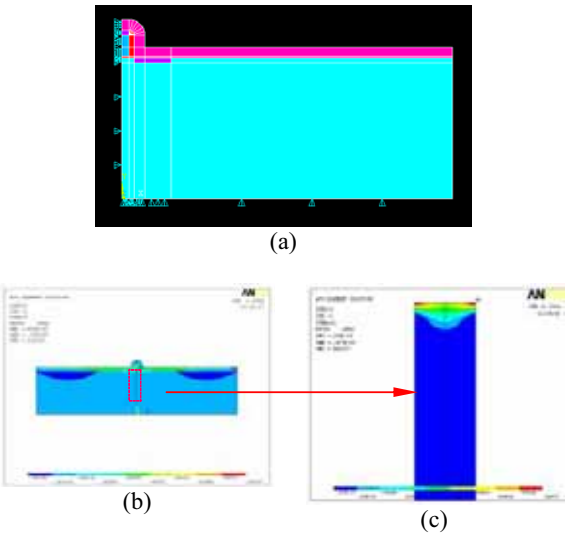

Fig. 4: (a) The 2D FEM model of NMOS transistor with "highly-tensile" SiN_x/Si capping layer, (b) The simulation result of tensile residual stress (c) The details of strain distribution on the surface of NMOS channel.

V. CONCLUSION

In this study, a novel finite element method based analysis has been applied to study the strain distribution when a small silicon island is stacked with either silicon germanium (SiGe) or silicon nitride (SiN_x). The simulation results revealed that the conventional strain partition rule of Si/SiGe layers with predictions of uniform strain distribution in the in Si/SiGe interfaces is no more adequate for small island size (<200nm) due to the significant local-strain effect of the edge lattice distortion. Moreover, the length of the Si/SiGe channel and the thickness of the Si/SiGe stack layers show significant effects of the strain distribution on the surface of the Si channel layer. Besides silicon germanium, a "highly-tensile" silicon nitride film could also be utilized to the strain silicon applications. The two-steps FEM simulation indicates there is the beneficial tensile strained area on the surface of NMOS Si channel when SiN_x layer is deposited.

VI. REFERENCE

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