CMOS Architectures for NOR & NAND Logic Gates Using Single Electron Transistors

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ABSTRACT

Single electron transistor (SET) is one of the nano devices suitable for developing nano-scale logic circuits. In this paper, CMOS architectures for NOR and NAND gates have been proposed using SET's and their operational characteristics have been verified by using the simulation model SET-SPICE. First, a two-input NOR gate was designed and verified and then the design was extended to implement a NOR3 gate and a NAND2 gate. The basic layout of a SET is a small conducting island coupled to the source and drain leads by tunnel junctions that are capacitively coupled to a control gate and one or more input gates. Operation of an SET as an "n" and a "p" device was achieved by controlling the charge on the SET island. This charge is related to the capacitance at the island, capacitance at the gate electrode and the voltage applied to the gate. The effects of temperature, island capacitance and the ability of the proposed gate to drive load capacitance have also been studied.

Keywords: single electron transistors (SET), CMOS, logic devices

1 INTRODUCTION

Nano-scale devices show potential for low power, high speed at a size much lower than current day CMOS [1, 2]. The popular nano-devices that are explored for logic circuit applications are carbon nanotube transistors, nanowire FETs, quantum dots and single electron transistors (SET). Quantum dots and single electron transistors can be combined into a single category called Single Electron Devices, which work on the principle of controlling the movement of a single electron.

Single electron transistors use quantum effects to perform operations similar to conventional CMOS transistors. In order to use these devices to perform logic operations it is required to realize operation identical to the MOSFET. Earlier logic designs [3-6] based on SET's have used architectures different from CMOS to realize simple logic gates, except to an inverter [7]. This will require developing architectures different from CMOS for each logic gate/operation. In this paper CMOS architecture based NOR and NAND gate has been proposed and operation verified using the simulation model SET-SPICE [8]. This model, developed by researchers at Delft University in Netherlands, makes use of the most popular circuit simulator called SPICE and incorporates a text-based model for single electron transistors.

The basic layout of an SET (Fig. 1) is a small conducting island coupled to the source and drain leads by tunnel junctions that are capacitively coupled to one or more gates. Single electron movement deals with a small amount of excess electrons on islands changing their distribution over time. The charges in single-electron devices are transported in a quantized way rather than continuously. Complementary operation of these devices can be achieved by controlling the charge on the island. The charge on the island is related to the capacitance at the island, capacitance at the gate electrode and the voltage applied to the gate.

In-order to obtain biasing voltage at the gate for complementary operation of the SET, current oscillations where observed for V_{cc} = 15 mV and V_{ee} = 0 V with C_{j1} = C_{j2} = C_{g1} = C_{g2} = C_0 = 10^{-18} F and R_t = 10^9 Ω. Voltage at the gate was varied from 0 to 1V and the corresponding current oscillations where observed. Based on this simulation it was found that gate bias has to be around 0.1V for the SET to operate as NMOS and it has to be around 0.3V for PMOS operation.

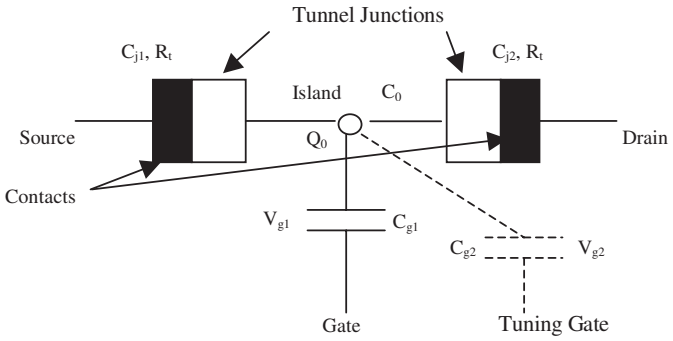

Fig. 1: A Schematic Diagram of a SET

2 DESIGN OF A NOR2 GATE

The NOR2 gate consists of four single electron transistors and was based on the complementary logic as shown in Fig. 2. Device parameters including V_{cc} and V_{ee} were set to values as mentioned in the previous section. All possible logic combinations for a two-input NOR gate were tested at the input. Logic '1' is represented by a 25 mV signal and the logic '0' is represented by ground at the input. The waveforms corresponding to the input and output as in SET-SPICE are shown in Fig. 3, which verify the NOR2 operation. At the output, logic '1' charges up to V_{cc}, while logic '0' is pulled down to ground. Based on these results, this design was extended to a 3-input NOR gate. These simulations where done at a temperature of 4.2°K.

3 DESIGN OF A NOR3 GATE

This design consists of three P-SET's in series and three N-SET's in parallel with a total of six transistors in similar to the CMOS based NOR3 gate. The parameters and the voltage levels at the input were similar to the previous simulation. The I/O waveforms for this circuit are shown in Fig. 4, which verifies a NOR3 logic operation.

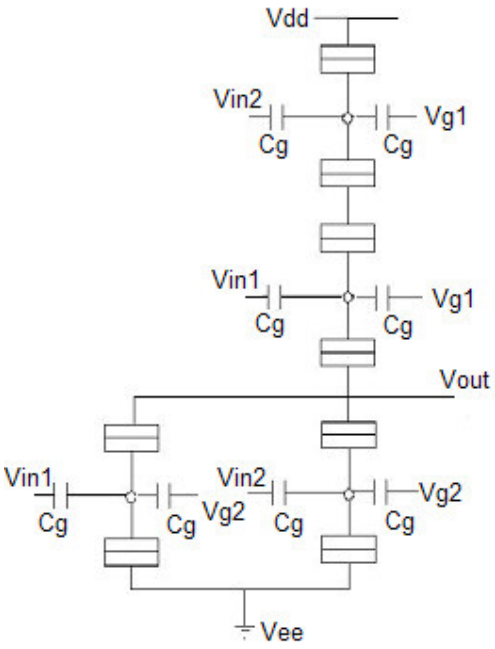

Fig. 2: NOR2 gate architecture

4 DESIGN OF A NAND2 GATE

CMOS architecture equivalent NAND2 gate was designed with SET's using four transistors. The NAND2 gate was also simulated with identical bias conditions as of the NOR2 gate. The device parameters for junction capacitance and resistance were also identical to the NOR2. The I/O waveforms of the NAND2 gate are shown in Fig. 5.

5 SIMULATION RESULTS

5.1 Dependence on Island Capacitance

The island capacitance was varied from 10^{-20} F to 10^{-18} F and the output was observed. A $C_0 = 10^{-19}$ F provided optimal results for both the NOR and NAND gates. This value translates to an island size of about 2 nm. The I/O waveforms of the NOR2 gate at $C_0 = 10^{-19}$ F are shown in Fig. 6.

5.2 Dependence on Load Capacitance

Similarly the load capacitance at the output was also varied between 10^{-18} F and 10^{-12} F. The results showed that the devices could drive a load of about 10^{-15} F. When the load capacitance was increased between 10^{-14} F and 10^{-12} F the waveform did not match with the normal gate operation as earlier.

5.3 Dependence on Temperature

The simulation temperature was at 4.2°K for the initial simulations. When the operating temperature was increased, useful results were obtained till about 10°K. If the temperature was increased further the logic '0' voltage level at the output shifted further away from zero and similarly the voltage level of logic '1' shifted downwards away from Vcc. The I/O waveforms for the NOR2 gate at 20°K having undesirable voltage level shifts at the output are shown in Fig. 7.

6 SUMMARY AND CONCLUSION

The CMOS architecture based NOR2, NOR3 and NAND2 gates have been designed with SET's and simulated using SET-SPICE model. The effects of the temperature, island and load capacitance were also studied.

ACKNOWLEDGEMENT AND DISCLAIMER

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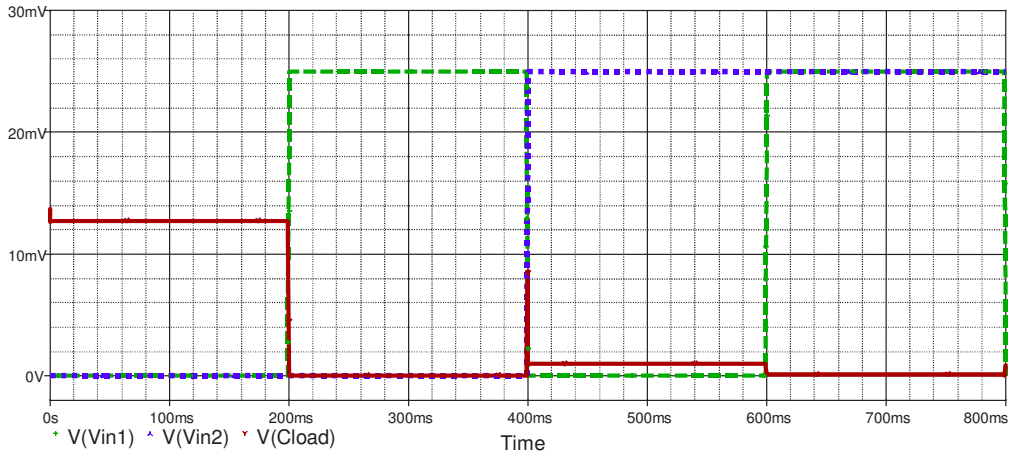

Fig. 3: I/O waveforms for the NOR2 gate at 4.2°K using SET-SPICE, $C_0=10^{-18}$F

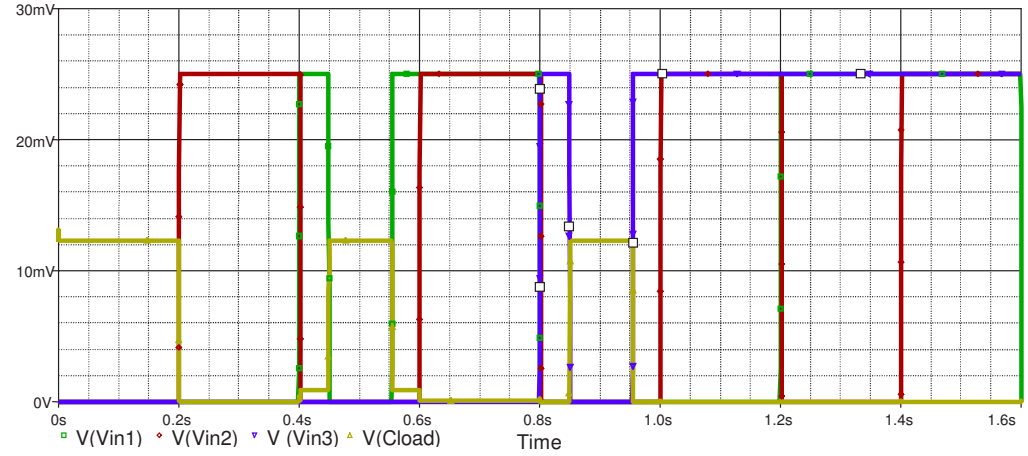

Fig. 4: I/O waveforms for the NOR3 gate at 4.2°K using SET-SPICE, $C_0=10^{-18}$F

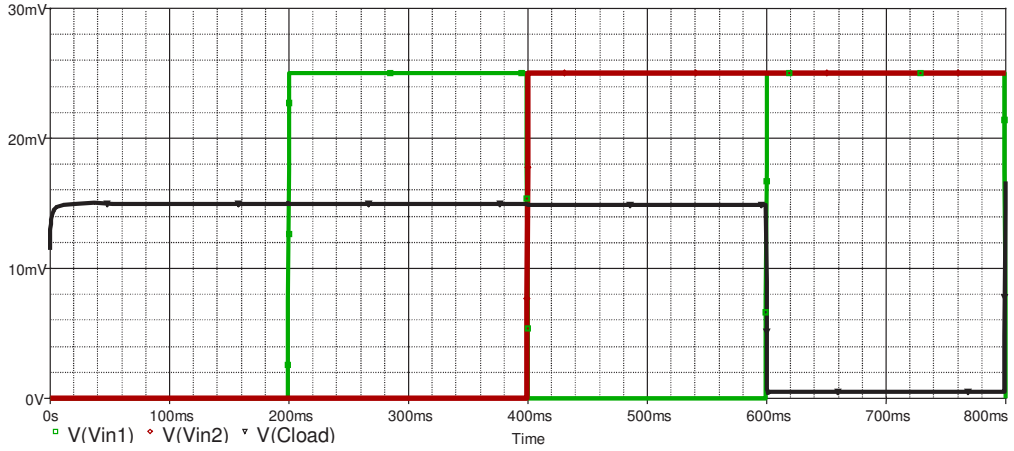

Fig. 5: I/O waveforms for the NAND2 gate at 4.2°K using SET-SPICE, $C_0=10^{-19}$F

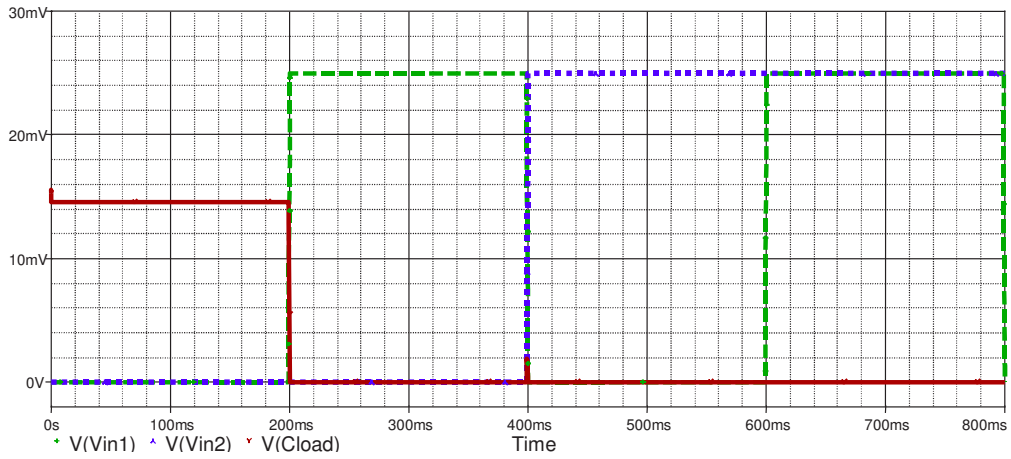

Fig. 6: I/O waveforms for the NOR2 gate at 4.2°K using SET-SPICE, $C_0=10^{-19}$F

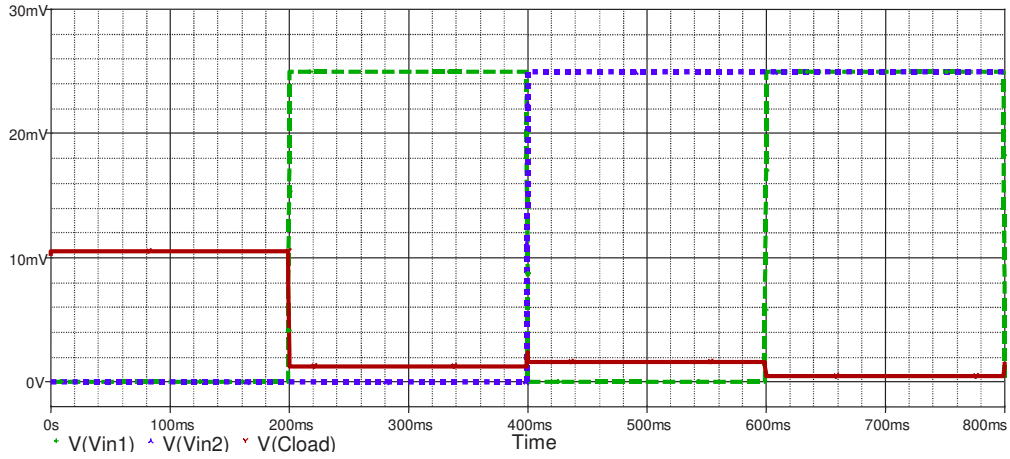

Fig. 7: I/O waveforms for the NOR2 gate at 20°K using SET-SPICE, $C_0=10^{-19}$F

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