Improved Compact Model for Four-Terminal DG MOSFETs

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ABSTRACT

This paper reports improvements of the compact model for double-gate field-effect transistors (DG MOSFETs). The improvements make the model more accurate for wider range of device dimensions and device operation conditions.

Carrier density calculation at the source-end is modified to the model applicable for wide range of gate voltages. By this modification, iteration counts for Newton's method are also drastically reduced. Two approaches to construct the transport equations, unified and separate current methods, in the channel are compared. Conventional charge-sheet model leads to too thin carrier density at the drain-end with unphysical high carrier velocity. Transport equation with velocity saturation and explicit drain electric field is proposed. Simulation result based on this equation is demonstrated.

Keywords: MOSFET, double-gate, compact modeling

1 INTRODUCTION

Double-gate field-effect transistors (DG MOSFETs), which have two insulating gates sandwiching a Si-channel, as shown in Fig. 1, have gained much attention as a promising device structure with excellent scalability because of its minimum short channel effect [1]. Beside the use of DG MOSFETs as three-terminal transistors with one electrically-common gate, we have proposed and demonstrated that four-terminal operation of DG MOSFETs is promising [2], [3]. This operation mode enables fine-grain dynamic threshold-voltage (V_t) control and sophisticated use for analog signal processing. To evaluate these merits, we developed a compact four-terminal DG MOSFET model by adopting the double charge-sheet model [4]. This model deals with four-terminal operation of DG MOSFETs of both symmetrical and asymmetrical double-gate structure. We tested this model with the device simulator (ATLAS) results for long-channel DG MOSFETs, and found that it describes the characteristics of the transistor in good accuracy. In this presentation, we report the improvement of the model to make it more accurate for wider range of device dimensions and device operation conditions.

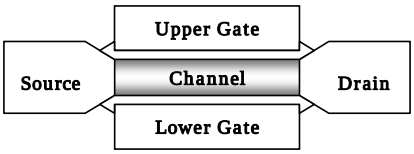

Fig. 1 Cross-sectional view of the DG MOSFET

2 SOURCE CARRIER DENSITY

For the charge-sheet model, the first step is to calculate the potential ψ at the source-end. It is achieved by solving one dimensional Poisson equation along the axis x perpendicular to the silicon/oxide interface.

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{q}{\varepsilon_s} n_i e^{\beta\psi} \tag{1}$$

where n_i is the intrinsic carrier density, q is the unit charge, ε_s is the dielectric constant of silicon, β is q/kT (k is Boltzmann constant, T is the temperature). By integrating this equation, we obtain an expression about the channel thickness d.

$$\begin{aligned} d &= s2 - s1 = (s2 - x_M) + (x_M - s1) \\ &= \int_{\psi_M}^{\psi_{s2}} \{F_2(\psi)\}^{-1/2} \partial\psi + \int_{\psi_M}^{\psi_{s1}} \{F_1(\psi)\}^{-1/2} \partial\psi \end{aligned}, \tag{2}$$

where

$$F_1(\psi)=\left(\frac{C_{OX1}}{\varepsilon_s}(V_{G1}-\psi_{s1})\right)^2+\frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi}-e^{\beta\psi_{s1}}\right),$$
$$F_2(\psi)=\left(\frac{C_{OX2}}{\varepsilon_s}(V_{G2}-\psi_{s2})\right)^2+\frac{2qn_i}{\varepsilon_s\beta}\left(e^{\beta\psi}-e^{\beta\psi_{s2}}\right).$$

In these equations, $s1$ and $s2$ stand for the upper and the lower silicon/oxide interface, x_M stands for the potential minimum. C_{OX1} (C_{OX2}) and V_{G1} (V_{G2}) are the gate capacitance and gate voltage of the upper (lower) gate. F_1 and F_2 become identical when the exact pair of the surface potentials ψ_{s1} and ψ_{s2} is given. These equations are used to determine two surface potentials.

The integrations in (2) give the analytical expressions as

$$\int_{\psi_M}^{\psi_{s2}}\{F_2(\psi)\}^{-1/2}\partial\psi = \frac{2}{\beta\sqrt{-F_2(-\infty)}}\tan^{-1}\left(\frac{C_{OX2}(V_{G2}-\psi_{s2})}{\varepsilon_s\sqrt{-F_2(-\infty)}}\right), \quad (3)$$

which represents the distance between $s2$ and x_M, and (2) implies that the total channel thickness is divided to two charge sheets. But when there is only one charge-sheet, x_M is not in the channel, and (2) becomes subtraction of two positive value. Also if $F(-\infty)>0$, which occurs when there is only one lightly populated charge-sheet, the integration of (1) is

$$d=\frac{1}{\beta\sqrt{F(-\infty)}}\left|\log\left(\frac{(C_{OX1}/\varepsilon_s)|V_{G1}-\psi_{s1}|-\sqrt{F(-\infty)}}{(C_{OX1}/\varepsilon_s)|V_{G1}-\psi_{s1}|+\sqrt{F(-\infty)}}\right)-\log\left(\frac{(C_{OX2}/\varepsilon_s)|V_{G2}-\psi_{s2}|-\sqrt{F(-\infty)}}{(C_{OX2}/\varepsilon_s)|V_{G2}-\psi_{s2}|+\sqrt{F(-\infty)}}\right)\right| \quad (4)$$

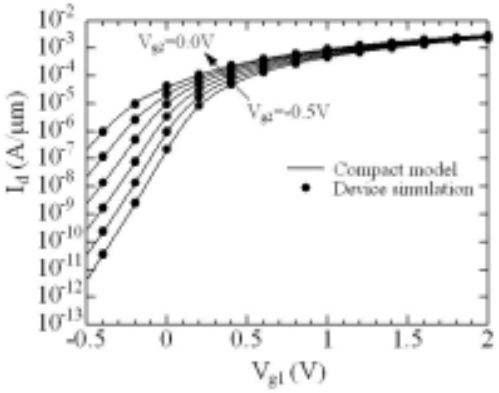

Figure 2 I-V characteristics of the DG MOSFET.

where F stands for either F_1 or F_2. Both equations (3) and (4) confront computational difficulty if $F(-\infty)\approx 0$. In this case, another form

$$d=-\frac{2}{\beta}\left(\frac{\varepsilon_s}{C_{OX1}(V_{G1}-\psi_{s1})}+\frac{\varepsilon_s}{C_{OX2}(V_{G2}-\psi_{s2})}\right) \quad (5)$$

can be used. With this set of equations, calculation of (1) becomes robust accepting highly unbalanced pair of gate voltages. At the same time average count of iteration for the Newton's method drastically decreased to about 8.

The calculation results are then used as the boundary condition for the carrier transport equation for the channel. Since the relation between the surface potential and the charge-density obtained by this calculation is not hold under the charge-sheet approximation, some adjustments are needed. We found that we have to abandon the surface potential accuracy at the source-end to keep the charge density accuracy. Fig. 2 is the simulation result obtained after these improvements.

3 TRANSPORT EQUATION

Electron transport in the channel is described as

$$\begin{aligned}-I_D &= I = I_1 + I_2 \\ &= q\left(-\mu_1\frac{\partial\psi_{s1}(y)}{\partial y}n_1(y)+D_1\frac{\partial n_1(y)}{\partial y}\right) \\ &\quad + q\left(-\mu_2\frac{\partial\psi_{s2}(y)}{\partial y}n_2(y)+D_2\frac{\partial n_2(y)}{\partial y}\right)\end{aligned} \quad (6)$$

where y is the axis along the channel with the origin y=0 at the source end, I is the total current, I_1 (I_2) and μ_1 (μ_2) are the current and the electron mobility of charge-sheet 1 (2), and D_i ($=\mu_i kT/q$) is the diffusion coefficient. Relationship between the surface potential and the carrier density in the channel is, under the gradual channel approximation:

$$\begin{aligned}\Delta\psi_{s1} &= -qn_1/C_{11}-qn_2/C_{12} \\ \Delta\psi_{s2} &= -qn_1/C_{21}-qn_2/C_{22}\,.\end{aligned} \quad (7)$$

where C_{11},C_{12},C_{21} ($=C_{12}$), and C_{22} are the constants with the dimension of the capacitance. If $\mu=\mu_1=\mu_2$ holds, (6) can be rewritten as follows:

$$I=q\mu\left(-\frac{1}{C_{11}}\frac{\partial n_1}{\partial y}n_1-\frac{1}{C_{22}}\frac{\partial n_2}{\partial y}n_2-\frac{1}{C_{12}}\frac{\partial(n_1n_2)}{\partial y}+\frac{kT}{q}\frac{\partial(n_1+n_2)}{\partial y}\right). \quad (8)$$

This can be integrated easily.

Although this approach gives exact result, it is not practical for many situations. It is because the surface

mobility is the strong function of the gate voltage. The mobility is also affected by the interface characteristics, and the interface characteristics may not be identical for device processing reason. To calculate two channels separately will be, therefore, more practical even if it is less accurate. In that case, relationship between n_1 and n_2 is necessary to simplify (7). Linear relationship as

$$n_1(y)/n_1(0)=n_2(y)/n_2(0) \tag{9}$$

was found to give accurate-enough approximation. Using this approximation, the transport equation becomes the sum of two transport equations.

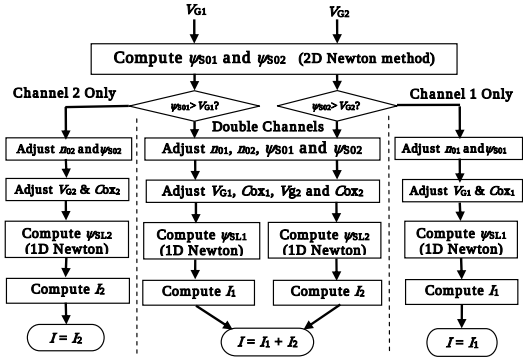

Figure 3 Computational algorithm of the double charge-sheet model of separate current method.

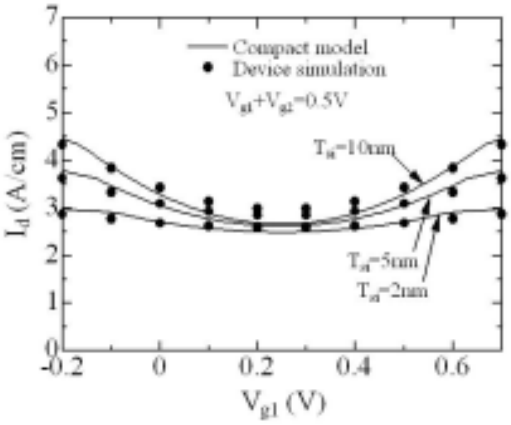

Fig. 4 Drain current change by the asymmetric gate voltages for 2, 5 and 10 nm thick Si channels. Drain voltage is 1V. Solid lines are for compact model results, and symbols are for the ATLAS results.

$$-I_D = I = I_1 + I_2$$
$$I_i = q\left(-\mu_i \frac{\partial \psi_{si}(y)}{\partial y} n_i(y) + D_i \frac{\partial n_i(y)}{\partial y}\right) \tag{10}$$

Fig. 3 shows the computational algorithm of the double charge-sheet model of separate current method. In the figure, adjustment stage of the gate voltages and capacitances are shown. It is necessary because the relation between the surface potential and the carrier density is, after adopting (9), described by an effective gate voltage and an effective gate capacitance.

Fig. 4 shows change in saturation current when the two gate voltages are varied while maintaining $V_{G1}+V_{G2}$ constant. Since the sum of two gate voltages is constant, the total channel charge does not change significantly, and the total current should remain relatively constant if the conduction mode is volume conduction. As shown in the figure, the total current has a distinct minimum value at $V_{G1}+V_{G2}$ for a thick Si channel is thick, whereas the total current remains relatively constant for thin Si channels. This shows that the proposed compact model accurately reproduces the transistor characteristics in both surface conduction and volume conduction regions.

Two kinks can be seen in the figure for all curves, corresponding to the single/double charge-sheet boundary. These kinks are caused by the approximation that the charge-sheet resides strictly at the interface, which is not rigorously true. Although these kinks do not have serious effects in the digital circuit simulation, care should be taken when the model is used for simulating analog circuits that use two gates for signal mixing.

4 SHORT CANNEL EFFECT

To make the model applicable to the short-channel device causes another problem. Conventional charge-sheet model assumes carrier density equilibrium between the drain and the channel at the drain-end as:

$$V_D = \psi_s(L) - \psi_s(0) + \frac{1}{\beta}\ln\frac{n(0)}{n(L)} \tag{11}$$

Although the expression describes small V_D subthreshold characteristics, it leads to the unphysical high carrier velocity when V_D becomes high. In other words, the conventional charge-sheet model is incompatible with the velocity saturation. To circumvent this problem we have to introduce the velocity saturation and the explicit drain electric field at the same time.

One simple form of the relation between carrier velocity v and the lateral electric field is

$$v = -\mu E / 1 + |E / E_c| \tag{12}$$

where E_c is the saturation electric field, and μ in this form is the low field mobility. This relation is reported to be accurate for PMOS and bulk n-type silicon. For NMOS channel electron, a more accurate form is known. In this paper, we adopt this form because of analytical simplicity. The transport equation including this effect is

$$-\mu\frac{\partial(\psi_s+\phi_s)}{\partial y}n+\mu\frac{kT}{q}\frac{\partial n}{\partial y}=\frac{I}{q}+\frac{I}{qE_c}\frac{\partial(\psi_s+\phi_s)}{\partial y}, \quad (13)$$

where ϕ_s is the drain electric field approximately have the form:

$$\phi_s(y)=\Delta\psi\exp(a\pi(y-L)/(d+t_{OX1}+t_{OX2})) \\ \Delta\psi=V_D-(\psi_s(L)-\psi_s(0)) \quad (14)$$

where L is the channel length, t_{OX1} and t_{OX2} are the gate insulator thickness, and a is a constant around 1. Equation (13) can be integrated much the same way as conventional transport equation, and the result is the same except by replacing the current term as

$$IL\rightarrow I\left(L+\frac{V_D}{E_c}\right)+\mu q\int_0^L\frac{\partial\phi_s}{\partial y}ndy. \quad (15)$$

The second term can be integrated using following approximation obtained by supposing that the diffusion current is negligible where the drain electric field is significant:

$$n(y)=n(L)\left(\frac{E(L)}{1+|E(L)/E_c|}\right)\Big/\left(\frac{E(y)}{1+|E(y)/E_c|}\right). \quad (16)$$

The result is as follows.

$$IL\rightarrow I\left(L_{eff}+\frac{V_D-\Delta\psi}{E_c}\right) \quad (17)$$

In the formula, L_{eff} is the point where $\psi_s/dy=\phi_s/dy$. Short channel effect is expressed that the channel length L is replaced to shorter L_{eff} causing larger drain current. On the other hand, $(V_D-\Delta\psi)/E_c$ describes the velocity saturation effect.

Fig. 5 shows transistor characteristics using this equation together with the separate current method. In the figure, the solid line is the result with no velocity saturation, whereas the dashed line is the result with velocity saturation and with explicit drain electric field. The result gives the smaller current mainly because of relatively low velocity near the velocity-saturation region inherent in (12). Still, excellent suppression of short channel effect characteristic of DG MOSFET is demonstrated distinctively.

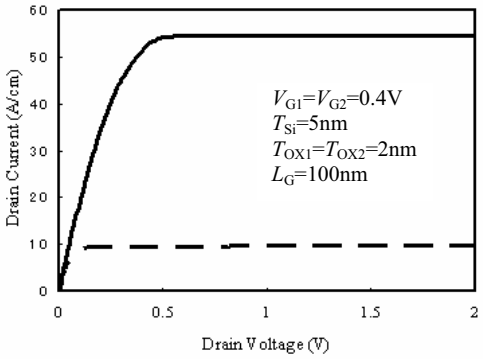

Fig. 5 Transistor characteristics without velocity saturation (solid line), and with velocity saturation and with explicit drain voltage (dashed line).

5 SUMMARY

Improvement of the compact modeling for the double-gate field-effect transistors was presented. Calculation of the carrier density at the source-end for a wider range of gate voltage was discussed. Reduction of the iteration count was achieved. Transport equations both for unified and separated current methods are compared. Velocity saturation effect was introduced in the transport equation, together with the short channel effect at the drain end. It was found that the analytical and simple form can be obtained. Compact model based on the equation was implemented.

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