Monte Carlo and Energy Balance Simulations of Deep Sub-micrometer Conventional and Asymmetric MOSFET Device Structures

Anand Mannargudi and Dragica Vasileska

Department of Electrical Engineering
Arizona State University, Tempe, AZ 85287-5706, USA
anandmm@asu.edu , vasileska@asu.edu

ABSTRACT

Device simulations are essential to explore new device designs, optimize performance and understand underlying physics. As we scale the gate lengths of deep sub micrometer devices, there are always contradicting requirements of increased hot carrier reliability and reduced short channel effects. These contradicting requirements have led semiconductor device engineers towards asymmetric device structures. Typical methods employed to simulate such devices include commercial simulation software such as ATLAS and Monte Carlo particle-based simulations. In this work, we have simulated conventional and highly asymmetric 100nm n-channel Focused-Ion-Beam MOS device(FIBMOS)[1]. As a second effort we have pushed the gate length of this asymmetric device down to 50nm and compared the results with that of a conventional MOS device of the same gate length.

Keywords: Monte Carlo, asymmetric device structure, FIBMOS.

1 INTRODUCTION

1.1 Market Forces and the State of the Art

Semiconductor Industry (SIA) projects that by the end of 2012, leading edge production devices will employ 25nm gate lengths and have an oxide thickness of 1.5nm or less. There have been a lot of improvements in MOSFET scaling, but as these devices transfer from laboratory to commercial applications, accurate device simulations will be essential to come up with new device designs and improve their performance. As device dimensions tend to reduce there are always additional problems that unfold each day such as gate depletion, transconductance degradation, problems due to surface roughness, tunneling effects that result in large off-state current, interface in-homogeneity and quantum mechanical space quantization effects. Hence, in modern technological world we can clearly say that device simulations are indispensable as they provide with the possibility to test hypothetical devices which could not be or which are yet to be manufactured. The downward scaling of the gate length towards smaller lengths have always associated a device engineer to encounter the previously mentioned contradicting requirements. In general the effect of hot carrier reliability is increased by using reduced substrate doping and that of the short channel effect by increased substrate doping. Advancements in epitaxial growth recently have lead us to the development of asymmetric devices that satisfy these contradicting requirements. Further, the trade-off between reliability and performance, inherent to drain engineering can be optimized by using optimal doping profiles in these asymmetric device structures.

1.2 Asymmetric Device Structures

There has been a vast amount of theoretical and experimental effort to predict optimal device structures that can operate at higher drain voltages and do not exhibit pronounced short channel effects. Some representative devices proposed are summarized in Figure 1 and include Lightly-doped drain (LDD) devices, gate overlapped LDD structure (GOLD), halo source GOLD drain (HS-GOLD) [2] and graded channel MOS (GCMOS) [3] devices. The last device overcomes the incompatible requirements of short channel effects and hot-carrier resistance.

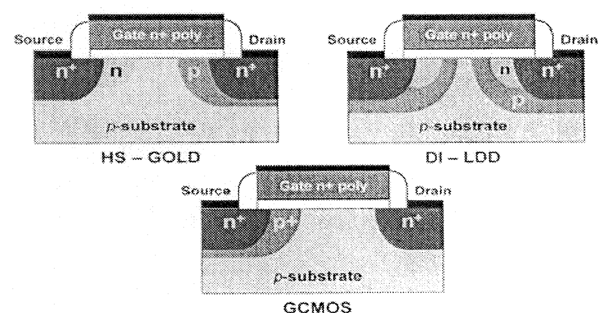


Figure 1: Halo source GOLD (Hs-GOLD), Dual implant lightly-doped drain (DI-LDD) and graded-channel MOS (GCMOS) devices.

With significant number of investigations, we have downscaled the device structure proposed by Knezevic *et al* [4], down to 100nm. We have further pushed

gate length of this device to 50nm. The description of the simulated device is schematically shown in Figure 2.

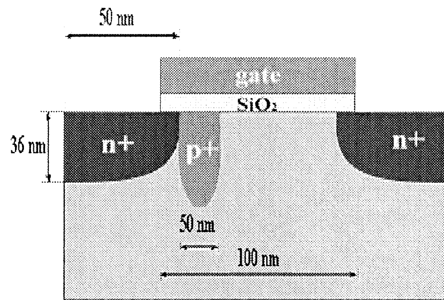


Figure 2: Schematic description of the simulated Focused-Ion-Beam (FIBMOS) device structure with gate length of 100nm, oxide thickness t_{ox} =2.1nm, source and drain doping $n^{+}=1\times10^{19}$ cm^{-3} and doping of the FIB implant of $p^{+}=1.4\times10^{18}$ cm^{-3}.The substrate doping equals $1\times10^{16}cm^{-3}$.

2 METHODOLOGIES

The Monte Carlo model is based on usual *Si* band structure for three dimensional electrons, in a set of non-parabolic Δ- valleys with energy dependent effective masses. The six conduction band valleys inherent to silicon band structure are included through three pairs, with valley 1 pointing towards the (100) direction, valley 2 pointing towards (010) direction and the final valley in (001) direction. The longitudinal and the transverse mass is very important in this case and they have been included using the Herring-Vogt transformation [5]. It is well known that the intravalley scattering is limited to acoustic phonons, but for intervalley scattering we have included both *g* and *f* – phonon processes. Although three zeroth-order *f* -phonons and three zeroth-order *g*-phonons with various energies are assumed [6], we know that by group symmetry considerations the zeroth-order low energy *f* and *g*-phonon processes are forbidden. Having taken this group symmetry into account we have considered two high-energy phonons and two low-energy *f* and *g*-phonon processes. Nevertheless, the two high-energy phonon scattering process are included through the zeroth-order interaction term, while the low-energy phonon through first order process [7] as it gives significant contribution for high energy electrons. At low temperatures, we have also considered low-energy phonons as they give a smooth velocity saturation curve. The phonon energies and the coupling constants in our model are determined so that experimental temperature-dependent mobility and velocity field characteristics are consistently recovered [8].

The incomplete Lower-Upper decomposition has been used for the solution of the 2D Poisson's equation. The Monte Carlo simulation has been used to obtain the charge distribution in the device. The electric fields are calculated in the free flight portion of the Monte Carlo transport kernel and the charges obtained are distributed within continuous mesh instead of discrete grid points. The particle mesh method is used to perform the switch between the continuum in a cell and discrete grid points at the corners of the cell. The charge assignment has been carried out using Nearest-Grid-Point (NGP) and the Cloud-in Cell (CIC) scheme[9]. The choice of these methods basically depends upon the factor that the charge assignment scheme must maintain zero self-forces and good spatial accuracy of the forces. The device current is determined by taking the sum of electron velocities in a portion of the device. For this purpose the device has been divided into several sections along the x-axis (along the channel). After each free-flight time step the number of electrons and their corresponding velocities are added up. The current at a particular section is determined by the average of the velocities of each carrier in that section. The total device current is determined from the average of several sections. We have also taken into account the sections near the source and drain where high y-components might exist. The average energy of the carriers is also computed in the same manner. Coulomb and surface roughness scattering are not included in this model as they tend to mask the performance of the device.

Regarding the choice of the model within the Silvaco simulation platform, the use of conventional drift-diffusion model might sound good for long channel devices. However, as we enter the era of nano-electronics devices, one has to take into consideration the "non-local" effects, such as velocity overshoot and reduced energy dependent impact ionization. Hence, for the 100nm and 50nm channel length devices, we have utilized the energy balance model, as it gives more accurate description of non-stationary transport. The significance of this model is that the energy loss rates define the physical mechanisms by which the carriers exchange energy with surrounding lattice. Using 2D Silvaco ATLAS energy balance model and 2D Monte Carlo particle-based simulations, we examine hot electron reliability of the FIBMOS devices. This problem is severe in deep sub-micrometer devices in which large substrate doping is used to prevent (for example in conventional MOS device) the punch-through effect, which in turn leads to large electric fields and enhanced impact ionization effect at the drain end. Further problems arise from the fact that the holes generated by this process give rise to undesirable substrate current. Both 2D Silvaco ATLAS and Monte Carlo simulations show that the built in electric field due to presence of the p^{+} implant highly influence the drive-current capabilities of the FIBMOS compared to the conventional one.

3 SIMULATION RESULTS

The output characteristics of the conventional and FIBMOS device, obtained via Silvaco ATLAS simulations are shown in Figure 3. These simulation results shown for channel length of 100nm with substrate doping of 5×10^{17} cm^{-3} for conventional MOS and 8×10^{15} cm^{-3} for the FIBMOS device. Figure 3 (a) suggests that one can use significantly lower substrate doping in the FIBMOS device and still achieve almost identical device performance. But

as we go down for a lower gate length of 50nm as shown in Figure 3 (b) we observe that for the same substrate doping concentration the FIBMOS exhibits improved output resistance (evident from slope of the output characteristics). The reduced current in FIBMOS device of both cases may be attributed to the presence of p^+ implant near the source end.

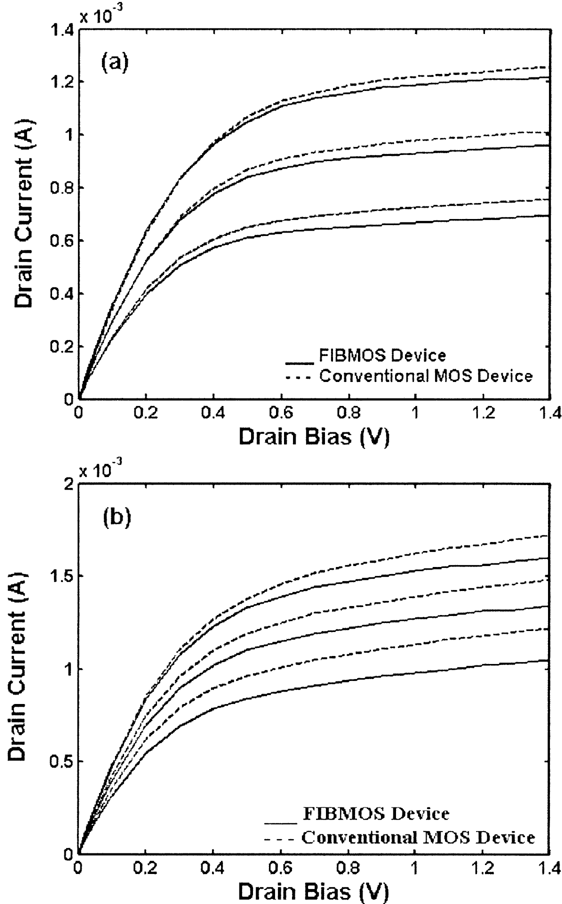


Figure 3: Simulated I-V characteristics of conventional MOS and FIBMOS device (a)for 100nm and (b)for 50nm.

It is worth pointing out that the energy balance simulation results are strongly affected by the choice of the energy relaxation time. This is shown in Figure 4, where we compare Monte Carlo and energy balance simulations for two different values of the energy relaxation time (0.1 and 0.2 ps) for a gate length of 100nm. Closer agreement with the Monte Carlo results is obtained when using energy relaxation time of 0.1 ps. Using this method we were able to determine the appropriate relaxation time. From Figure 4 it is very evident that choice of proper relaxation time is necessary as the drain current varies drastically for different relaxation times.

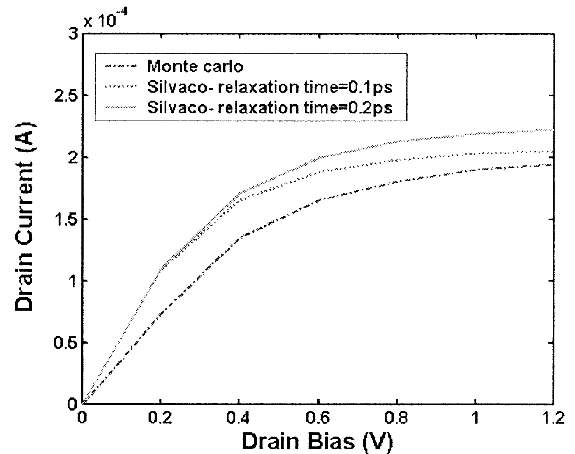
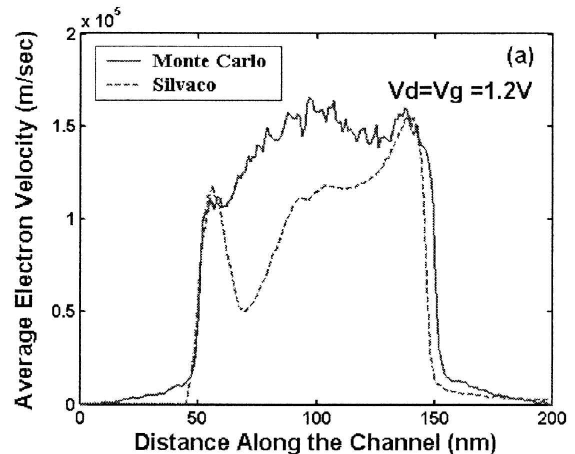


Figure 4: Output characteristics of 100nm gate length FIBMOS device for different values of the energy relaxation times. Also shown in this figure are the Monte Carlo simulation results.

Another noteworthy difference between the energy balance and the Monte Carlo simulation results is the observed velocity overshoot in 100nm as well as 50nm gate length FIBMOS device structure (Figure 5). The energy balance model tends to underestimate both the velocity overshoot effect and the average electron energy, This leads to the conclusion that the Monte Carlo method is a more reliable approach for predicting device performance. Also as discussed in the previous section, our 2D Monte Carlo as well 2D Silvaco ATLAS simulations show that due to low electric field, the average electron energy remains lower than that of conventional MOS device (not shown in figure), which significantly lowers the probability of impact ionization to occur near the drain end.



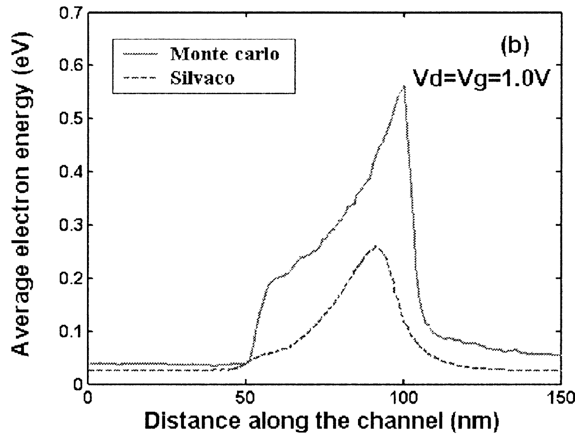


Figure 5: Comparison of carrier velocity and energy along the channel between Silvaco-Atlas and the Monte Carlo simulations.(a) for 100nm and (b) for 50nm gate lengths.

As a last effort we have also simulated the transfer characteristics of the FIBMOS device using Silvaco ATLAS simulator and compared it to that of a conventional MOS device. As we scaled down the gate length to 50nm we were able observe a marked difference in the values of the sub-threshold slopes between the FIBMOS device and the conventional one. It was observed that the values were 85.2 mV/dec in a FIBMOS device which is very less compared to that of a conventional one whose value was 109.8 mV/dec. This is due to the presence of the p^+ implant near the source end. This enables the device to toggle between OFF and ON states more easily compared to conventional MOS. Figure 6 shows the transfer characteristics of both devices.

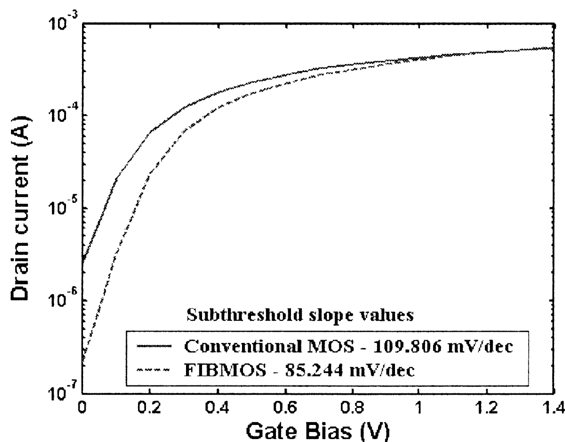


Figure 6: Transfer characteristics of FIBMOS and conventional MOS device for gate length of 50nm.

4 CONCLUSIONS

In conclusion, simulations presented in this paper suggest that Monte-Carlo simulations will be required to accurately predict the operation of nano-scale devices with uniform and asymmetric doping profiles. Also, the results shown in this paper suggest that using FIBMOS device structures has a number of advantages in modern nano-technology in comparison to conventional MOSFET devices.

REFERENCES

[1] C.-C. Shen, J. Murguia, N. Goldsman, M. Peckerar, J. Melngailis, and D.A. Antoniadis, "Use of focused-ion-beam and modeling to optimize submicron MOSFET characteristics," *IEEE Trans. Electron Devices*, vol.45, pp. 453–459, Feb. 1998.

[2] T. N. Buti, S. Ogura, N. Rovedo, and K. Tobimatsu, "A new assymetrical halo source GOLD drain (HS-GOLD) deep sub-half-micrometer n-MOSFET design for reliability and performance," *IEEE Trans. Electron Devices*, vol. 38, pp. 1757–1764, Aug. 1991.

[3] J. Ma, H.-B. Liang, R. A. Pryor, S. Cheng, M. H. Kaneshiro, C. S.Kyono,and K. Papworth, "Graded-channel MOSFET (GCMOSFET) for high performance, low voltage DSP applications," *IEEE Trans. VLSI Syst.*,vol. 5, pp. 352–359, Apr. 1997.

[4] I Knezevic, D. Vasileska and D. K. Ferry, IEEE Transactions on Electron Devices, Vol 49, No 6, Feb. 2002.

[5] C. Herring and E. Vogt, "Transport and deformation-potential theory for many-valley semiconductors with anisotropic scattering," *Phys. Rev.*,vol. 101, pp. 944–961, 1956.

[6] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Mod. Phys.*, vol. 55, pp. 645–705, 1983.

[7] D. K. Ferry, "First-order optical and intervalley scattering in semiconductors," *Phys. Rev. B*, vol. 14, pp. 1605–1609, 1976.

[8] W. J. Gross, D. Vasileska, and D. K. Ferry, "3-D Simulations of ultrasmall MOSFET's with real-space treatment of the electron–electron and electron–ion interactions," *VLSI Design*, vol. 10, pp. 437–452, 2000.

[9] R. W. Hockney and J. W. Eastwood, *Computer Simulation Using Particles*. Maidenhead, U.K.: McGraw-Hill, 1981.