

Partial-Element Equivalent-Circuit Model Simulation for Designing RF-Wireless Communication Products with Embedded Passive Components

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ABSTRACT

Rapidly increasing functionality and performance of RF/wireless communication products, along with mandated decreases in size, weight, and cost, have created a critical need to replace discrete, surface-mounted passive circuit components with embedded passives in substrate technologies such as Low-Temperature Cofired Ceramic (LTCC). The design process for embedded passives requires rapid electromagnetic simulation with full mutual coupling among all embedded structures, to allow each design-refining iteration to be carried out in a few minutes. Full-wave "2.5-D planar" solvers perform the right type of simulation, but typically require run times of hours to days and sometimes cannot accommodate the required circuit/layout complexity. In order to achieve results of comparable accuracy in the RF/wireless frequency range, with simulation times of a few minutes, we have used the well-known Partial-Element Equivalent-Circuit (PEEC) modeling technique to develop a simulator that is used in the same way as existing multi-layer planar solvers.

Keywords: RF/wireless communication, device and circuit simulation, boundary-element method, CAD, LTCC

RF-WIRELESS DESIGN TOOL PROBLEM

The next two generations of personal wireless terminals will evolve from basic cellular telephones and pagers to terminals offering full internet access, with a concomitant explosion in the amount of data processed. In order to accomplish this in terminals having adequately small size, weight, and power consumption, it will be necessary to replace many discrete, passive components (now mounted on the surface of interconnection substrates) with embedded passives integrated into the wiring of the substrate. As surface-mounted passive components that have no significant electromagnetic coupling give way to closely-packed, buried passives, the design process must model mutual coupling (intentional or unwanted) among all components.

Figure 1 shows schematically a portion of an LTCC substrate having buried inductors, capacitors, and ground planes, and also a few remaining discrete, surface-mounted components. LTCC allows an especially high level of integration because it affords up to fifty wiring layers and the possibility of as many as a few hundred buried passive components in a single substrate.

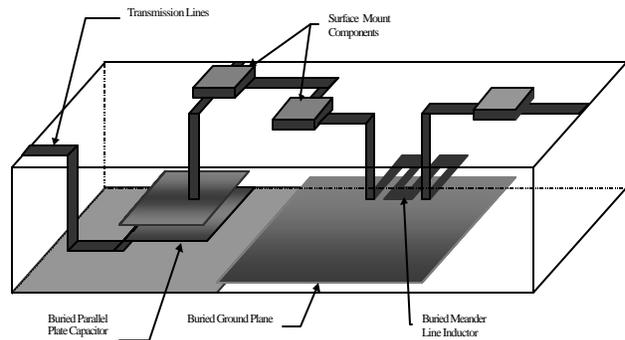


Figure 1 - Schematic view of an LTCC substrate with interacting Embedded passive components

A critical deficiency of existing RF modeling and simulation tools for designing today's RF-wireless products is their inability to model full mutual coupling within embedded-passive circuits having realistic size and complexity. Current ceramic and PWB technologies can support up to one or two hundred embedded passive components on up to fifty wiring layers. For significant value in the real-time design iterations of these systems, a simulator must calculate performance at tens to hundreds of frequency-points in times of seconds to a few minutes. Multi-layer planar solvers perform the right type of analysis on the right types of structures, but they run for a few hours to over a weekend for a single functional block (e.g. band-pass filter) having a few embedded passive components.

PARTIAL-ELEMENT EQUIVALENT-CIRCUIT (PEEC) MODEL

In order to overcome this problem, we have used of the well-known Partial-Element Equivalent-Circuit (PEEC) modeling technique to develop a simulator that is used in the same way as full-wave multi-layer planar solvers. The PEEC approach substitutes an equivalent-circuit model with mutual inductances and capacitances (found by magnetostatic/electrostatic calculation) for a large matrix solution of Maxwell's electromagnetic equations on a fine mesh. By modeling the skin effect with frequency-dependent resistors, the PEEC method avoids a full-wave solution at every frequency, substituting an ordinary nodal circuit analysis. This turns out to be a judicious tradeoff giving great speed enhancement at little sacrifice of accuracy in the important RF wireless frequency range 1 to 3 GHz, and will be tested to at least 5 GHz.

In the PEEC technique, the entire circuit is partitioned into conductor-segments having dimensions that are a fairly small fraction (e.g. 10%) of a wavelength at the highest operating frequency. Figure 2 shows schematically a few elements of the partial-element equivalent-circuit (PEEC) model for a system of embedded components, the portion shown corresponding to only a few segments of all the embedded conductors. Conductor segments may be grouped into named "components": a rectangular spiral inductor having one segment for each "side" is a typical example of a

Figure 2 – PEEC Model for Embedded Conductors: only a few plates of a larger circuit are shown.

"component", within which the end-to-end connections of self-inductances (at circuit "nodes") correspond to the electrical continuity of the complete spiral. A break in the end-to-end connectivity of self-inductances corresponds to separate "components". Although Figure 2 shows of a simple sequential connectivity of self-inductances (at most two self-L's attached to any node), there is in fact no such restriction in the general PEEC model or simulator.

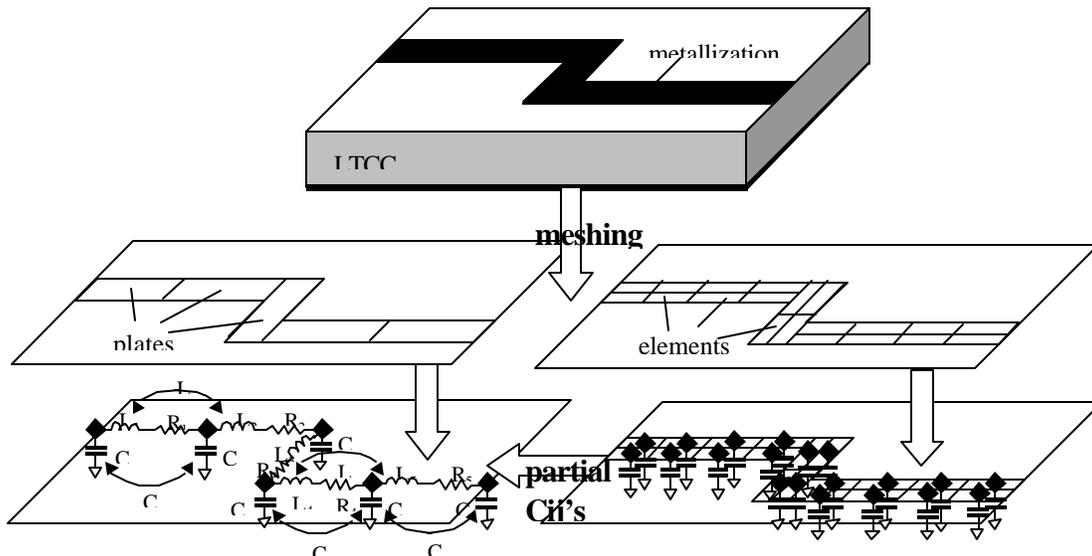
Inductance and Capacitance Calculations

Full matrices of mutual inductances and capacitances among the segments represent electromagnetic coupling among segments, both within each component and also among the segments of separate components. Electrostatic values of the self- and mutual inductances and capacitances are found, in our particular simulator by the boundary-element method (BEM) using Galerkin's method to allow relatively coarse conductor segments.

Formally, the mutual inductance between two plates carrying currents along paths L and L' is given by Neumann's integral formula,

$$M_{IJ} = \frac{\mu_0}{4\pi} \int_{L_I} d\mathbf{L} \cdot \int_{L_J} d\mathbf{L}' G(\mathbf{r}, \mathbf{r}') \quad (1)$$

where the Green's function $G(\mathbf{r}, \mathbf{r}')$ embodies the ground plane configuration. For parallel or orthogonal rectangular



plates, closed-form expressions for M_{ij} are given in [1]. Integration by numerical quadrature is used for curvilinear plates. Self-inductance is a special case.

The method of partial capacitance [2] is used to find the circuit capacitances from potential coefficients p_{ij} [3] for *elements* shown in Figure 2. Formally,

$$p_{ij} = \frac{1}{S_i S_j} \iint_{S_i} dS \iint_{S_j} dS' G(\mathbf{r}, \mathbf{r}') \quad (2)$$

where $G(\mathbf{r}, \mathbf{r}')$ embodies the dielectric layer configuration by using the method of complex images [4]. Closed-form expressions for parallel and orthogonal rectangular plates are given in [3], and numerical quadrature is used for curvilinear plates. The circuit capacitances are then found as follows. The capacitance matrix for the *elements* is found by solving the following system for the charges q_j (each plate I is in turn set to one volt with all others at zero volts):

$$\sum_{\text{elements } j} p_{ij} q_j = V_i$$

$$\text{with } V_i = \begin{cases} 1 & \text{element } i \text{ is on plate } I \\ 0 & \text{element } i \text{ is not on plate } I \end{cases}$$

The plate capacitances follow from:

$$CP_{II} = \sum_{\text{elements } j \text{ on plate } I} q_j \quad \text{plate } I \text{ being set to 1 volt}$$

This is a standard electrostatic “partial capacitance” calculation, after which the CP_{II} of the “plates” are remapped to the C_{KL} of the “nodes: by allocating half of the capacitance of each plate to each of the two nodes on its ends; each mutual CP_{IJ} gets mapped to four G_{KL} ’s. The system of equations is solved using iterative methods like “greatest common residual” or “conjugate gradient”.

Skin Effect

We have developed an approximate empirical model for the skin effect, based on references [5-7]. Using this model, the ac-resistance of each segment is made strongly frequency dependent, and each self-inductance is made weakly frequency-dependent, within our simulator's ac-analysis routine. Coefficients of empirical curve-fits of frequency-dependent resistance and internal self-inductance are determined for each conductor segment,

reflecting the effect of conductor width, thickness, and proximity to ground plane(s). This model allows the calculation of scattering parameters at many frequency points by an ordinary nodal circuit analysis, requiring only a single extraction of the self- R 's, and self- and mutual L 's and C 's before beginning the ac-analysis.

Modal dispersion

Generally, stratified dielectric media having materials with different dielectric constants (including ordinary microstrip) are dispersive, i.e., the electromagnetic propagation velocity is frequency-dependent. LTCC having ground planes on both the top and bottom surfaces (“strip line”) is nondispersive, and even when the top or bottom surface (or both) is an unmetallized air-interface, dispersion can be neglected if the bandwidth of device operation is small enough that the variation in the ratio (LTCC-thickness/wavelength) is much less than unity. Since this is the case in the RF/wireless designs we have studied up to 3 GHz, we have not explicitly included modal dispersion in the PEEC model. For more general stratified dielectric substrates, or wider bandwidth device operation, the PEEC model can be enhanced with a frequency-dependent capacitance model, implemented in a fashion similar to that of the ac skin resistance; see, for example, [8] for the simple microstrip line case.

Retardation

Another phenomenon that we have not yet included in our PEEC simulator but that has been studied by other investigators is “retardation”. This effect refers to the fact that there is a delayed response in the electric potential at a point “B” to a charge or current at a different point “A”. Retardation becomes significant when the dimensions of the structure are large enough and the operating frequency is high enough that some “A-B” point-pairs encounter delays comparable to one period (inverse frequency). Such situations are within the realm of allowable LTCC but we have not thus far designed circuits where retardation is significant.

PEEC SIMULATOR USAGE

Figure 3 is a schematic block diagram showing the main functions of our PEEC simulator. It contains routines for generating the geometry of embedded components; at the present time these routines prompt the user for numerical parameters describing these structures and do not use a graphical user-interface (GUI). Additional routines use the Galerkin version of the boundary-element method [eqs. (1),

(2)] to extract the L's, R's, and C's of the PEEC model. After the user provides additional input describing connectivity of the embedded components and/or addition of optional ideal, discrete L's, R's, and C's, an ac-analysis routine calculates scattering parameters S_{ij} relative to user-defined electric ports. This is an ordinary nodal analysis, and allows segment resistances and self-inductances as a representation of the skin-effect. Output data is available as printed reports, scattering-parameter graphs (decibel plots, Smith charts, or polar charts), and also as files importible into a commercial CAD system. Layout information is also available as a file importible into a CAD system. It is planned to implement *import* of layout information from a CAD system for simulation, but this is not presently supported.

The usage of our PEEC simulator is very similar to that of commercial, "2.5-D" multi-layer planar solvers, in that it models an arbitrary multi-layer configuration of thin conductors, with zero, one, or two ideal ground planes. It supports simulation of LTCC circuits whose fundamental

circuit elements. For example, a spiral inductor structure can be given a name such as "L1", and even though the simulator makes a good approximation to fully distributed behavior of the spiral, it also reports a total "DC" inductance of this spiral as well as of every other named "component", and further reports a matrix of mutual inductances among all such components. Similarly, a "DC" capacitance matrix is reported. This enables a check on the degree to which the actual structures approximate the original lumped circuit model, and specifically reports "parasitic" mutual inductive and capacitive coupling. Subsequently, the ac_analysis of the layout (which uses the more finely-segmented internal PEEC model) reveals the extent to which the true distributed behavior deviates from the conceptual lumped-element model.

The PEEC model automatically associates a physical point or line in the layout with each electrical node of the circuit. This will be directly useful for performing layout-versus-schematic checking when our PEEC simulator

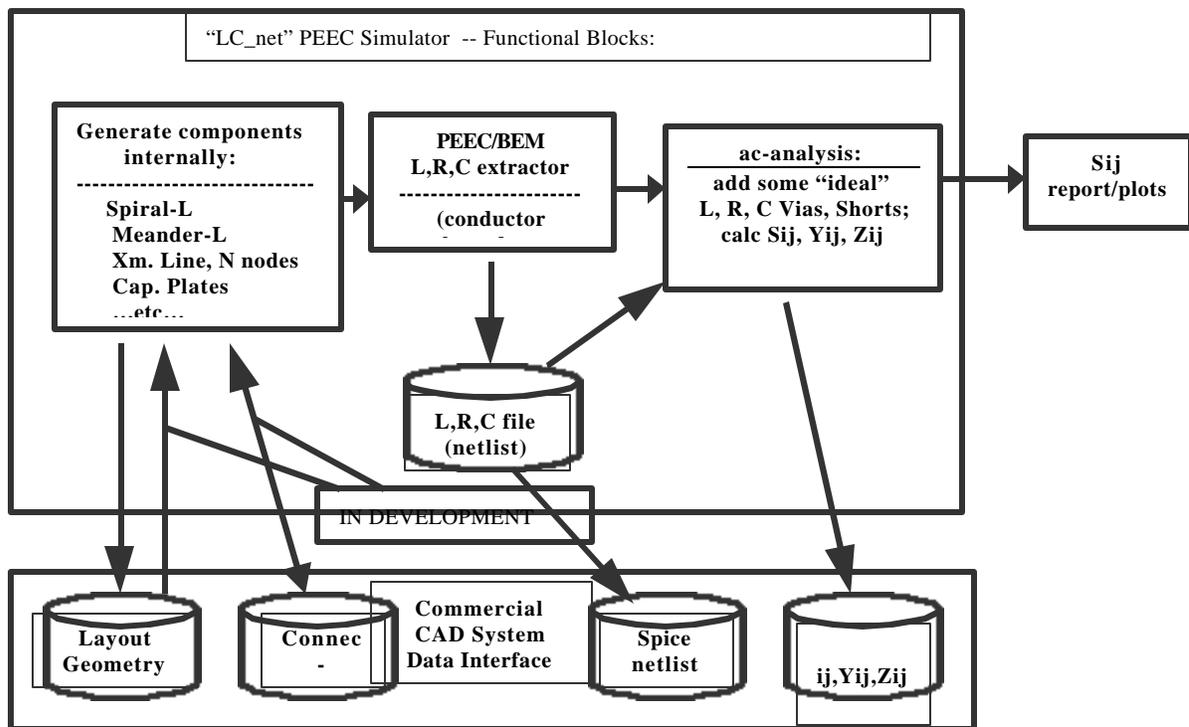


Figure 3 – Block Diagram of PEEC Simulator “LC_net”

design concept is lumped, distributed, or a combination. The simulator's method of naming structures is especially well-suited to implementing circuits that begin conceptually as a lumped-model, such as an LC-filter, including the use of intentional mutual inductance, since the simulator reports calculated values for the lumped

becomes an integrated tool within a commercial CAD system.

DESIGN EXAMPLES: LTCC BANDPASS FILTERS

We illustrate usage of the PEEC simulator with some bandpass filter examples originating as lumped-element LC-filters, but requiring iterative simulation and design refinement to compensate for distributed-circuit and parasitic-coupling effects. Although we compare PEEC simulation times against those of a 2.5-D planar solver for four different filters, we will for brevity describe and present simulation results for only one of these filters.

The filter structure shown in Figure 4 is for a wireless paging application and exploits the multilayer capability of

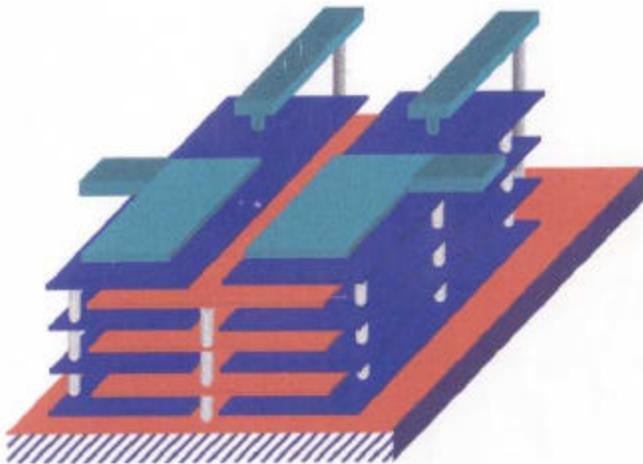


Figure 4 - Perspective view of embedded conductors of multilayer LTCC bandpass filter for a paging application

LTCC to minimize area, implementing two large capacitors as multiple-layer, parallel-plate "sandwiches". The plates in the center (orange in the color rendering), are attached to the bottom ground plane with vias (vertical rods) intended as zero-impedance connections, but which in reality have a small inductive reactance. The approximate equivalent circuit model shown in Figure 5 shows this impedance as an inductance "Lgv" which actually turns out to be an important source of coupling between the L-C resonators on the input and output sides of this filter. The 1-nanohenry inductance of each shunt resonator resides in two inductor strips on the top wiring level, as well as in the capacitor plates and in the vias connecting the inductor strips to the capacitor plates.

Figure 6 shows the insertion loss $S_{21}(f)$ of this filter as obtained by simulation and measurement. The black or solid curve shows the measured insertion loss. Three distinct simulation results are presented; in the color rendering, these are shown as red, green, and violet curves, corresponding respectively to the highest, middle, and

lowest trap frequencies in the black-and-white rendering. The red (0.66-GHz trap) curve represents the nominal structure dimensions, including the vias (vertical "rod" interconnections, which are modeled as 5-mil-diameter, solid-silver wires with a frequency-dependent impedance

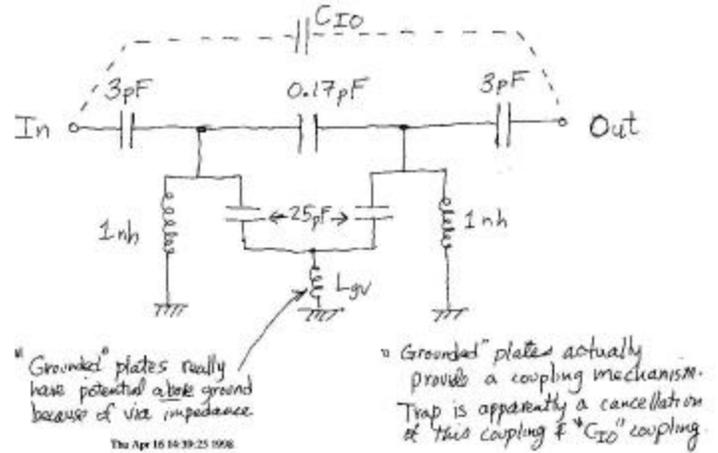


Figure 5 - Approximate lumped equivalent circuit model for interpreting multilayer filter performance

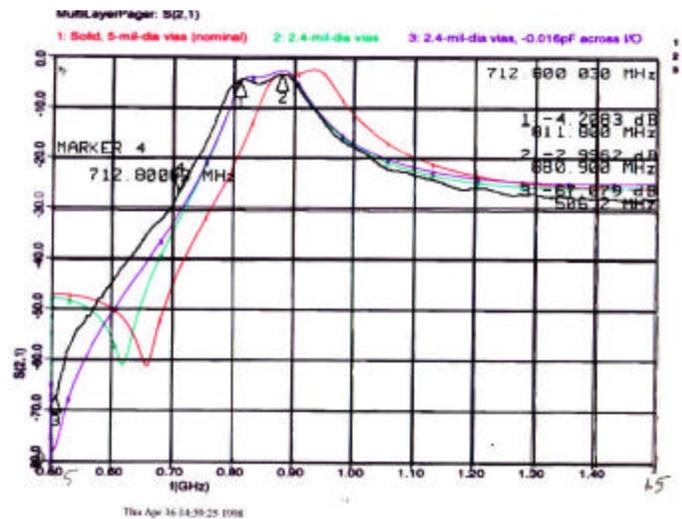


Figure 6 - Measured and simulated insertion loss of the multilayer LTCC bandpass filter

modulated by the skin effect. The only different assumption for the green (0.61-GHz trap) curve is that the via's impedance is higher in an amount that corresponds to reducing their diameter to 2.4 mils; this change in a structure whose impedance is a relatively small part of the overall resonator, is sufficient to shift the passband frequency by about 50 MHz, making it agree very well with measurement. The violet (0.5-GHz-trap) curve was

obtained by using the capability of the simulator to perform rapid "what-if" experiments, by artificially adding "ideal" or "external, discrete" components (capacitors, inductors, resistors, etc.) to the PEEC that represents the physical, embedded conductors. In this case, a hypothetical negative capacitor (-16 fF) was connected directly across the input and output terminals, in the position marked "CIO" in Figure 5. The resultant shift in the trap frequency (now agreeing well with experiment) strongly suggests that the trap is due to destructive interference between signals coupled through elements Lgv and CIO, and it is straightforward to show the existence and frequency of such a trap from the approximate circuit model of Figure 5. Thus, although the simulation was not sufficiently accurate for a one-pass design, it gives much insight into the filter operation and is probably good enough for a two-pass design. This is extremely valuable for the LTCC design process.

PEEC SPEED ADVANTAGE : QUANTITATIVE RESULTS

Figure 7 compares the simulation times for our PEEC simulator "LC_net" against those for a commercial 2.5-D full-wave simulator, for the two filters described above and for two additional filters. In all four cases, the simulators gave results of comparable accuracy (agreement with experimental measurement). In three of these cases, two different meshes (ordinary mesh and edge mesh) were used in the full-wave simulator. The edge-mesh more accurately models the transverse current distribution, and accordingly takes longer.

The "bottom line" of the benchmarks used here is the time required to obtain a filter response with 200 frequency points, even though fewer, judiciously-placed samples could have accurately described the filter performance. All times are for a 151-MHz Sparc station model 20. Comparing the PEEC simulator to the 2.5-D full-wave simulator, the speedup factor ranges from just over two orders of magnitude to about 3.5 orders of

Figure 7 – Comparison of PEEC and full-wave run times magnitude, depending on the complexity (number of layers, conductors, and electrical nodes used in the PEEC model). This is not surprising, considering the relatively coarse conductor "meshing" used by the PEEC model.

All filter structures considered here are made of "Manhattan-oriented" rectangles, for which the PEEC simulator exploits closed-form expressions for mutual inductance and mutual potential coefficients. It is somewhat slower with structures having arbitrary shape, but only in extracting the circuit; the frequency-sweep speed is unaffected. In the circuit extraction, it still gains a speed advantage by using numerical quadrature on coarse polygonal or curvilinear segments.

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