Challenges in Process Modeling for MEMS

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ABSTRACT

The potency of the silicon IC technology base, its use of CAD for design targeted for manufacturing and the related challenges faced in deployment of MEMS are discussed. The rapidly growing field of MEMS has created opportunities to merge new functional capabilities with integrated circuit (IC) electronics. MEMS fabrication uniquely requires accurate prediction of both geometry and materials dependencies that affect electrical, mechanical and other structurally constrained behavior.

Keywords: *Geometry modeling, Process simulation*

INTRODUCTION

The ubiquitous use of IC technology in virtually every aspect of modern society is a remarkable fact that supports and shapes an information revolution that is now unfolding. Particularly, the areas of communications, computation and industrial/commercial electronics each drive major market segments. At the same time, just as with Amdahl's Law which reveals the limits of computer performance, there are other basic (Newtonian) laws that reflect other systems challenges. Amdahl's Law states that the slowest path will limit logic speed (or memory access) which can in turn control computer performance. From a mechanical systems perspective, the size and mass will pose basic limits on the range of application. Hence, there are basic limitations for both ICs and MEMS; each is directly linked to fabrication processes and control of manufacturing tolerances. In the case of VLSI, the interconnect delays and associated materials properties in back-end processing now dominate; while for MEMS the material issues are an even greater challenge along with process integration and control of tolerances.

After briefly reviewing the present status of IC scaling, the underlying technology base and the capabilities of existing TCAD tools to support design and manufacturing, specific examples of new challenges for future IC developments will be presented. Much of the IC fabrication and TCAD infrastructure provide bootstrapping for MEMS. Specifically, computational prototyping (especially from a geometry perspective) of advanced VLSI technology has evolved rapidly, driven by aggressive targets for higher performance and reliability. This progress in TCAD synergistically supports challenges that face the MEMS field. The remainder of the paper presents results in support of process modeling for MEMS: geometric modeling, visualization, and physical models for deposition and etching.

VLSI TCAD PERSPECTIVE

There are two facets of VLSI that directly map into the domain of MEMS. First, the limitations of functional density that can be achieved within the silicon wafer have pushed technologists to: a) use trench etching of silicon for both isolation and in creating functional devices (i.e. DRAMS) and b) create more exotic structures on top of the wafers involving a range of conventional (i.e. poly silicon, aluminum...) as well as non-traditional (low- and high-dielectric constant...) materials. Second, many of the performance issues facing future ICs--achieving higher speed and dealing with greater amounts of heat dissipation--have mandated more careful considerations of packaging.

From a VLSI TCAD perspective, there has been an important shift in attention towards: a) back-end processing (deposition etching), b) new multi-layer (and polycrystalline) materials systems and c) electro-thermal and electro-mechanical (stress) analysis. While each of these areas are only a subset of needs for fabrication and simulation-based design for MEMS, there are two major leveraging factors. First, the growing tool infrastructure to create complex 3D geometric models, including simulation of realistic process dependent effects, is both powerful and economically leveraged. Second, many application drivers such as communications (mixed-signal systems with analog/digital) push the design tools and technology base towards greater heterogeneity that in turn supports MEMS needs as well. The next section will show direct impact on MEMS from 3D modeling perspective that also supports VLSI interconnect applications.

GEOMETRY MODELING for MEMS

As discussed above, the critical dependence of MEMS on geometry and associated process-dependent materials parameters (including surface roughness and grain structure), put a premium on predictive geometry as well as detailed parameterization of geometry. Two example are now presented show-

ing new 3D geometry modeling capabilities for MEMS. The structure used is an RF switch that gives a variable capacitance based on electrostatic deflection of upper electrode beams. The geometry supports, surface and other boundary conditions [1] have a major impact on performance. Moreover, physical parameters of the electrode layer (i.e. Young's modules) strongly affect capacitance with pull-in voltage [2]. The focus here is on modeling of geometry as well as surface morphology as discussed in the next section.

The combined use of basic solid geometry modeling and simulation-based surface shaping, in this case using deposition simulation with SPEEDIE [3], provides a powerful combination that can markedly enhance accuracy of performance simulation. A new pseudo 3D physical process simulation approach has recently been demonstrated which is fully integrated with traditional geometric capabilities [4]. The technique is used to create 3D physical geometry that combines: initial geometry (ideal), cut planes created using 2D physical simulation and nonuniform rational b-spline (NURBS) data smoothing and integration, including use of Boolean operations.

The resulting profile is incorporated into the solid model, and can be manipulated in subsequent steps by geometric operations and additional physical depositions. The RF switch (Figure 1) was created using this technique. The entire device was created by the user defining only the mask specification (.CIF file) and a simple process flow. One physical deposition step was performed in conjunction with multiple geometric etches to achieve the final shape. Notice the rounded corners on the top of the switch due to the physical process simulation, while the sharp edges are the result of an ideal (geometric) etching step. The solution of coupled elastostatic-electrostatic equations shows that Von Mises stress for the electrostatically actuated RF switch concentrates at the inner corners due to the sharp edges. A similar result would have been seen at the top edges if geometric deposition had been performed. Physically based simulation, however, indicates rounded corners will appear and thus no stress concentration will be observed at the top corners, in agreement with experimental results.

The second example considers the formation of the switch from the perspective of etching and this time a complete 3D simulator is used to remove the sacrificial layer, creating the membrane and well shown in Figure 2. This model was created using a combination of 3D constructive computational geometry modeling [5] and surface extraction for both visualization and to generate a meshed surface representation. The level set algorithm allows a range of advanced physical models for deposition and etching to be incorporated into the simulations. The level set algorithms are implemented on an octtree grid as shown in Figure 3. The refinement (and de-refinement) features of tree-based gridding allows for local capture of process dependences, even down to atomic-scale features if needed [6]. Hence, numerical methods such as FEM and boundary movement algorithms can be formulated on the same static grid.

For FEM analysis, volume meshing of the final geometry is needed. The use of routines such as marching cubes for extraction of iso-surfaces provides a two-fold benefit: 1) it is useful as part of the visualization process and 2) it provides a means to capture and triangulate a mesh on the surfaces. Figure 4 shows both these capabilities in reference to modeling the RF switch.

PHYSICAL PROCESS MODELS

Modeling of IC technology has a long history in the area of VLSI bulk processing. For example, the SUPREM program provides capabilities to model 2D effects critical for device scaling. In the case of deposition and etching, especially for VLSI interconnect modeling, tools such as SPEEDIE [3] have demonstrated great potential in capturing the complexity of surface chemistry and associated effects from ion bombardment. For example, etching (chemical and sputtering) and deposition (inhibitor formation) occur simultaneously. Figure 4 shows a SPEEDIE simulation of etching silicon dioxide in high density plasma. The structure shown known as the "champagne glass" device, has large overhang regions to separate the physics bombardment, species sticking coefficients and surface chemistry of various process conditions. From the perspective of MEMS device fabrication, it is also interesting to note that such structures with such large lateral aspect ratios are not uncommon.

The level set method is a parametric boundary movement method by using the signed distance to the boundary as the tracking parameters, and has shown significant improvement on stability, accuracy and robustness in comparison with the geometrical methods [5]. Since the surface normal and curvature can be evaluated precisely, physical smooth surface evolution with high accuracy can be achieved. This is important for modeling the increasingly complex fabrication technology, such as high density plasma etching and deposition in deep submicron processes. Accuracy in the physical models and level-set boundary movement has been validated in various fabrication processes in 2D and 3D. Features captured by simulation for PECVD and PVD are now illustrated.

A typical PECVD process is modeled with dual profile controlling mechanisms: one for LPCVD induced by a neutral precursor and one for ion induced deposition activated by ion bombardment. The LPCVD component is assumed to be sufficiently randomized in the gas phase and to have isotropic angular distribution. The angular distribution of the ion-induced component is calculated by Monte Carlo simulation of the plasma sheath. Figure 5 shows the SEM and SPEEDIE simulation of PECVD film deposited in a rectangular gap with

aspect ratio 1.25 with aluminum lines on both sides. The sticking coefficient of the neutral precursor is 0.07, and the ratio of the LPCVD component to the ion induced deposition component at the top surface is 2. Since direct ion bombardment is the dominant factor affecting deposition topography, the ion induced deposition is a sensitive function of local visibility. Any jaggedness in the simulated surface profile may shadow unphysically incident ions, and this error may accumulate and amplify over simulation to lead to numerical instability. Generation of smooth profile evolution is essential to model topography evolution in the plasma assisted environment. The level-set method can be easily controlled to generate smooth surface profiles, without compromising its ability to capture and preserve the sharp corners at the bottom of the trench.

Figure 6 shows the SEM and SPEEDIE simulation of the deposited aluminum thin film in an argon discharge in a rectangular trench with aspect ratio 2. Since the motion of the sputtered atoms from the target is assumed to be sufficiently randomized through collisions in the gas phase with a cutoff angle close to, its angular distribution is assumed isotropic. A sticking coefficient of 1 is used for these sputtered atoms. The ion acceleration through the plasma sheath is practically collisionless, and the ion impact-angle distribution is assumed unidirectional. The ratio of the neutral component to the ion component at the top flat surface is 7:3. Despite that smooth profile evolution for etching and deposition simulation in plasma assisted environments is necessary to avoid numerical instability, the ability to capture sharp corners is nonetheless equally important. Owing to the fairly anisotropic distribution of the incident ion flux, we can expect the growth of the hump on the bottom of the trench along with its two surrounding sharp corners.

CONCLUSION

This paper presents a broad yet strategic view of process modeling of IC fabrication process and especially the potential synergism between TCAD for VLSI technology and the growing opportunities for process modeling of MEMS. Emphasis is given to 3D geometry modeling (and visualization) of MEMS structures which is of critical importance due to the dependence of performance on layer shapes and thicknesses. In addition, examples of the state-of-the-art for physical modeling for deposition (and etching) is presented. Based on such simulations it is possible to create quantitative geometry models for complex structures. The long-term goal is to realize accurate geometry and physical models in support of simulation-based design of MEMS.

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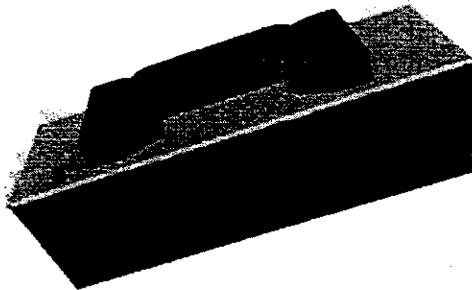

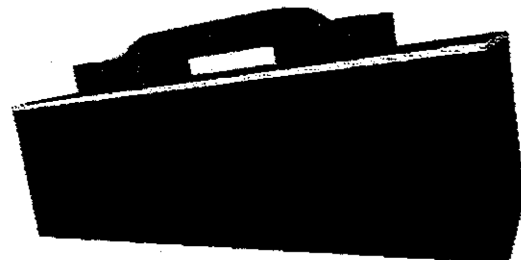

Figure 1: 3D computational prototype of a MEMS-based RF switch. Two views of the device show realistic surface structure resulting from a physical deposition model based on multiple SPEEDIE (2D) simulations and constructive 3D (and quasi-3D) geometry modeling, combined using NURBS.

Figure 2: 3D computational prototype of an RF switch. An externally applied voltage deflects the top plate, as shown in the figure, and in turn modulates the capacitance across the air gap.

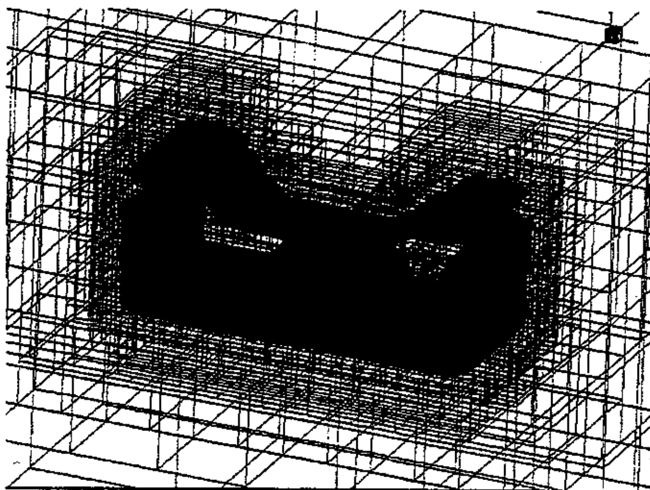

Figure 3: The oct-tree based level-set grid, from which the geometry in Fig. 2 is generated. The geometry is embedded in the grid. Each grid point holds a distance to the boundary of the geometry. Boundary movement can be performed on this grid using the level-set method.

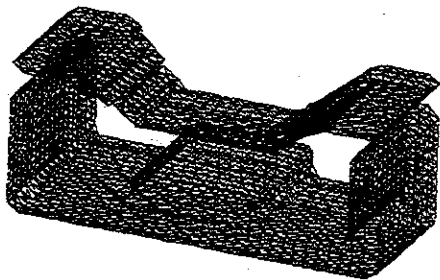

Figure 4: The triangular mesh generated from the level-set grid (fig. 2). The marching cube algorithm is used to extract the iso-distance surface. This mesh can be used for visualization and FEM simulation.

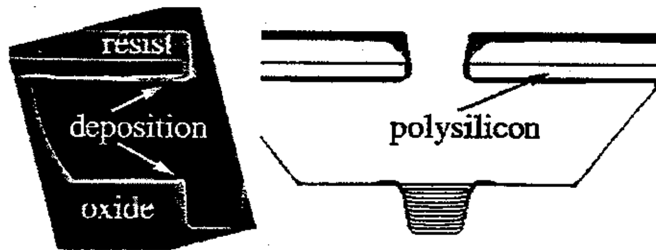

Figure 4: A SPEEDIE [3] simulation of etching silicon dioxide in high density plasma. Thin layers of inhibitor deposits on parts of the surface during etching. The physical model accounts for inter-structure radicals transport, ion sputtering, ion-assisted etching, and ion enhanced inhibitor deposition.

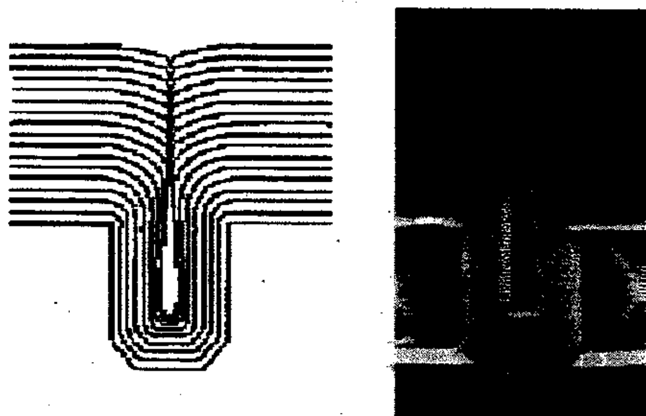

Figure 5: PECVD of SiO2 from TEOS in a trench [5].
(a) The simulated profile evolution. (b) The SEM. Process conditions: 375°C, 2.1 Torr, Sc = 0.07, incoming ion impact-angle distribution: $\cos^{10}(\theta)$, ration of neutral-to-ion component = 2, TEOS flow rate = 1.8 sccm, O^2 flow rate = 6.5 slm.

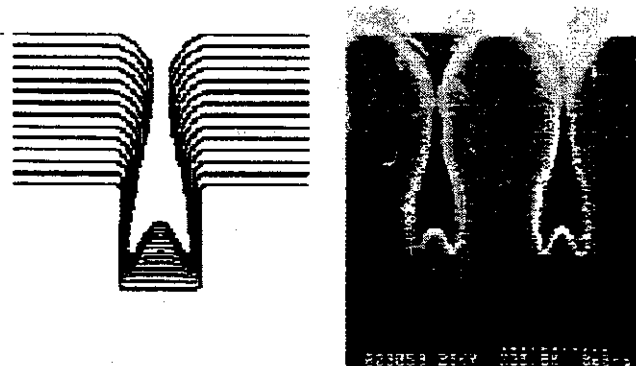

Figure 6: Ionized magnetron physical vapor deposition (PVD) of aluminum in a trench [5]. (a) The simulated profile evolution. Simulation conditions: temperature below 100°C, 35 mTorr, Sc = 1.0, unidirectional ion distribution, neutral-to-ion flux ratio = 7:3, sputter yield = 0.0. (b) The SEM.