Physics-based and compact models for self-heating in high-speed bipolar integrated circuits

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ABSTRACT

We present three-dimensional heat-transport simulation for bipolar transistors. The simulations are validated on experimental data, and are employed to develop analytical models for the thermal resistance of devices fabricated on bulk and SOI substrate, and with deep-trench isolation. The cross-heating effect in multifinger devices is also modeled.

Keywords: Bipolar transistors; compact models; device simulation; thermal resistance; self-heating

1 INTRODUCTION

Bipolar transistors are extremely sensitive to temperature variations. Moreover, the adoption of advanced isolation techniques such as silicon-on-insulator (SOI) and deep-trench isolation (DTI) to increase device speed also dramatically increases self-heating, due to the poor thermal conductivity of silicon dioxide. In many cases, an estimate of self-heating is needed before fabrication. However, analytical models for the thermal resistance of bipolar transistors exist only for a limited range of device geometries [1]–[3]. In this work we present numerical simulations and compact models of thermal resistance for bipolar transistors in a variety of geometries, including shallow- and deep-trench isolation, and bulk and SOI substrates. The numerical simulation is validated on experimental data, and is used as a guide in developing new analytical compact models, which can then be used for both manual calculations and computer-aided design. No fitting parameters are necessary, and the total thermal resistance is obtained as a series or parallel composition of terms, each corresponding to a geometric feature.

2 PHYSICS-BASED MODELING

Three-dimensional (3D) numerical simulations of heat transport were performed using the simulator DESSIS from ISE AG [4]. The adoption of a 3D model is essential for heat-transport simulations, to avoid results which are inaccurate at best, or even unphysical, as pointed out in Ref. [5]. A full 3D device structure was defined for the SiGe bipolar technology described in Ref. [6]. A uniform heat generation was assumed in the base-collector depletion region.

In all the simulations we only considered linear heat transport. A unique thermal resistance can be defined only in the limit of a temperature increase linearly proportional to dissipated power. The nonlinearity due to decrease of thermal conductivity with temperature can be simply accounted for by analytical transformations, as a simple correction factor to the linear result [7]. Current crowding was also neglected, since it will not affect the thermal resistance strongly, especially for devices on SOI and with deep-trench isolation, where the largest part of the temperature drop occurs outside the active areas. Finally, size effects due to phonon-boundary scattering [8] were not included, due to the relatively large size of the structures. For smaller devices, size effects can be accounted by employing a reduced effective thermal conductivity.

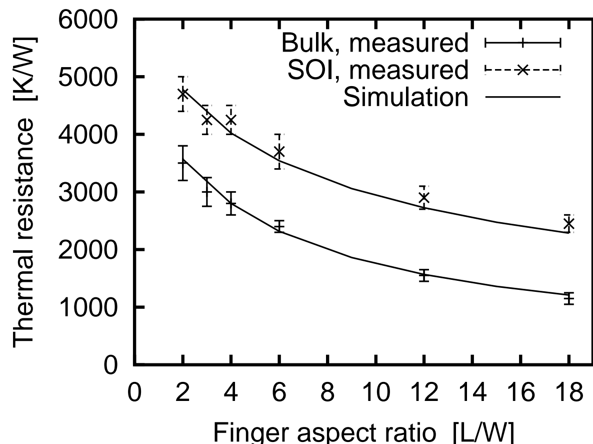

Figure 1: Comparison between measurement (symbols) and simulations (lines) for the thermal resistance of single-finger bipolar transistors, with varying finger length, and finger width of $0.28\,\mu m$. An additional heat loss through the metallization is modeled by a fixed thermal resistance of 8×10^4 K/W. Results are shown for devices fabricated on bulk substrate and on SOI (silicon thickness $1.1\,\mu m$, buried oxide $0.4\,\mu m$.)

Figures 1 and 2 show the comparison between experimental data and numerical simulation for single-finger and multifinger devices, respectively. Measurements were performed as reported in Ref. [9] in devices on both bulk and SOI substrates. In the case of single-finger transistors, the heat loss through the metallization was accounted for, according to the results of Ref. [8].

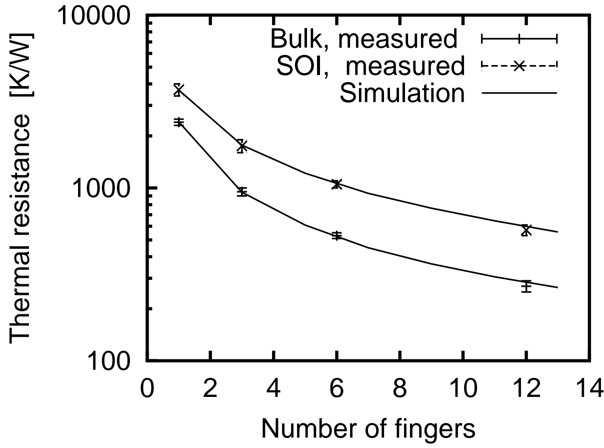

Figure 2: Thermal resistance for multifinger devices, plotted as a function of the number of fingers. Experimental values (symbols with error bars) are compared to simulations (lines). For all devices, the finger aspect ratio is $L/W = 6$. The finger pitch is $3.56\ \mu m$.

Figures 3, 4, and 5 show the three-dimensional temperature distribution in bulk, SOI, and trench-isolated transistors. It is apparent how the physics of heat removal is different in the three cases. In bulk, heat transport occurs radially. In SOI, heat diffuses laterally over a 'healing length' m given by [8]

$$m = \sqrt{t_c t_i \kappa_c / \kappa_i}, \tag{1}$$

where t_c and κ_c are the conductor's thickness and thermal conductivity, and t_i and κ_i are those for the insulator. After heat has spread to a sufficiently large area, it can travel vertically through the buried oxide. Finally, in a deep-trench-isolated device, heat travels radially to the walls of the trench, then straight down, and finally it resumes the radial diffusion from the bottom opening of the trench. For a very deep trench, heat propagation through the trench walls will also be significant [10].

3 COMPACT MODELING

Using the insights obtained from the three-dimensional simulation results, a full set of analytical models were developed for the cases of transistors on bulk substrate, including shallow-trench isolation; on SOI substrate; on bulk, with deep-trench isolation; and multi-finger devices, for all the above cases. All the results were validated on an extensive set of simulations. Note that such a compact modeling approach is only possible using accurate 3D simulation, and would be prohibitive if only experimental data were employed.

The model for single-finger bulk devices is based on the formula of Joy and Schlig [1], corrected for the finite depth D

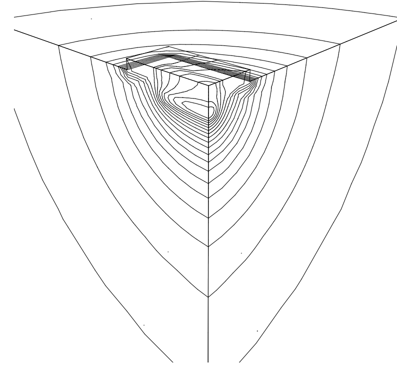

Figure 3: Three-dimensional temperature distribution for a single-finger bipolar transistor fabricated on bulk substrate. Only one-quarter of the device is shown. The vertical planes are the planes of symmetry of the finger. The finger size is $0.28 \times 1.68 \mu m$.

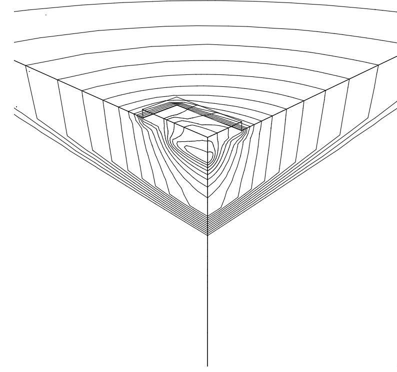

Figure 4: Three-dimensional temperature distribution for a single-finger bipolar transistor fabricated on SOI substrate. The silicon thickness is $1.1 \mu m$, the buried oxide thickness is $0.4 \mu m$.

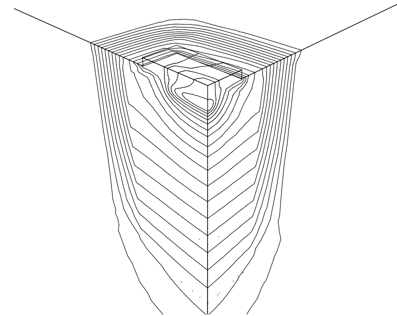

Figure 5: Three-dimensional temperature distribution for a single-finger bipolar transistor fabricated on bulk substrate with deep-trench isolation. The trench depth is $4 \mu m$.

of the heat-generating region:

$$R_{\mathrm{th,bulk}} = \frac{1}{4\kappa_{\mathrm{Si}}\sqrt{LW + (\pi D/2)^2}}, \tag{2}$$

where L and W are the finger length and width, and κ_{Si} is the silicon thermal conductivity. Shallow- and deep-trench isolation is modeled by a series thermal resistance, depending on the depth d_{tr} of the trench and its distance d_{tr} from the active area:

$$R_{\mathrm{th,well}} = \frac{t_{\mathrm{tr}}}{\kappa_{\mathrm{Si}} A_{\mathrm{tr}}} \times \frac{2}{\pi} \arctan(t_{\mathrm{tr}}/d_{\mathrm{tr}}), \tag{3}$$

where A_{tr} is the area of the well (i.e., the area enclosed by the deep trench). The first factor is simply the intrinsic thermal resistance of the vertical well, while the second factor accounts for partial heat blocking by the trench walls. Heat transfer through the trench walls is accounted for by an additional parallel term:

$$R_{\mathrm{th,side}} = \frac{2W_{\mathrm{tr}}}{\kappa_{\mathrm{tr}} t_{\mathrm{tr}} P_{\mathrm{tr}}} \times \frac{2}{\pi} \arctan(t_{\mathrm{tr}}/d_{\mathrm{tr}}), \tag{4}$$

where W_{tr} is the trench width, κ_{tr} is the trench thermal conductivity, and P_{tr} is the perimeter of the well.

In the case of SOI, the buried oxide partially blocks heat flow. However, some small heat transfer must occur, or else the thermal resistance would be infinite. Such a 'quasi-adiabatic' surface can be modeled by the method of images [1], [9]. An infinite number of image heat sources can represent two adiabatic planes. The imperfect isolation is modeled by truncating the series of images to a finite distance, which is taken equal to the healing length m [11]:

$$R_{\mathrm{th,SOI}} = \frac{1}{2\pi\kappa_{\mathrm{Si}} t_{\mathrm{Si}}} \left(\frac{1}{\sqrt{1 + (L/4t_{\mathrm{Si}})^2}} + \log \frac{m}{3t_{\mathrm{Si}}} \right) \tag{5}$$

Finally, the effect of multiple fingers is modeled by a set of cross-heating components, representing the mutual heating between fingers. The cross-heating terms are computed by neglecting the finite size of the fingers [9], [11]:

$$R_{\mathrm{th,i,j}} = \frac{1}{2\pi\kappa_{\mathrm{Si}} d_{i,j}} \tag{6}$$

where $R_{\mathrm{th,i,j}}$ is the cross-heating between the i-th and the j-th fingers and $d_{i,j}$ is the distance.

Figures 6 to 9 show the comparison between the analytical models and numerical simulation and/or experimental data. We remark that the model is entirely predictive, i.e., no adjustment of model parameters was performed in order to fit the data. On the other hand, a careful evaluation of all geometric parameters was found to be crucial for the accuracy of the model. For our devices, we found it necessary to account for the presence of a LOCOS isolation, modeled as a shallow trench according to Eq. (3). The most important parameters in the model are the vertical dimensions, such as the trench depths and the heat-generation depth D. Since real bipolar transistors are not perfectly planar devices, there is some degree of ambiguity in the origin of vertical coordinates. For all models, we measured the vertical dimensions starting from the base-emitter metallurgical junction, consistently with the simplified picture of Ref. [1].

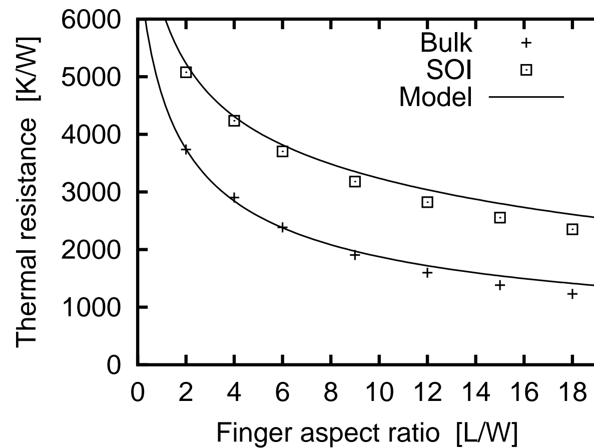

Figure 6: Comparison between numerical simulation (symbols) and compact model (lines) for the thermal resistance of single-finger bipolar transistors on bulk and SOI substrates, plotted as a function of the finger aspect ratio. The finger width is $W = 0.28\,\mu m$, and a $0.16\,\mu m$ shallow-trench isolation was included.

4 CONCLUSIONS

We have presented three-dimensional numerical simulations and analytical compact models for the thermal resistance of bipolar transistors on bulk and SOI substrates. Simulations were found to be in excellent agreement with available experimental data, and were employed for the exploration of a wide range of device structures. Analytical models were found to be accurate to within about 10% for a wide variation in the SOI and trench geometrical parameters, and can be used for predictive estimation of self-heating in state-of-the-art bipolar and BiCMOS integrated circuits.

REFERENCES

[1] R. C. Joy and E. S. Schlig, "Thermal proprieties of very fast transistors", *IEEE Trans. Electron Devices*, vol. 17, pp. 586, 1970.

[2] R. M. Fox and S.-G. Lee, "Scalable small-signal model for BJT self-heating", *IEEE Electron Device Letters*, vol. 12, pp. 649–651, Dec. 1991.

[3] J. S. Brodsky, R. M. Fox, and D. T. Zweidinger, "A physics-based dynamic thermal impedance model for vertical bipolar transistors on SOI substrates", *IEEE Trans. Electron Devices*, vol. 46, pp. 2333–2339, Dec. 1999.

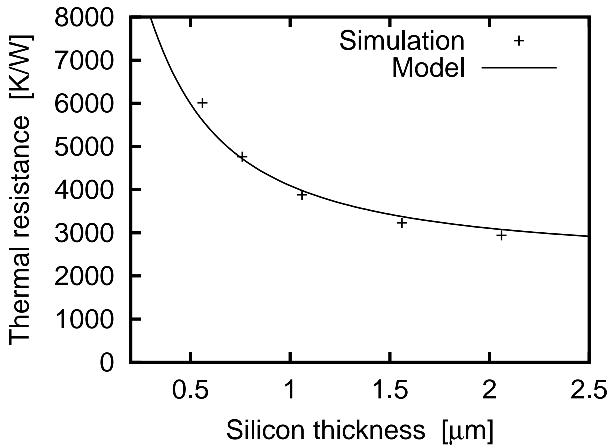

Figure 7: Comparison between numerical simulation (symbols) and compact model (lines) for the thermal resistance of single-finger bipolar transistors on SOI substrate, plotted as a function of the silicon thickness. The buried-oxide thickness is fixed at $0.4\,\mu m$.

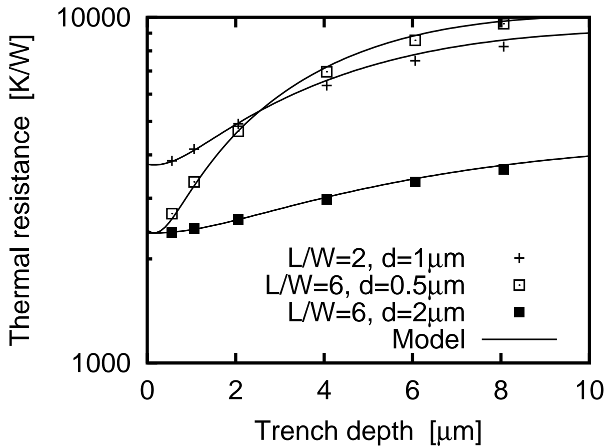

Figure 8: Comparison between numerical simulation (symbols) and compact model (lines) for the thermal resistance of single-finger bipolar transistors on bulk substrate with both shallow- and deep-trench isolation, for two finger aspect ratios ($L/W = 2$ and 6) and finger-to-trench spacing of 0.5, 1, and $2\,\mu m$. In all cases the deep trench is $1\,\mu m$ wide and entirely filled with oxide.

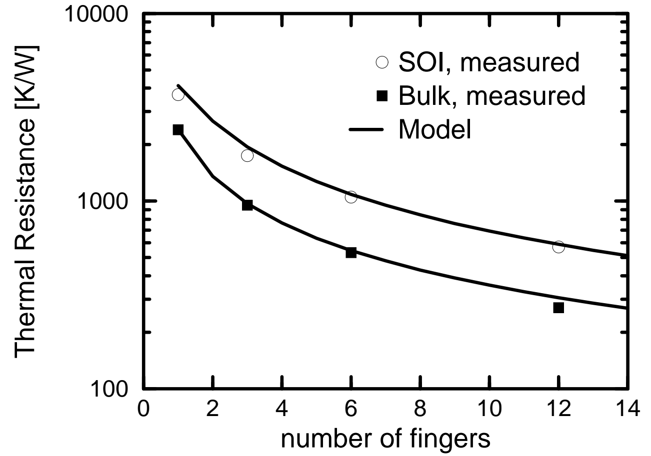

Figure 9: Comparison between measurement (symbols) and compact model (lines) for the thermal resistance of multi-finger devices on bulk and SOI substrates. Data are shown for a finger pitch of $3.56\,\mu m$ and finger aspect ratio $L/W = 6$. The thermal resistance is extracted from measurements as described in Ref. [9].

[4] Integrated Systems Engineering AG, Zurich, Switzerland, *DESSIS-ISE release 6.1*, 2000.

[5] M. Mastrapasqua, A. Pacelli, P. Palestri, and C. A. King, "Device simulation for advanced $Si_{1-x}Ge_x$ HBTs", in *Proc. Bipolar Circuits and Technologies Meeting*, 2001, pp. 42–51.

[6] C. A. King et al., "Very low cost graded SiGe base bipolar transistors for a high performance modular BiCMOS process", in *IEDM Tech. Dig.*, 1999, pp. 565–568.

[7] W. B. Joyce, "Thermal resistance of heat sinks with temperature-dependent conductivity", *Solid-State Electronics*, vol. 18, pp. 321–322, 1975.

[8] K. E. Goodson and M. I. Flik, "Effect of microscale thermal conduction on the packing limit of silicon-on-insulator electronic devices", *IEEE Trans. Components, Hybrids and Manufacturing*, vol. 15, pp. 715–722, 1992.

[9] P. Palestri, A. Pacelli, and M. Mastrapasqua, "Thermal resistance in $Si_{1-x}Ge_x$ HBTs on bulk-Si and SOI substrates", in *Proc. Bipolar Circuits and Technologies Meeting*, 2001, pp. 98–101.

[10] D. J. Walkey et al., "Extraction and modelling of thermal behavior in trench isolated bipolar structures", in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting*, 1999, pp. 97–100.

[11] A. Pacelli, A. Palestri, and M. Mastrapasqua, "Compact modeling of thermal resistance in bipolar transistors on bulk and SOI substrates", submitted to *IEEE Trans. Electron Devices*.