Characterization of “Multipath Interconnects” for Microelectronic and Nanotechnology Circuits

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ABSTRACT

A multipath interconnect carries a signal by using the concept of parallel processing by providing two or more paths between the driver and the load. These paths are stacked vertically isolated from one another by insulating layers between them. In this paper, we have used the Green’s function method to determine the parasitic capacitances associated with a system of multipath interconnects printed on a silicon-based substrate.

Keywords: Interconnects, capacitances, Green’s function, nanoelectronics, VLSI

1. INTRODUCTION

On the state-of-the-art microelectronic circuits, the transistors and other devices are often connected by the metallic interconnects though optical and superconducting interconnects have also been considered. On this front, the recent improvements have resulted in replacing aluminum interconnects with the copper lines that have resulted in lower propagation delays and hence higher chip speeds. “Nanotechnology” refers to the technology for designing, fabricating and applying nanometer-scale systems to the development of next-generation systems including nanocomputers. Formation of digital nanocomputers that promise dramatically increased computational speed and density requires the successful formation of molecular-scale devices that can switch between the on and off states. Even after the challenges of fabricating the molecular devices are successfully overcome, we still face the problem of connecting these devices in a circuit to carry the information from the output of one device to the input of the next device. This problem is usually referred to as the “Interconnect Problem”. The interconnect problem arises because of the extremely high density of devices in the circuit and because of the extremely high rapidity at which the information needs to be transmitted from one point in the circuit to the next. This requires an unprecedented high density of interconnects operating at unprecedented high speeds. Furthermore, an extremely large number of interconnects are needed not just for connecting the devices in a circuit but also for connecting the circuits together. This can lead to the excessive heating problem in addition to the unacceptably high crosstalk introduced by the very close proximity of the rather large number of interconnects. New interconnect strategies are required to tackle these problems. Ideas that have been tossed around are “wireless” interconnects and “stochastic” transmission though these are at best theoretical at present.

As a possible solution of the interconnect problem, we are studying “Multipath Interconnects” [1], a modified version of the traditional metallic interconnects. The modification consists of using the concept of parallel processing by providing two or more paths between the driver and the load (Fig. 1) to carry the signal. These paths are stacked vertically isolated from one another by insulating layers between them thereby taking the same area on the chip as a standard single-path interconnect. Such a structure can carry much larger currents on the chip and this interconnect structure can be built by an extension of the existing microelectronics fabrication infrastructure. Recently, we performed computer simulations of the propagation delays expected in a multipath interconnect [1]. Our results indicated that the overall interconnect delay would decrease as the number of paths is increased. Since these interconnects are expected to carry high current densities which can cause excessive local heating, we have also performed an analysis of the electromigration-induced failure of the multipath interconnects [1]. These results suggested that the median-time-to-failure (MTF) increases as the number of paths is increased. Clearly the multipath interconnects show great promise for microelectronic circuits or hybrid circuits consisting of both the microelectronic and nanotechnology devices. In this paper, we have determined the parasitic capacitances associated with a system of multipath interconnects printed on a silicon-based substrate by using the Green’s function method [2-5].

Fig. 1: Schematic diagram of a 3-section multipath interconnect (side view). The shaded area is an insulator such as silicon dioxide.

2. THE GREEN'S FUNCTION

The method of capacitance extraction used here employs the standard Green's function combined with the charge distribution on the conductors. The Green's function is given as follows:

$$G(p,q) = \frac{1}{4\pi\varepsilon|p-q|} \tag{1}$$

where G(p,q) represents the electrostatic potential at a point p due to a point charge at point q. This function when applied to a three dimensional Cartesian coordinate system becomes:

$$G(p,q) = \frac{1}{4\pi\varepsilon_1}\{\frac{1}{\sqrt{z_1^2+p^2}} - \frac{1}{\sqrt{(2z'+z_1)^2+p^2}} + \sum_{n=0}^{\infty}(-1)^n K^{(n+1)}[\frac{1}{\sqrt{[2(n+1)d-(2z'+z_1)]^2+p^2}} - \frac{1}{\sqrt{[2(n+1)d+z_1]^2+p^2}} + \frac{1}{\sqrt{[2(n+1)d+(2z'+z_1)]^2+p^2}} - \frac{1}{\sqrt{[2(n+1)d-z_1]^2+p^2}}]\} \tag{2}$$

Where

$$z_1 = z - z'$$

$$p = \sqrt{(x-x')^2+(y-y')^2}$$

$$K = (\frac{\varepsilon_1-\varepsilon_2}{\varepsilon_1+\varepsilon_2})$$

This is assuming that both points the are in a silicon dioxide layer with a thickness of d. In other words, the interconnects are surrounded by the silicon dioxide and and are at a height d above the silicon substrate. The silicon dioxide has a dielectric constant of ε_1 and the region above the silicon dioxide has a dielectric constant of ε_2.

2.1 The Charge Distribution

The charge is distributed evenly over the surface of all the conductors in the system using a shape function of two variables. The conductors are divided up into nodes with a width "a". The nodes are assigned a shape function of the following form:

$$f(x,y) = (C_2 - C_1x^2 - C_1y^2)^2 \tag{3}$$

Applying the boundary conditions that f(a,0)=0 and

$$\int_{-a}^{a}\int_{-a}^{a} f(x,y)dxdy = 1$$

values for the two constants are found to be:

$$C_1 = \frac{3\sqrt{5/13}}{2a^3} \tag{4}$$

$$C_2 = \frac{3\sqrt{5/13}}{2a} \tag{5}$$

Shown below in Fig. 2 is the graphical representation of the shape function that is assigned to each node. Notice that this function diverges from the desired value near the corners however depending on the integration step used the values near the corners may never be used in the estimation. If a very fine integration step is employed the values near the corners of the node should be set to zero to provide a better estimate of the charge distribution. By distributing these functions over the surface of the conductors so that each shape function overlaps, as shown below, the charge is distributed over the conductors.

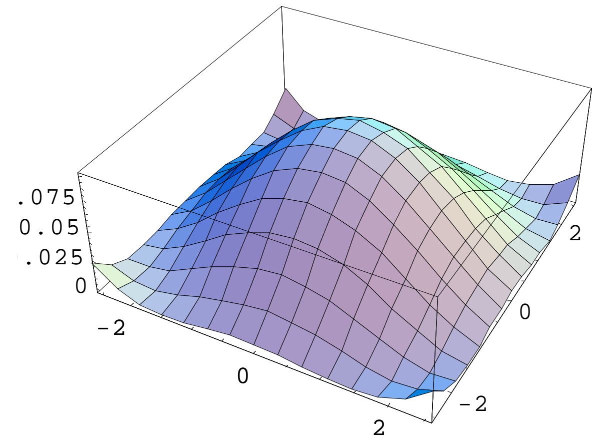


Fig. 2: Graphical representation of the shape function assigned to each node.

Using the Green's function and the charge distribution the electrostatic potential is found by using the equation:

$$\Phi(p) = \int_{charge} G(p,q)\sigma(q)dq \tag{6}$$

Extending this to an M conductor system yields:

$$\Phi_j(p) = \sum_{i=1}^{M} \int_{surface} G(p,q)\sigma_i(q)dA_i(q) \qquad (7)$$

j = 1, 2,…, M

Setting

$$F_{ji}(p) = \int_{ijnode} G(p,q) f_{ji}(q) dA_{ji}(q)$$

Equation (7) can be found to be:

$$\Phi_w(p) = \sum_{j=1}^{M} \sum_{i=1}^{N_j} \alpha_{ji} F_{ji}(p); \qquad w = 1, 2, \ldots, L \qquad (8)$$

where L is the total number of nodes in the system. Converting equations (7) and (8) to the matrix notation yields:

$$FA = J\Phi \qquad (9)$$

Using the basic capacitance matrix equation $Q = C\Phi$ and the previously developed equation, the ground and coupling capacitance values for all the conductors in the system are found by:

$$C = J^T F^{-1} J \qquad (10)$$

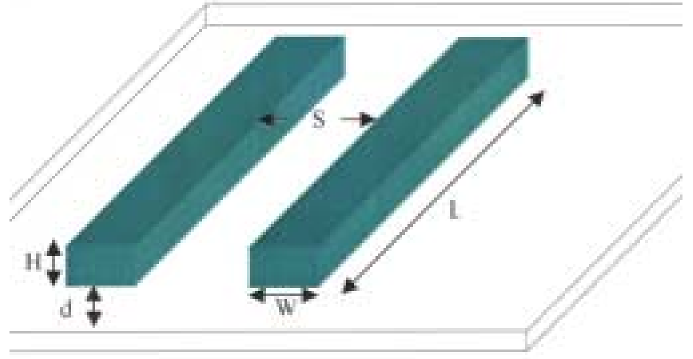
F is the LxL matrix of double integrals shown above and J is the incident matrix where element Jji = 1 if conductor i contains node j.

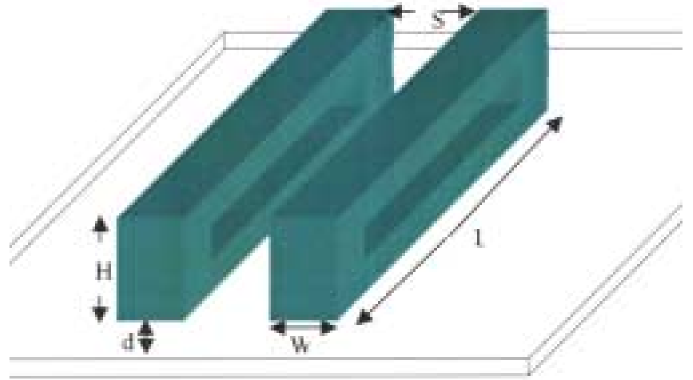
SIMULATION RESULTS

Schematic diagrams the 1-path, 2-path and 3-path interconnect structures simulated in this paper are shown in Fig. 3. These interconnects are placed on an SiO_2 layer which in turn is deposited on the silicon substrate. SiO_2 is also the insulating material separating the different paths in the same interconnect except on its ends. Further, all conductors are embedded in an SiO_2 layer 60 nm thick. The Silicon dioxide has a relative permitivity of 4.5 whereas silicon has a relative permitivity of 11.8. The various parameters used in the following simulation results and shown in Fig. 3 are:

L = Interconnect length
W = Interconnect width
H = Total height of each interconnect
S = Separation between the neighboring interconnects
d = Thickness of the oxide layer under the interconnect

Shown below in Fig. 4 is the total ground capacitance of a single 1-path interconnection structure. It is observed that the capacitance does indeed increase as expected since the surface area increases with the length. A linear relationship is also





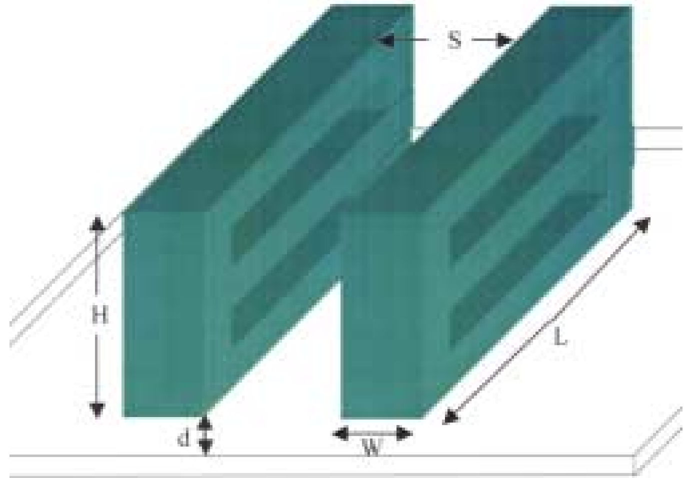


Fig. 3: Schematic diagrams of two 1-path, 2-path and 3-path interconnects.

expected since the capacitance will be directly proportional to the surface area of the interconnection. Since the width is held constant, the surface area of this conductor will increase linearly with an increase in length.

The total ground capacitance of a single 3-path interconnect is shown in Fig. 5. It shows that increasing the number of current carrying paths does not effect the overall

trend of the capacitance, i.e., it remains fairly linear. However, there is an overall increase in the capacitance.

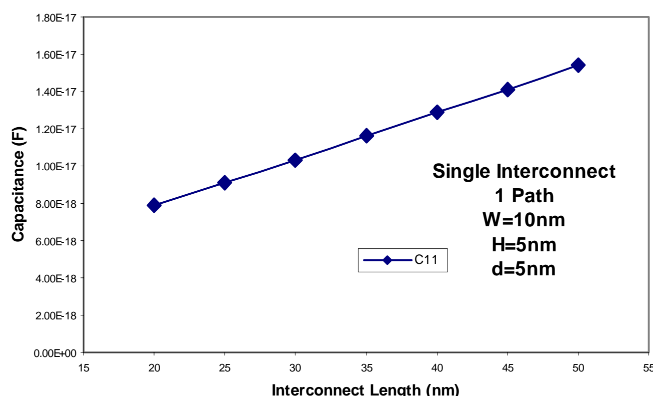


Fig. 4: Ground capacitance of a single 1-path interconnect.

Varying the separation between the neighboring interconnects has the effect seen Figs. 6 and 7 which show the dependences of the various ground and coupling capacitances on the separations between the neighboring interconnects for a system of 2 and 3 2-path interconnects, respectively. Both figures show a similar trend of a rapid decrease in capacitance when the interconnections are very close together and a decreasing rate when the conductors are moved further apart. The coupling capacitances are also seen to decrease as expected as the distance between the conductors is increased.

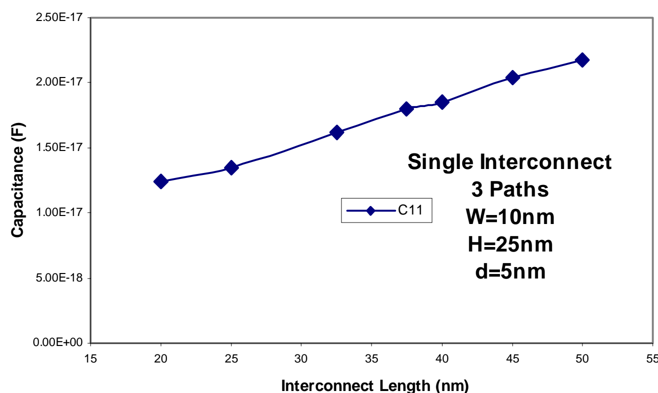


Fig. 5: Ground capacitance of a single 3-path interconnect.

CONCLUSIONS

These results show that multipath interconnects show similar capacitance behavior as do the corresponding single-path interconnects. However the current carrying capability of a multipath interconnection is expected to be much higher. Therefore it could be beneficial to use multipath interconnects since more current could be carried by the interconnect in relation to the amount of additional capacitance that the interconnect adds to the circuit. This structure could also lead to higher values of median-time-to-failure (MTF) due to electromigration and also result in lower propagation delays as shown earlier [1].

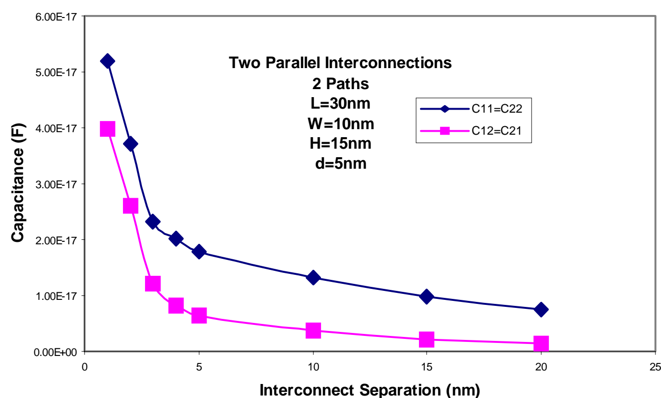


Fig. 6: Dependences of the ground and coupling capacitances for a system of two 2-path interconnects on separation.

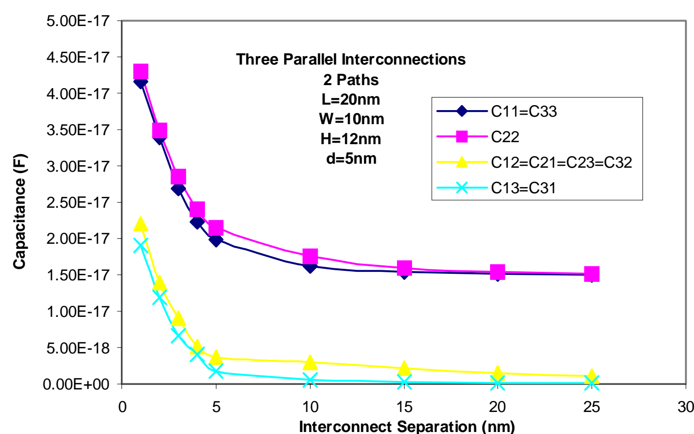


Fig. 7: Dependences of the ground and coupling capacitances for a system of three 2-path interconnects on separation.

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