Modeling and Simulation of 3D Structures for Gigabit DRAM

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ABSTRACT

In this paper, we present a 3D topography simulator, so-called 3D-SURFILER(SURface proFILER), to model a complicated 3D structure on the substrate for gigabit DRAMs. The 3D-SURFILER comprises a deposition and etching simulator employing a cell advancing scheme and a parallel computational numerical engine. An MIM (Metal-Insulator-Metal) stacked capacitor [1] has been chosen to verify the validity of the simulator.

Keywords: modeling, topography, deposition, etching, process simulation, process integration, parallel computation, DRAM.

INTRODUCTION

A great deal of attraction has been made on topography simulation in order to generate a three-dimensional simulation structure having a complex geometry. Despite of many efforts to accurately model the topographical evolution of complex semiconductor structures on the substrate [2-4], the currently available topography simulator lacks the capability to represent a complex 3D structure such as a DRAM cell capacitor on a bit line with multi-level interconnects. These simulators suffer from the memory requirement and the extensive CPU time. It is widely understood that three-dimensional numerical calculation with a large simulation area requires a huge memory size and CPU time for the serial computational approach [5].

In this work, a novel cell-advancing scheme has been developed to resolve the computational difficulties and applied to model the topographical evolution of the complex structure on the wafer during deposition and etching process. Furthermore, a parallel computational method with a domain decomposition scheme was employed to drastically reduce the calculation time.

SIMULATION MODEL

If the device structures to be analyzed are strongly non-planar and complex, they cannot be obtained only from layout information. Therefore, an accurate topography simulation must be performed. Otherwise, large errors can exist, which makes the simulated 3D structures useless.

In our solution, topography simulation is performed by the user-defined process recipe, which is generated by layout and run-sheet editor. Furthermore, 3D-SURFILER supports an interactive run-sheet editing feature with graphic user interface and a layout-editing feature for the process integration. The run-sheet editor supervises and controls the simulation tasks. The layout editor allows the user to add, delete, or change the layout by editing windows for specifying materials, process recipe, and mask layers. Thereafter, the subsequent process simulation is carried out in accordance with the user-defined process recipe and the layout structures. The 3D-SURFIELR also provides an interactive graphic user interface mode for inputting a process recipe.

Our tool includes chemical and physical models for maintaining a high accuracy, too. The etching process is simulated with the plasma sheath Monte Carlo module and the analytic module [6] included in the simulator. These modules calculate the angular and energy distributions of energetic particles, and the distributions obtained can be used to study profile evolution. For sputter deposition, the sputter yield is calculated by employing the Monte Carlo method. The sputter yield of atoms as a function of incident energy, incident angle, and atomic ejection distribution is calculated for a wide range of 10eV~100keV.

A topographical model that dynamically allocates memory for surface evolution, so-called cell advancing model, has been developed. The traditional problem of a large memory size can be resolved by dynamically allocating only the surface cells for storing the complete information about topography and material. In the meanwhile, all of the cells including the surface cells are assigned with a corresponding material index. A complex 3D structure on the wafer is decomposed into multiple domains, followed by parallel computational steps through multiple processors. The parallel-computing program

involves modules such as film deposition, dry etching, photolithography, and CMP (Chemical Mechanical Polishing).

Figure 1 is a schematic workflow illustrating the parallel computation of the 3D-SURFILER. Referring to Figure 1, the simulation region on the wafer is decomposed into a multiple of domains in proportion to the number of the process elements (PEs). First of all, each domain is assigned to the individual process element, followed by parallel computational steps through multiple processors, as shown in Figure 1. The method is very efficient because the multiple processors do not communicate with their data during parallel computation.

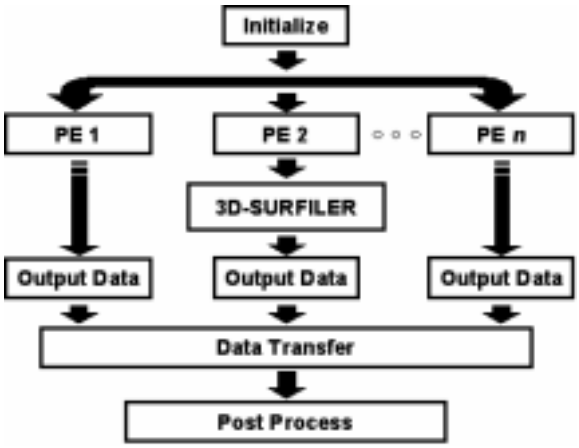


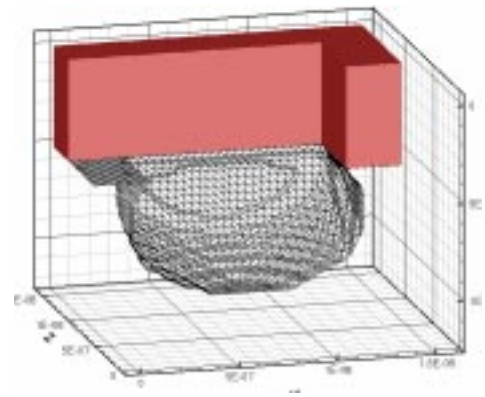
Figure 1: Schematic diagram illustrating the workflow of the parallel calculation.

SIMULATIONS

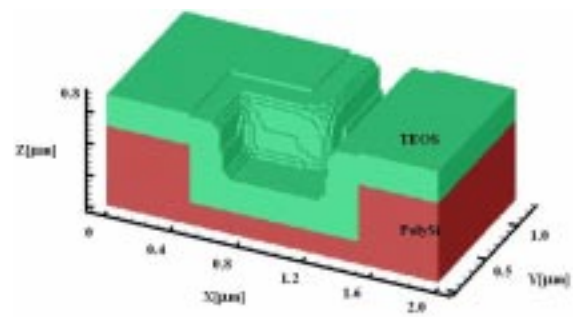
Plasma Deposition and Dry Etching Process

Figure 2(a) and Figure 2(b) are schematic diagrams illustrating an etch profile during a plasma etching step at 600 mTorr and a deposition profile, respectively. Referring to Figure 2(a), a negative slope on the wall can be observed under the mask, which ions hit the bottom of the trench resulting in a higher etch rate there and a negative profile slope under the mask is shown due to the sidewall etching of the scattered ions. The angular and energy distributions of the incident ions are calculated by Monte Carlo method in topography simulation. In this simulation, the etch rate is assumed to be 50_/sec and the mask window size is chosen as 1μm×1μm.

In order to investigate the flow and reflow characteristics of an inter-metal dielectric (IMD), an exemplary simulation of the CVD (Chemical Vapor Deposition) of TEOS (Tetraethylorthosilicate) was performed. The deposition rate is assumed to be 50_/sec and the analysis region is chosen as 2μm×1μm×0.8μm (100×50×40 cells). Referring to Figure 2(b), the improved step coverage of the contact hole is due to the gap-filling capability of conformal TEOS layer. Consequently, the thickness of the deposited TEOS layer is uniform all over the surface.



(a)



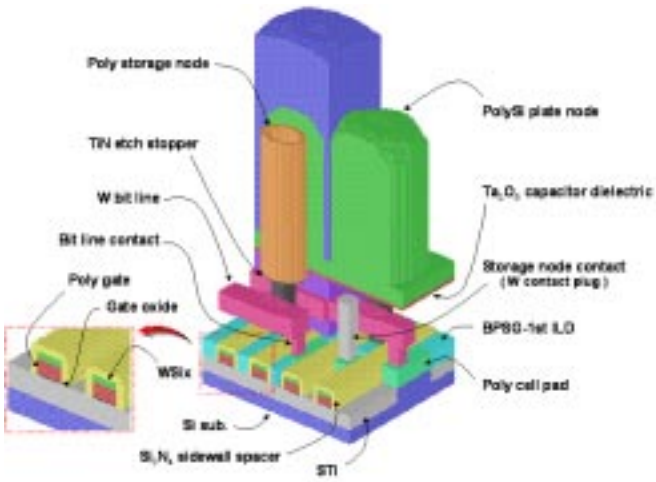
(b)

Figure 2: Schematic views illustrating the results of topography simulation: (a) a simulation result of the dry etching process at 600 mTorr; (b) a simulation result of TEOS deposition process.

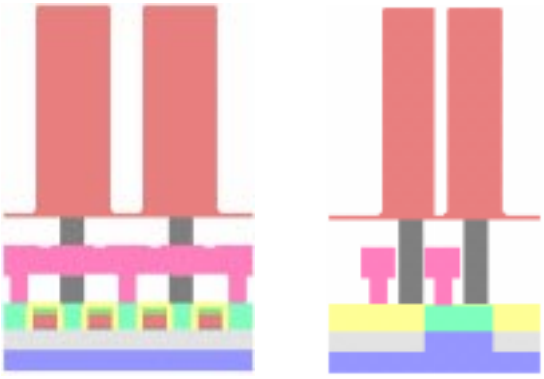
Process Integration of a DRAM cell

One of the most useful applications of a topography simulator lies in the area of process integration. An MIM stacked capacitor was chosen to test the capability of 3D-SURFILER. Figure 3 is a schematic diagram illustrating a final profile structure on the wafer after virtual processing in accordance with the user-defined layout and process recipe. The process sequence begins with the definition of the STI (Shallow Trench Isolation), followed by the formation of word line and bit line. Thereafter, the storage nodes are defined on the polysilicon layer, and finally Ta_2O_5 film for the cell capacitor is deposited. In this

example, 5475600 (130_ 156 270) cells were employed for the simulation region of 1.3µm_1.56µm_ 2.7µm. For an overall structure with 5475600 cells, the simulator requires about 22 Mbytes to represent the topography, and the CPU time is 64082 seconds.



(a)



(b) (c)

Figure 3: Schematic views illustrating (a) the simulation result of a part of the final profile, (b) the results from word line and (c) bit line direction.

Figure 4 is a schematic diagram illustrating a domain decomposition of a DRAM cell capacitor with four process elements on CRAY T3E computer. Figure 5 is a schematic diagram illustrating the dependence of required CPU time on the number of processing elements. Referring to Figure 5, the total CPU time decreases approximately in a proportional manner as the number of process elements increases.

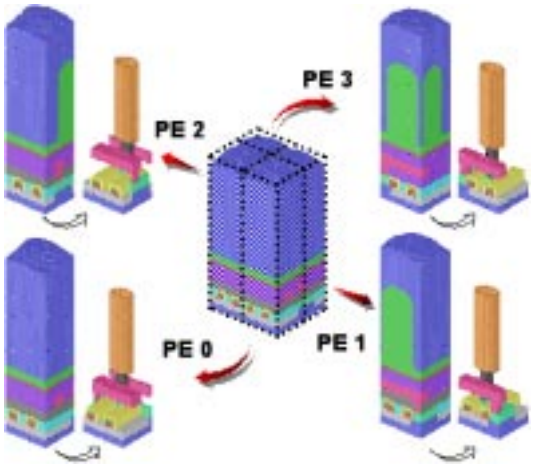


Figure 4: Schematic view illustrating the simulation result of a DRAM cell capacitor with 4 process elements.

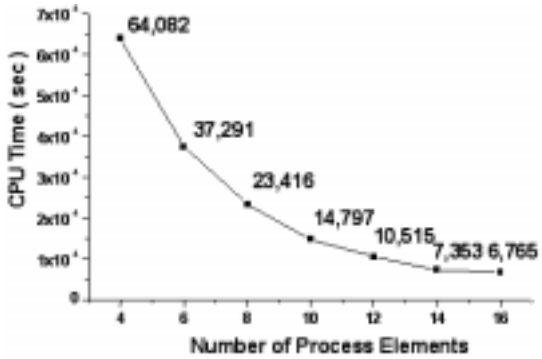


Figure 5: Schematic view illustrating the dependence of required CPU time.

CONCLUSION

In this paper, we report a method to model 3D complex topography. A topography model that dynamically allocates memory is proposed to resolve an extensive memory requirement. The parallel-computing capability makes is possible to save system resources and simulation time. Topography simulation based on cell advancing model was proposed with a process recipe, which can be defined by the user-friendly layout and run-sheet editor. A cylinder-type cell capacitor was chosen to test the capability of our model. In this example, a total of 5475600 (130×156×270) cells were employed for the simulation of semiconductor regions including four DRAM cell capacitors with a dimension of 1.3µm×1.56µm×2.7µm. The required size of memory is about 22 Mbytes and typical simulation time is 64082 seconds.

ACKNOWLEDGEMENT

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