IBM SRDC-Bangalore, INDIA

Effective Width Modeling for BC devices in SOI

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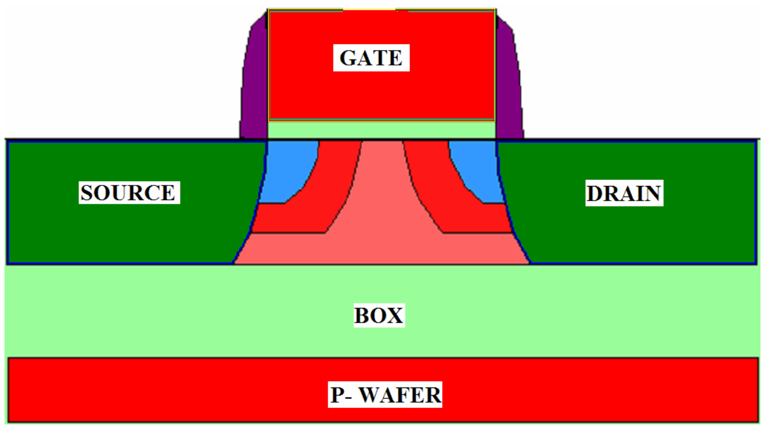
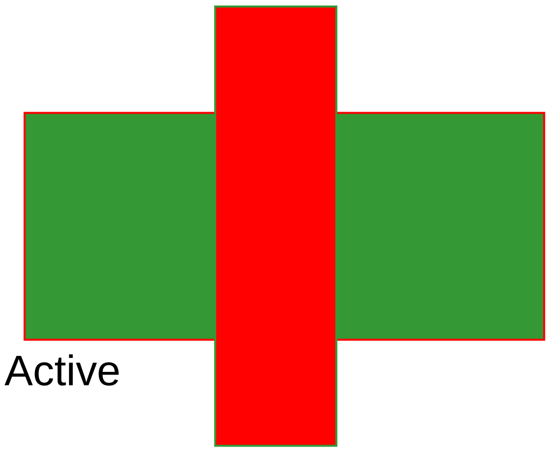
Outline

- **SOI FET Overview**
- **Width offset problem description : Thick gate oxide devices**
  - Solution
  - Implementation & Results
- **Width offset problem description : Thin gate oxide devices**
  - Solution
  - Implementation & Results
- **Summary**

Silicon on Insulator : FET



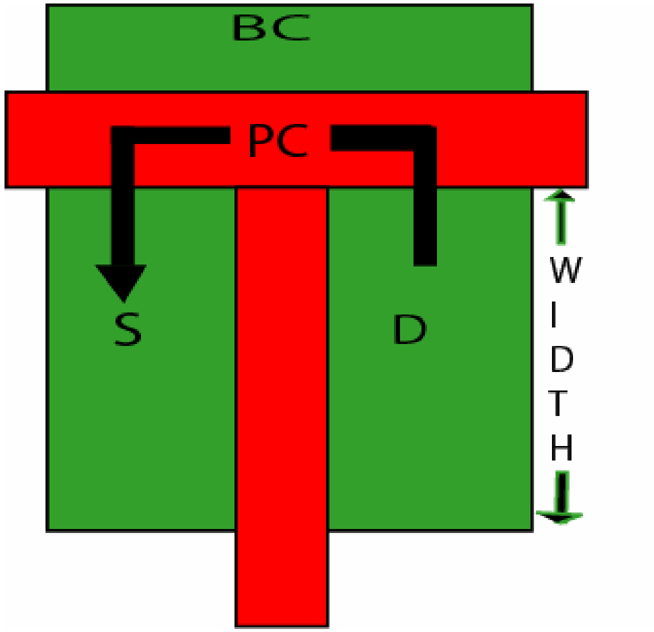


Active

Poly-Silicon

- Lower extrinsic capacitances
- Higher Currents compared to bulk devices
- Higher digital circuit speeds
  - but
- Kink Effect creates problem in analog circuits

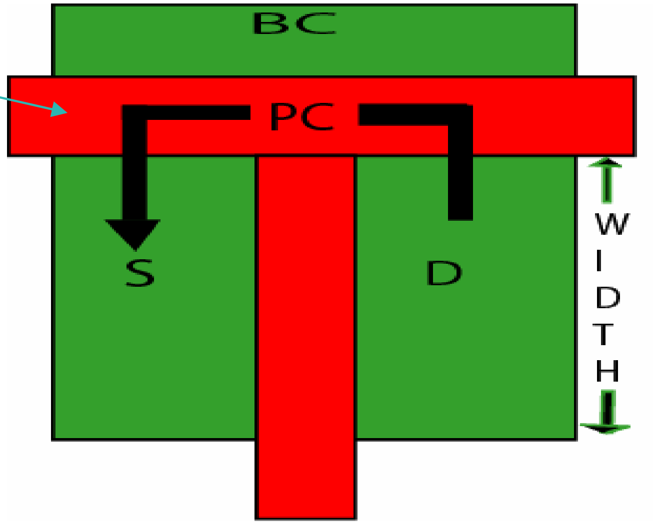
Silicon on Insulator : Body Contacted FET



- To avoid kink effect
- Special layout needed
- T & H type layouts used
- Special layout causes extra current

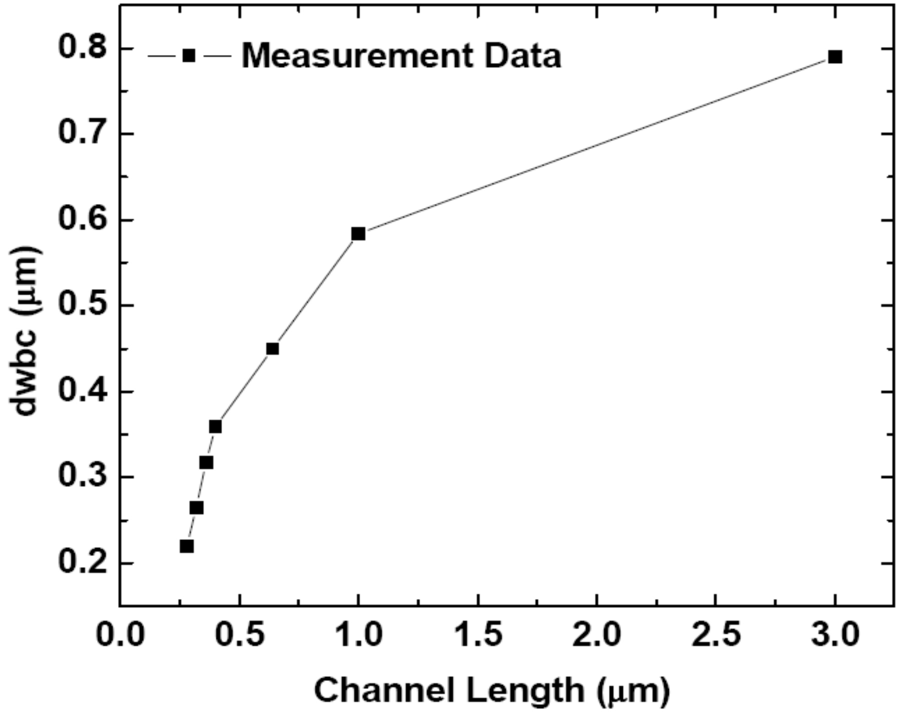
Width offset modeling

- BC device has this width offset due to extra current
  - Standard BSIMSOI has only constant width offset **dwbc** for BC devices coming from layout
  - With constant width offset it was difficult to fit different channel length devices
  - Is dwbc constant with length?



dwbc scaling with geometry

- For thick-oxide devices

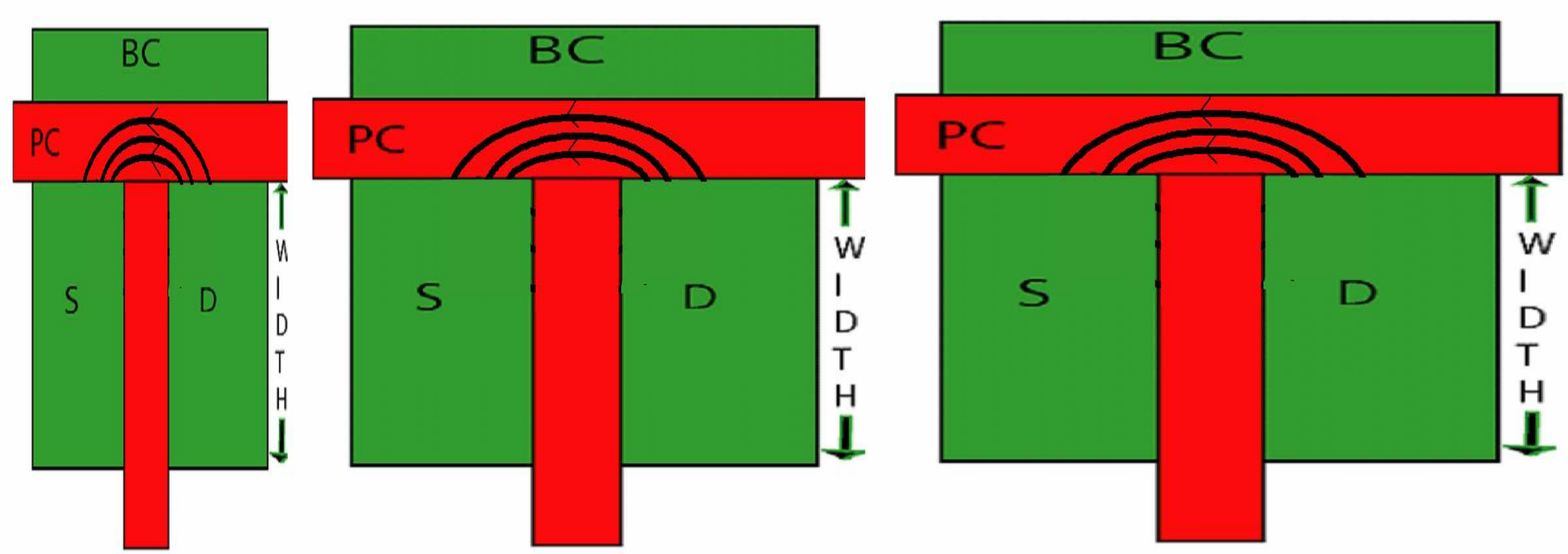


- BC and FB device has only extra poly piece as difference
- Ratio of linear currents gives dwbc

$$\frac{I_{BC}}{I_{FB}} = \frac{W_{BC}}{W_{FB}}$$

$$dwbc = W_{eff}\frac{I_{BC}}{I_{FB}} - W_{eff}$$

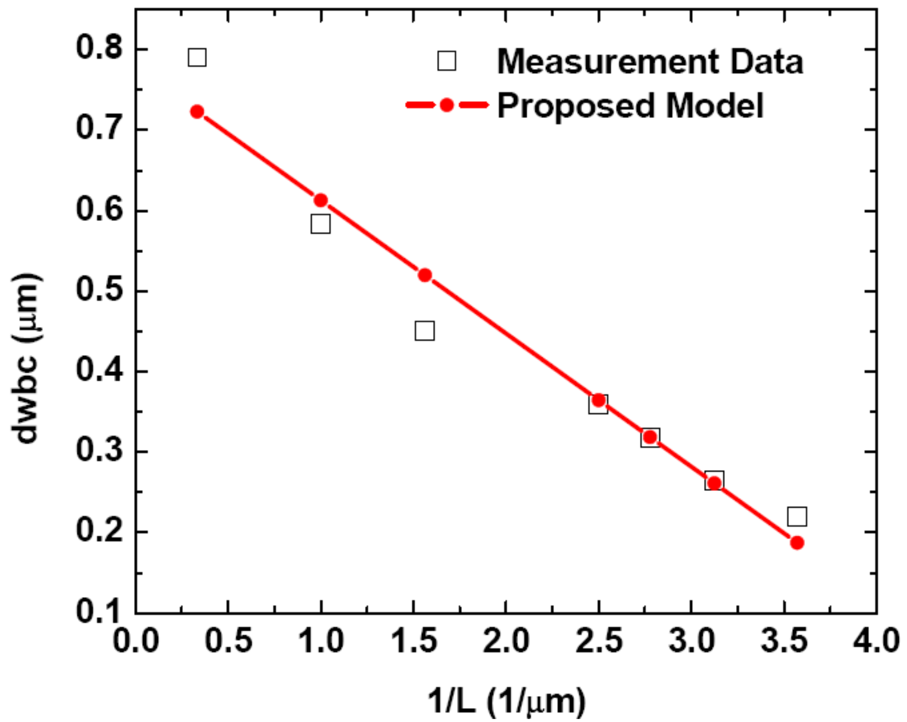
Length Dependence : dwbc



- Field lines for extra current increases with increase in length
- Finally layout is the physical limit

Dwbc scaling

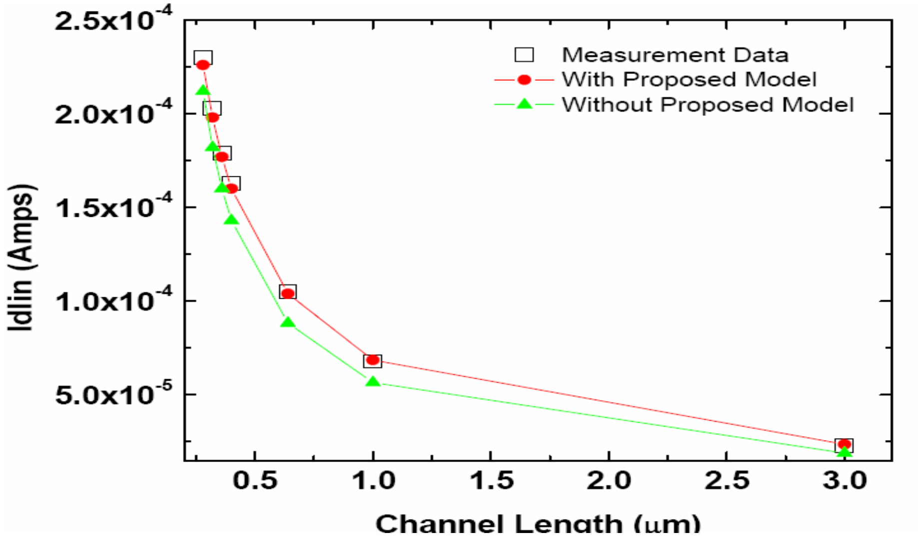
- For thick oxide devices

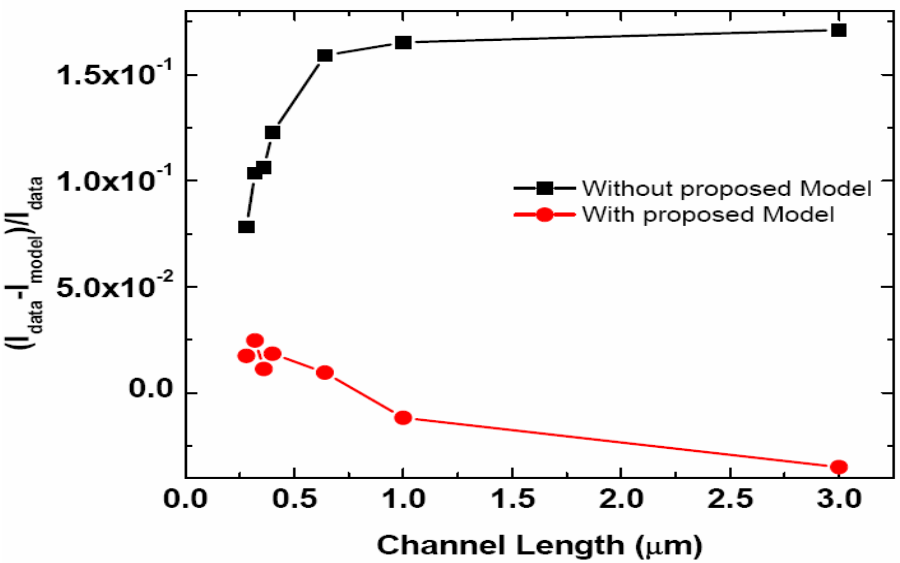


- Increase in channel length causes increase in field lines from drain to source for extra current
- Increase in width offset in limited by physical limit from the layout
- Proposed equation to model this effect

$$dwbc = dwbc_0 - \frac{dwbc_l}{L}$$

Implementation & Results

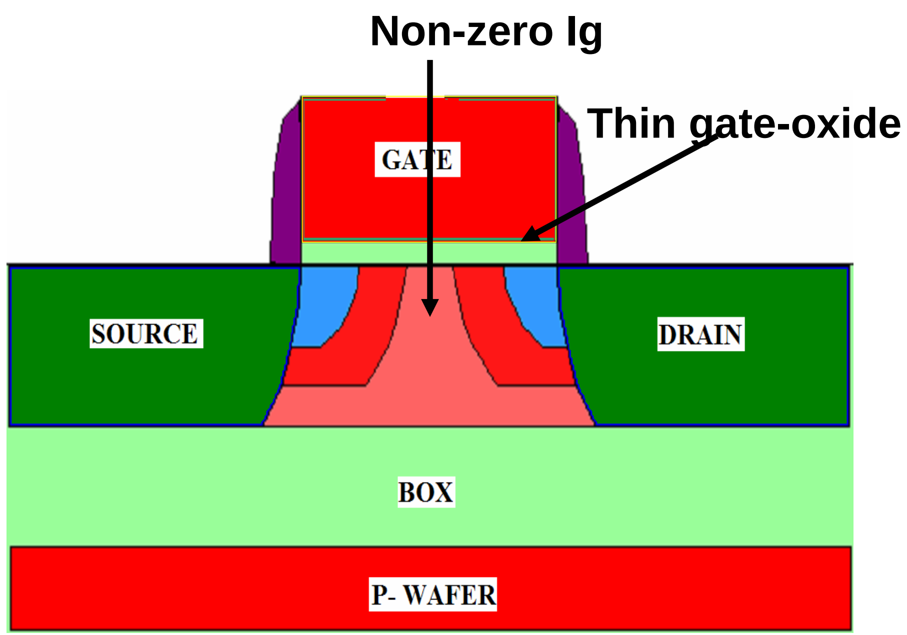




- Equation implemented using sub-circuit approach
- Improvement in the model observed from Ilin Vs L scaling fits
- Error plot validates the equation

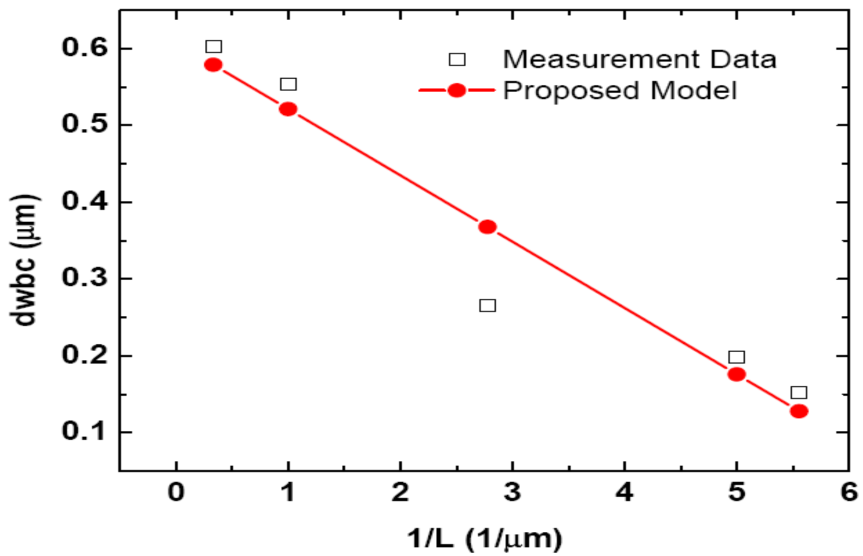
Dwbc : Thin-oxide Devices

- Thin-oxide BC and FB devices will have different linear Vt due to gate-leakage
- Gate leakage raises body-potential of FB device and changes Vt
- How to extract dwbc for thin-oxide devices?



dwbc scaling for thin-ox devices

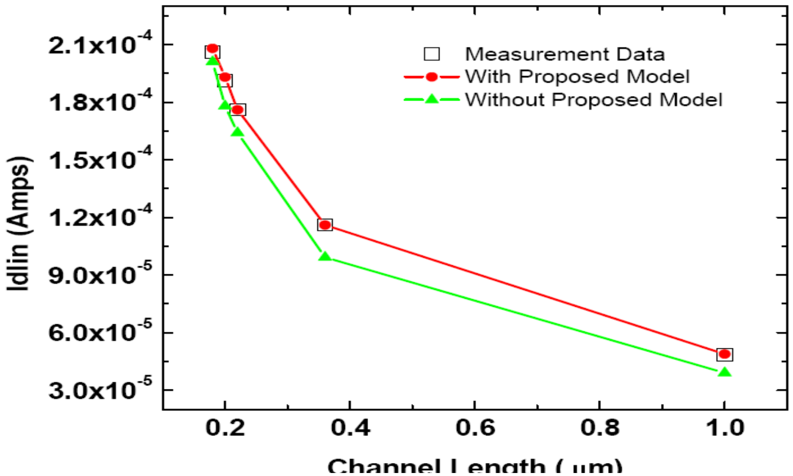
- For thin-oxide dwbc extraction done by comparing linear peak trans-conductance
- Peak trans-conductance takes care of Vt change coming from gate leakage
- Ratio of peak linear trans-conductance is thus measure of dwbc
  - For thin oxide FETs



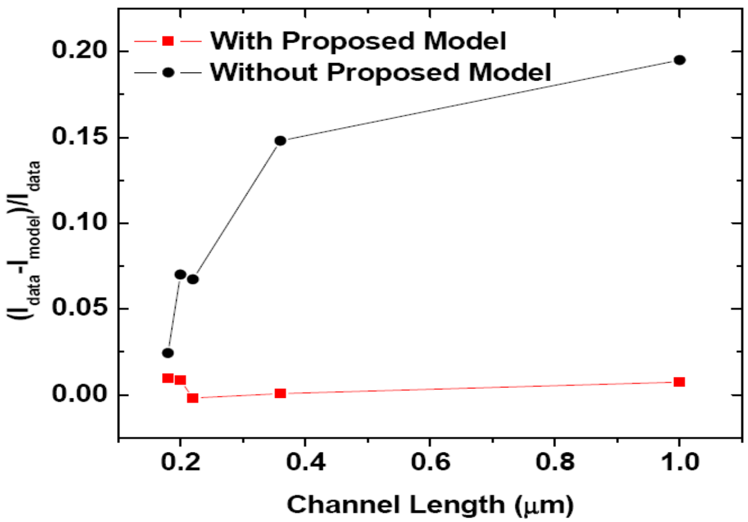
$$\frac{gm_{peak,BC}}{gm_{peak,FB}} = \frac{W_{BC}}{W_{FB}}$$

$$dwbc = dwbc_0 - \frac{dwbc_l}{L}$$

Implementation & Results



- Improvement in fits for Ilin Vs L for thin oxide FETs



- Error plot shows the signature of dwbc

Summary

- Width offset In BC devices in SOI has length dependence
- Effect seen for both thick and thin-oxide BC devices
- This work provides method to extract width-offset for both type of devices
- Proposed equation to capture the effect seems to have reasonable fits for both type of devices