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A Unified Compact model for FinFET and Silicon Nanowire MOSFETs

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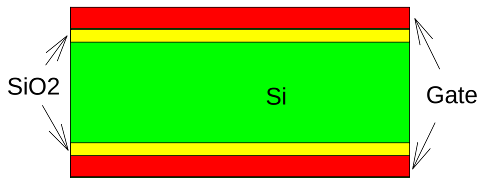
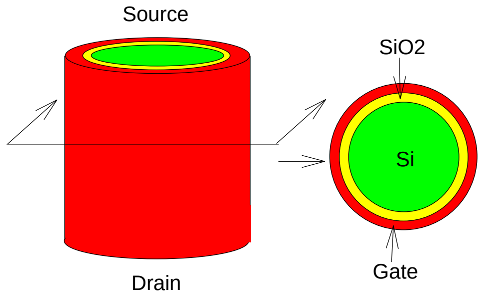
Outline

- **Introduction to FinFET and SiNW MOSFETs**
- **Compact Model Formulation**
- **Results & Discussion**

FinFET and SiNW MOSFETs





- ☐ **Why FinFET and SiNW MOSFETs**
  - Superior control of short channel effects
- ☐ **Similarities**
  - Same cross-section
  - Undoped silicon channel
- ☐ **Differences**
  - Cylindrical vs. Cartesian

Surface Potential Formulation

- **FinFET (Double Gate)**

$$\frac{d^2\phi}{dx^2} = \frac{qn_i}{\varepsilon_{Si}} e^{(\phi - V_c)/v_{th}}$$

- **First integration**

$$V_{gf} - \phi_s = \Upsilon_i \sqrt{v_{th}\left(e^{(\phi_s - V_c)/v_{th}} - e^{(\phi_o - V_c)/v_{th}}\right)}$$

- **SiNW MOSFETs**

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right) = \frac{qn_i}{\varepsilon_{Si}} e^{(\phi - V_c)/v_{th}}$$

- **First integration**

$$V_{gf} - \phi_s = \Upsilon_i \sqrt{v_{th}\left(e^{(\phi_s - V_c)/v_{th}} - e^{(\phi_o - V_c)/v_{th}}\right)}$$

Drop Phi0, we have the same surface potential expression!

$$\phi_s\left[V_c\left(y\right)\right] = V_{gf} - 2v_{th}\mathcal{L}\left\{\frac{\Upsilon_i}{2\sqrt{v_{th}}} e^{(V_{gf} - V_c)/2v_{th}}\right\}$$

Inversion charge

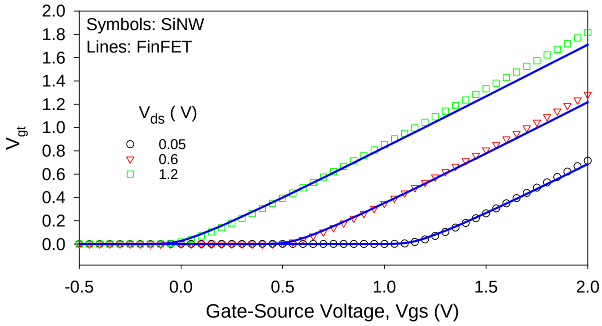
- **Integrate Poisson equation twice**

FinFET (DG)

$$V_{gt,c}(V_c)=\Upsilon_i\sqrt{v_{th}e^{\frac{\phi_s(V_c)-V_c}{v_{th}}}}\sin\left(\frac{\Upsilon_i C_{ox}}{\varepsilon_{Si}}\frac{T_{Si}}{4v_{th}}\sqrt{v_{th}e^{\frac{\phi_o(V_c)-V_c}{v_{th}}}}\right)$$

SiNW

$$V_{gt,c}(V_c)=\frac{Rqn_i}{2C_{ox}}e^{(\phi_s+\phi_0-2V_c)/2v_{th}}$$



Terminal current and charge

- Terminal current (all major short channel effects built in)

$$I_{ds}=2\mu_{eff0}C_{ox}\frac{W}{L}\left(V_{gf}-\overline{\phi_s}+2v_{th}\right)\left(V_{d,eff}-V_{s,eff}\right)$$

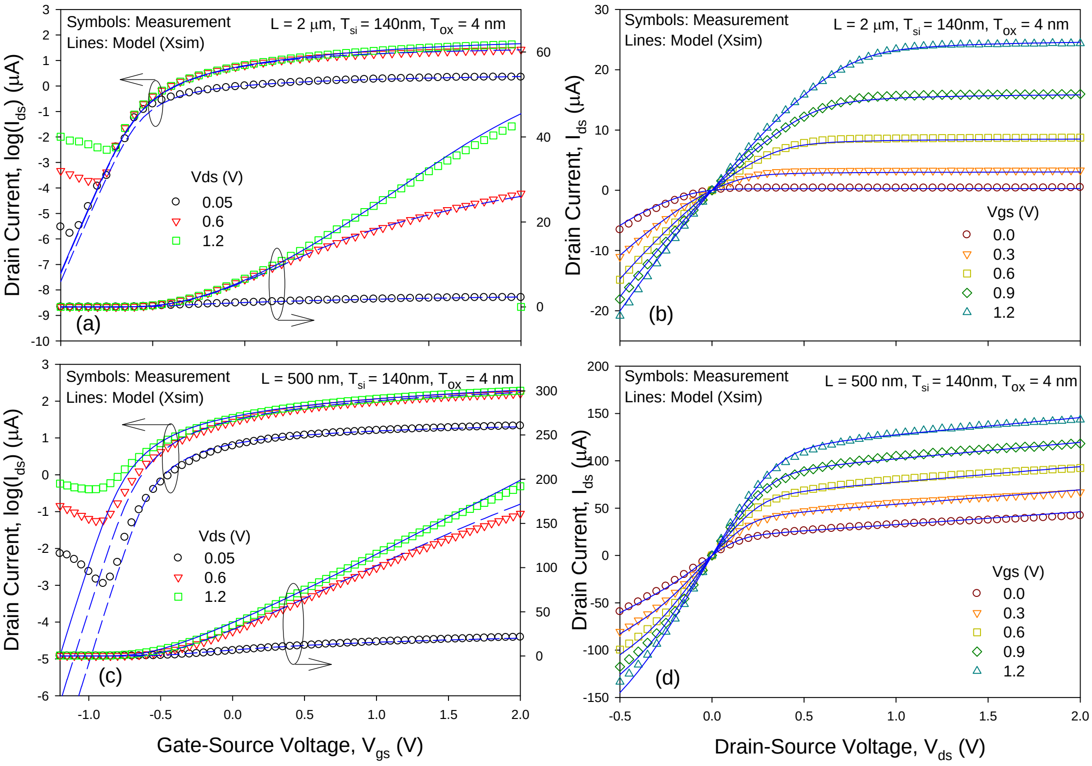
- Terminal charge based on explicit surface potential

$$Q_D=\frac{WC_{ox}L_{eff}}{2}\left(\overline{q_i}-\frac{\Delta\phi}{6}\left(1-\frac{\Delta\phi}{2H}-\frac{\Delta\phi^2}{20H^2}\right)\right)$$

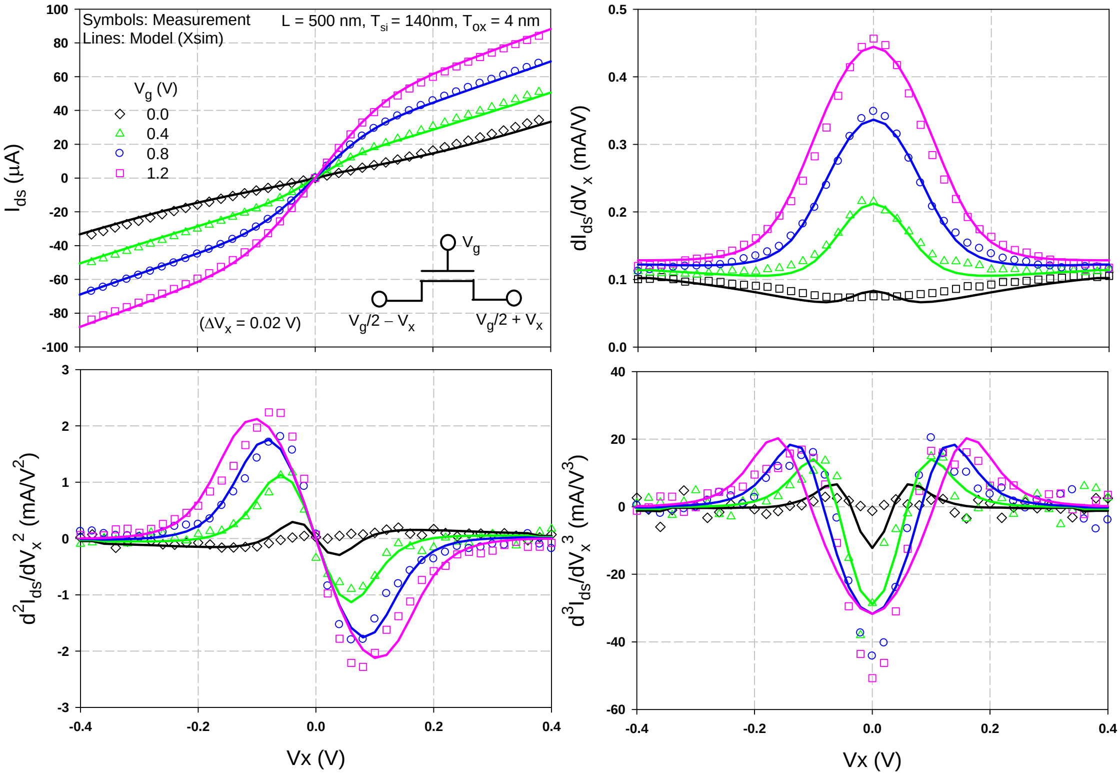
$$Q_S=\frac{WC_{ox}L_{eff}}{2}\left(\overline{q_i}+\frac{\Delta\phi}{6}\left(1+\frac{\Delta\phi}{2H}-\frac{\Delta\phi^2}{20H^2}\right)\right)$$

$$Q_g=Q_s+Q_d$$

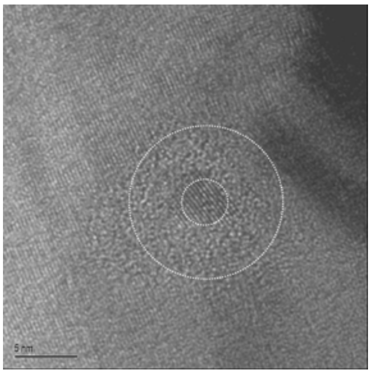
Model verification (FinFET)

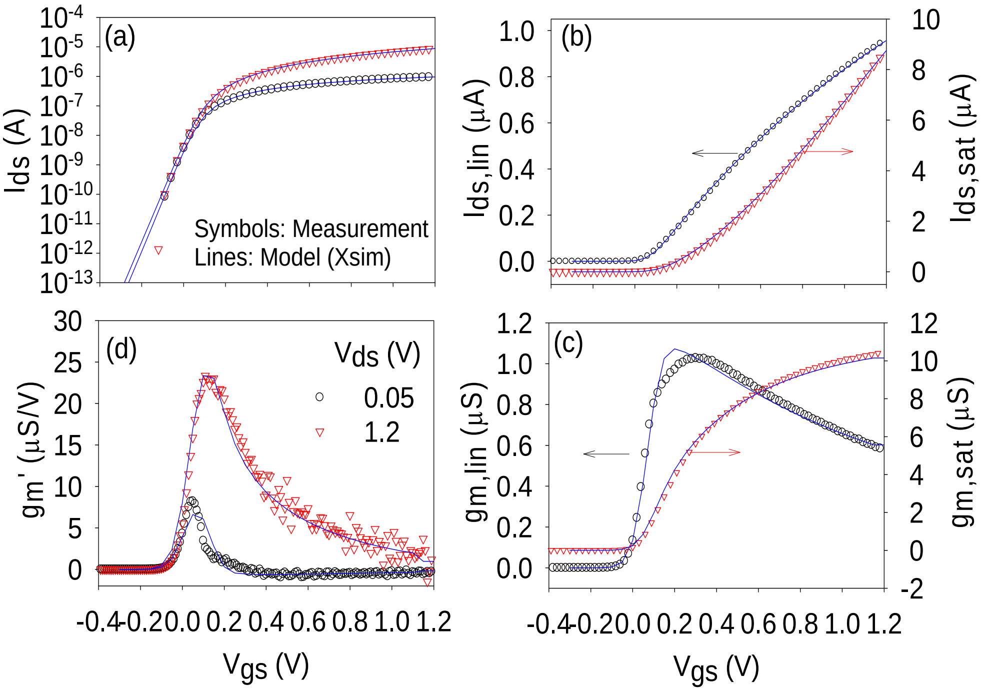


Perfect Symmetry (FinFET)

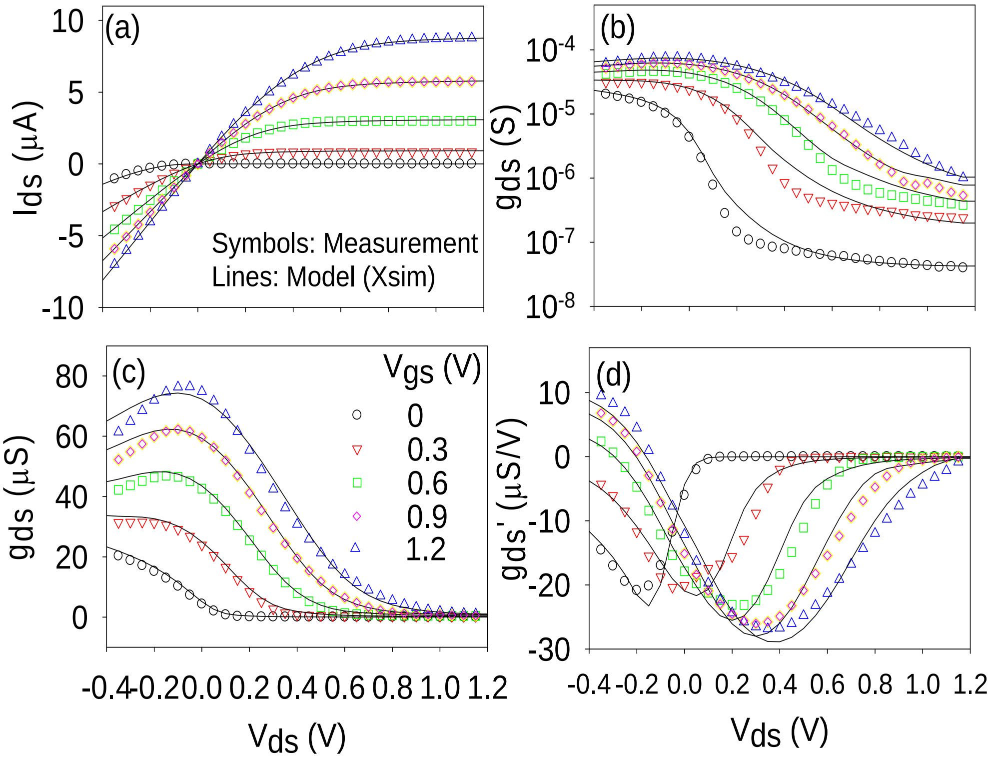


Model verification (SiNW)

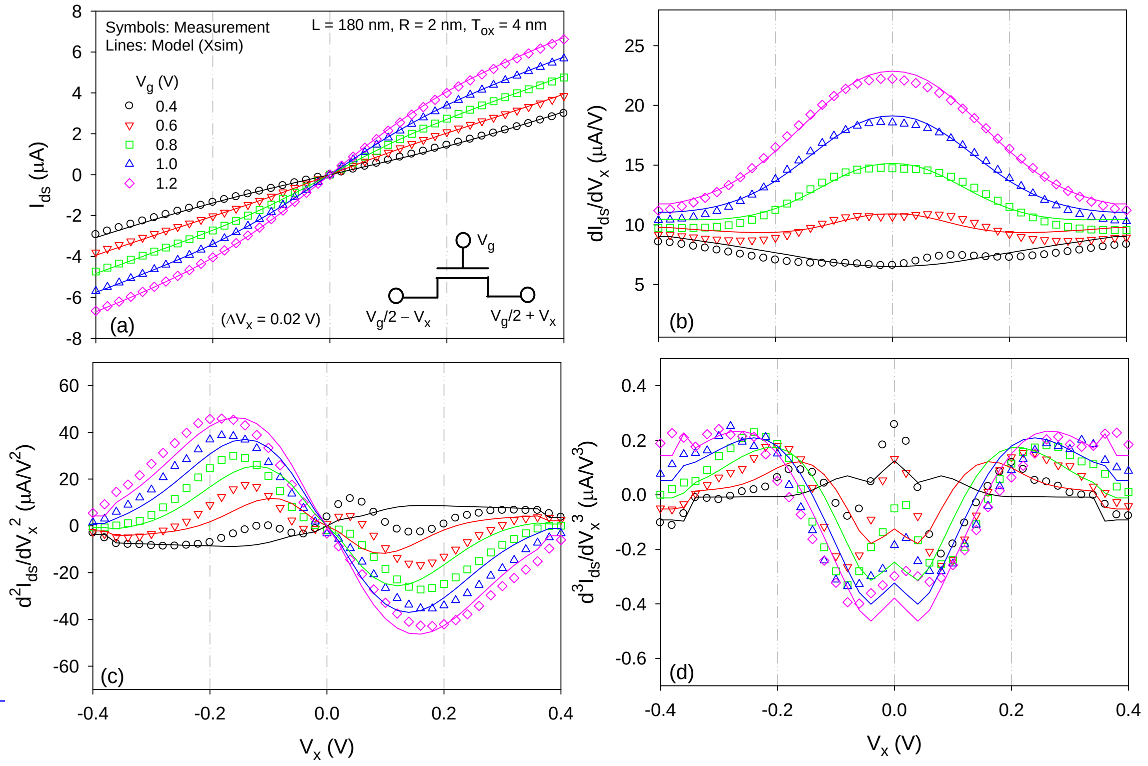




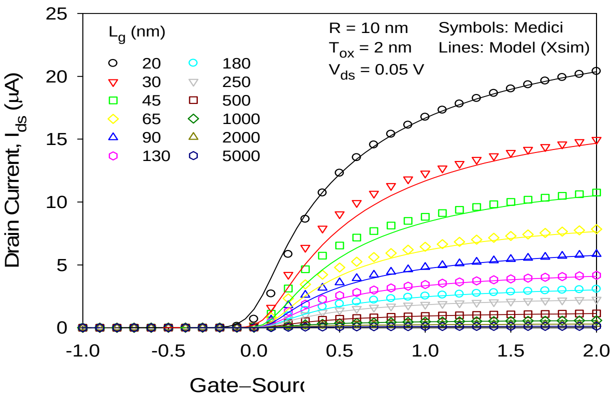
Model verification (SiNW)

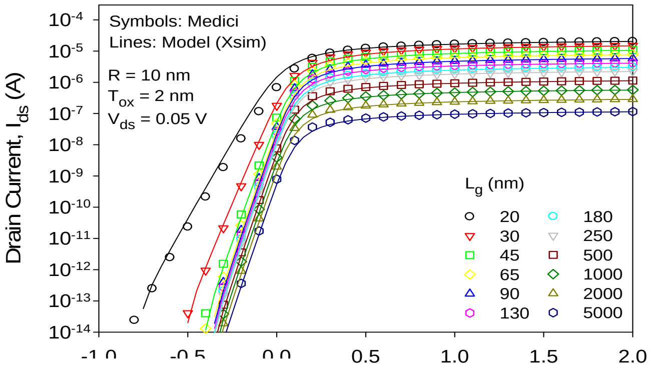


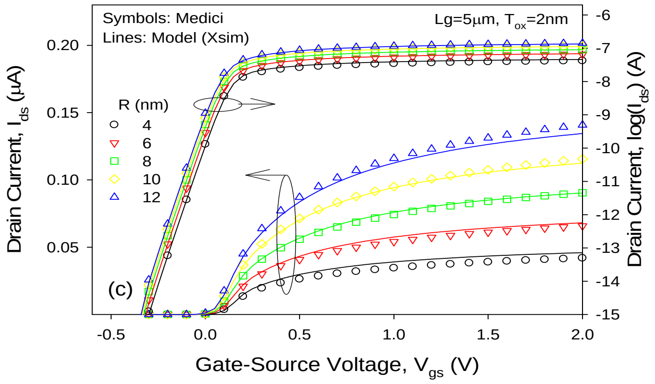
Perfect Symmetry (SiNW)



Model Scalability

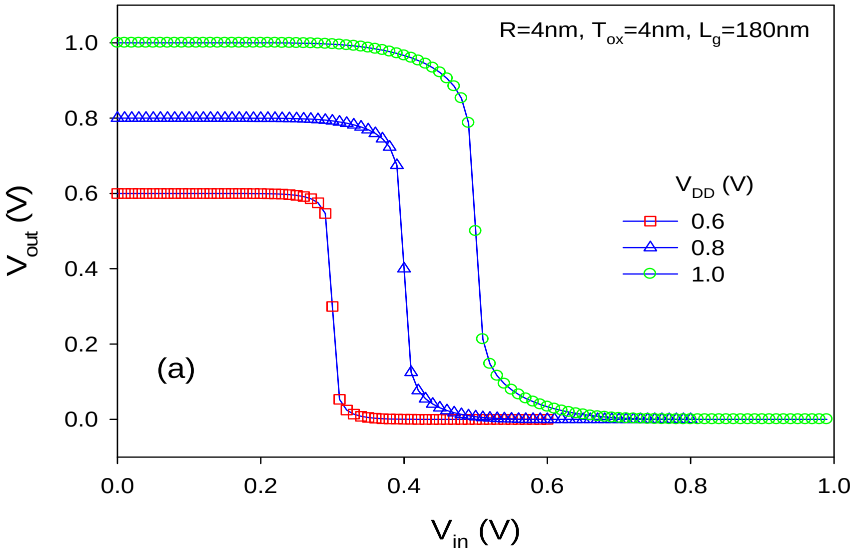






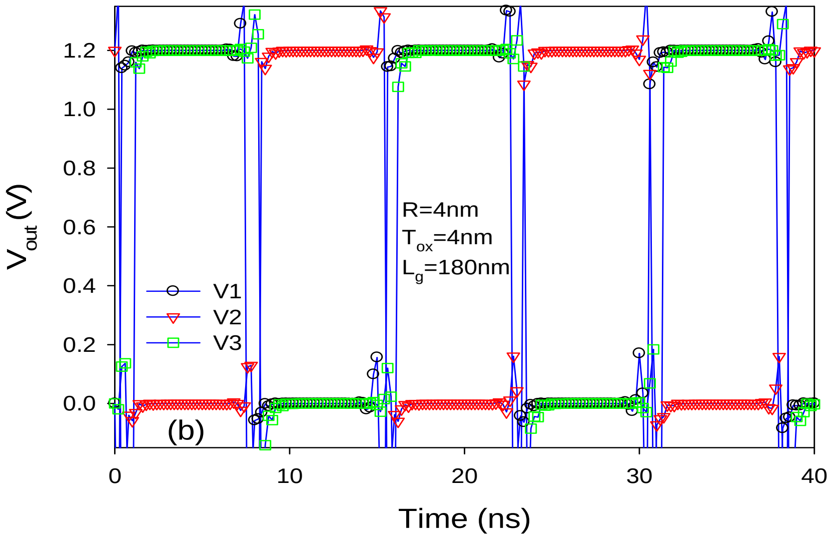
Circuit Simulation (Verilog A)

- Dc transfer characteristics of an inverter



Circuit Simulation (Verilog A)

- Transient characteristic of a 21 stage ring oscillator



Conclusions

☐ A unified compact model for FinFET and SiNW MOSFETs is formulated and fully consistent with bulk/SOI model. The model has been coded using Verilog-A and stable circuit simulation is achieved

☐ Model is verified with data from both FinFET and SiNW measurements, including high order derivatives of drain current