



June 3–4 2008

 **NSTI Nanotech 2008**
Hynes Convention Center, Boston, Massachusetts, June 1–5, 2008

11th Annual
4000 attendees & 400 exhibitors

Boston, Massachusetts, U.S.A.

The seventh

Workshop on Compact Modeling

Workshop Chair: Xing Zhou

Room 201

Hynes Convention Center

Boston, MA, USA



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WCM poster session:

Wed, 5:30–7:00, Room 302

Poster presenters: please set up your posters, there will be no oral briefing



Tue, June 3 2008

Session Chair: Christian Enz

WCM-1

Bulk MOS Models

- 8:30** **JUNCAP2 Express: an extremely efficient evaluation of the JUNCAP2 model**
G.D.J. Smit, A.J. Scholten, D.B.M. Klaassen, NXP Semiconductors, NL
- 9:00** **Modeling of gain in advanced CMOS technologies**
A. Spessot, F. Gattel, P. Fantini, A. Marmiroli, STMicroelectronics, IT
- 9:20** **Effective Drive Current in CMOS Inverters for Sub-45nm Technologies**
J. Hu, J.E. Park, G. Freeman, H.S.P. Wong, Stanford University, US
- 9:40** **Process Aware Compact Model Parameter Extraction for 45 nm Process**
A.P. Karmarkar, V.K. Dasarapu, A.R. Saha, G. Braun, S. Krishnamurthy, X.-W. Lin, Synopsys (India) Pvt. Ltd., IN



Tue, June 3 2008

Session Chair: Dirk Klaassen

WCM-2

Noise/Statistical Models

- 10:30** Compact Modeling of Noise in non-uniform channel MOSFET
A.S. Roy, **C.C. Enz**, T.C. Lim and F. Danneville, *CSEM & EPFL, CH*
- 11:00** An Iterative Approach to Characterize Various Advanced Non-Uniformly Doped Channel Profiles
R. Kaur, R. Chaujar, M. Saxena, R.S. Gupta, *University of Delhi, IN*
- 11:20** Modeling of Spatial Correlations in Process, Device, and Circuit Variations
N. Lu, *IBM, US*
- 11:40** Model Implementation for Accurate Variation Estimation of Analog Parameters in Advanced SOI Technologies
S. Suryagandh, N. Subba, V. Wason, P. Chiney, Z-Y Wu, B.Q. Chen, S. Krishnan, M. Rathor, A. Icel, *Advanced Micro Devices, US*



Tue, June 3 2008

Session Chair: Mitiko Miura-Mattausch

WCM-3

Multiple-gate Models

- 1:30** *Capacitance modeling of Short-Channel DG and GAA MOSFETs*
H. Børli, S. Kolberg, T.A. Fjeldly, Norwegian University of Science and Technology, NO
- 2:00** *New Properties and New Challenges in MOS Compact Modeling*
X. Zhou, G.H. See, G. Zhu, Z. Zhu, S. Lin, C. Wei, A. Srinivas, J. Zhang, Nanyang Technological University, SG
- 2:20** *Unified Regional Surface Potential for Modeling Common-Gate Symmetric/Asymmetric Double-Gate MOSFETs with Quantum-Mechanical Effects*
G.H. See, X. Zhou, G. Zhu, Z. Zhu, S. Lin, C. Wei, J. Zhang, A. Srinivas, Nanyang Technological University, SG
- 2:40** *Quasi-2D Surface-Potential Solution to Three-Terminal Undoped Symmetric Double-Gate Schottky-Barrier MOSFETs*
G. Zhu, G.H. See, X. Zhou, Z. Zhu, S. Lin, C. Wei, J. Zhang, A. Srinivas, Nanyang Technological University, SG



Tue, June 3 2008

Session Chair: Tor Fjeldly

WCM-4

Multiple-gate/DG Models

- 3:30** *Construction of a Compact Modeling Platform and Its Application to the Development of Multi-Gate MOSFET Models for Circuit Simulation*
M. Miura-Mattausch, M. Chan, J. He, H. Koike, H.J. Mattausch, T. Nakagawa, Y.J. Park, T. Tsutsumi, Z. Yu, Hiroshima University, JP
- 4:00** *Unified Regional Surface Potential for Modeling Common-Gate Symmetric/Asymmetric Double-Gate MOSFETs with Any Body Doping*
G.H. See, X. Zhou, G. Zhu, Z. Zhu, S. Lin, C. Wei, J. Zhang, A. Srinivas, Nanyang Technological University, SG
- 4:20** *Surface Potential versus Voltage Equation from Accumulation to Strong Region for Undoped Symmetric Double-Gate MOSFETs and Its Continuous Solution*
J. He, Y. Chen, B. Li, Y. Wei, M. Chan, PEKING University, CN
- 4:40** *Modeling of Floating-Body Devices Based on Complete Potential Description*
N. Sadachika, T. Murakami, M. Ando, K. Ishimura, K. Ohyama, M. Miyake, H.J. Mattausch, M. Miura-Mattausch, Hiroshima-University, JP



Tue, June 3 2008

Session Chair: Josef Watts

WCM-Panel

Compact Models for Manufacturability

Panelist:

- **NVIDIA, B-K. Liew, US**
- **TSMC, A. Doganis, US**
- **H. Trombley, IBM, US**
- **S. Rochel, Blaze DFM, US**

Questions:

- What information does the circuit designer need to know in order to design products which meet their design goals across the whole process window.
- How can this information be delivered to and used by the circuit designer.

Whatever your design goals, to achieve them in silicon you must account for manufacturing variation in your design. A typical foundry collects a huge amount of information on process variation. But this information is not available to the circuit designer in a form that can be used to make design decisions.

Compact models have traditionally come with fixed corner files which are useful predicting best and worst case delays of static CMOS logic but not appropriate for other types of circuits or other circuit characteristics. Each member of the Panel will address two board questions from the perspective of their own experience.



Wed, June 4 2008

Session Chair: Michael Schröter

WCM-5

Interconnect/Interface/ESD Models

- 8:30** ***The Driftless Electromigration Theory (Diffusion-Generation-Recombination-Trapping)***
C-T Sah, B.B. Jie, University of Florida, US
- 9:00** ***Adaptable Simulator-independent HiSIM2.4 Extractor***
T. Gneiting, T. Eguchi, W. Grabinski, AdMOS GmbH Advanced Modeling Solutions, DE
- 9:20** ***Recent Advancements on ADMS Development***
B. Gu, L. Lemaitre, Freescale Semiconductor, US
- 9:40** ***Source/Drain Junction Partition in MOS Snapback Modeling for ESD Simulation***
Y. Zhou, J.-J. Hajjar, Analog Devices, Inc., US



Wed, June 4 2008

*Session Chair: **Xuemei Xi***

WCM-6

HBT/BiFET/HV Models

- 10:30** *Improved layout dependent modeling of the base resistance in advanced HBTs*
S. Lehmann, M. Schroter, University of Technology Dresden, DE
- 11:00** *The Bipolar Field-Effect Transistor Theory (A. Summary of Recent Progresses)*
B.B. Jie, C-T Sah, Peking University, CN
- 11:20** *The Bipolar Field-Effect Transistor Theory (B. Latest Advances)*
C-T Sah, B.B. Jie, University of Florida, US
- 11:40** *An Accurate and Versatile ED- and LD-MOS Model for High-Voltage CMOS IC Spice Simulation*
B. Tudor, J.W. Wang, B.P. Hu, W. Liu, F. Lee, Synopsys, Inc., US



Wed, June 4 2008

Session Chair: Bin B. Jie

WCM-7

Diode/SOI/DG Circuit Models

- 1:30** *Modeling of PN Diode Based Phase-Change Memory Access Circuit*
M. Chan, K. Lu, T.D. Happ, B. Rajendran, H-L Lung, C. Lam, HKUST, HK
- 2:00** *Analytical Modelling and Performance Analysis of Double-Gate MOSFET-based Circuit Including Ballistic/quasi-ballistic Effects*
S. Martinie, CEA LETI-MINATEC, FR
- 2:20** *An Improved Impact Ionization Model for SOI Circuit Simulation*
X. Xi, F. Li, B. Tudor, W. Wang, W. Liu, F. Lee, P. Wang, N. Subba, J-S Goo, Synopsys Inc, US
- 2:40** *Parameter Extraction for Advanced MOSFET Model using Particle Swarm Optimization*
R.A. Thakker, M.B. Patil, K.G. Anil, Indian Institute of Technology, IN



Wed, June 4 2008

Session Chair: Mansun Chan

WCM-8

DG/FinFET Models

- 3:30** *Compact Models for Double Gate MOSFET with Quantum Mechanical Effects using Lambert Function*
H. Abebe, H. Morris, E. Cumberbatch, V. Tyree, University of Southern California, ISI, US
- 3:50** *Neural Computational Approach for FinFET Modeling and Nano-Circuit Simulation*
M.S. Alam, A. Kranti, G.A. Armstrong, Z. H. College of Engineering & Technology, IN
- 4:10** *Closed Form Current and Conductance Model for Symmetric Double-Gate MOSFETs using Field-dependent Mobility and Body Doping*
V. Hariharan, R. Thakker, M.B. Patil, J. Vasi, V.R. Rao, IIT Bombay, IN
- 4:30** *Comparison of Four-terminal DG MOSFET Compact Model with Thin Si channel FinFET Devices*
T. Nakagawa, T. Sekigawa, T. Tsutsumi, Y. Liu, M. Hioki, S. O'uchi, H. Koike, Electoinformatics Group, JP
- 4:50** *MOSFET Compact Modeling Issues for Low Temperature (77 K - 200 K) Operation*
P. Martin, M. Cavelier, R. Fascio, G. Ghibaud, CEA-LETI Minatec, FR



Thank you for your participation!

Presenting authors:

Call for volunteer contribution of presentation slides

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WCM events

Hope to see you all next year at WCM2009:

May 3-7 2009, Houston, TX, USA

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