

Modeling Process Variations Using a Compact Model

Raghu Murali, James Meindl

Microelectronics Research Center,
Georgia Institute of Technology, Atlanta GA.

Email: raghu@gatech.edu

Outline

- Introduction
- Model Derivation
- Model Verification
- Model Applications

Manufacturing Variation

- Gate-length – lithography, etch
- threshold voltage – dopant fluctuation
- interconnect* – lithography, CMP, LER
- die-to-die (D2D) vs within-die (WID)

* Lopez et al, IITC, June 2007, San Francisco CA

Tackling Variations

Architecture

variation-tolerant system design

System

Circuit

circuit optimization

Layout

regular layout

Device

body-bias, pocket doping

Manufacturing

increase process tolerance

Previous Work

- Monte-Carlo simulations
- Worst-case analysis
- curve-fit models
- compact model based on semi-empirical models

Model Derivation

$$T_{PD-chain} = \frac{1}{b} \cdot n_{CP} \cdot T_{PD} \quad (1)$$

clock-skew factor

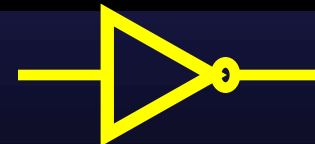
of gates in
critical path

delay of a single gate



$$T_{PD} = f_{ineff} \cdot \frac{C_L \cdot V_{DD}}{I_{dsat}} \quad (2)$$

effective fan-in factor



Model Derivation

Sakurai alpha-power model

$$I_{dsat} = K \mu C_{ox} \frac{W}{L} \cdot (V_{DD} - V_t)^\alpha \quad (3)$$

threshold voltage modeled
with physics-based derivation

Propagation delay standard-deviation

$$\sigma_{T_{PD}} = \sigma_L \cdot \frac{dT_{PD}}{dL} \quad (4)$$

computation requires a V_t rolloff model

Threshold Voltage Modeling

- Physics-based derivation based on 2-D Poisson equation
- More details in *R. Murali et al, IEEE TED, June 2004.*

$$\Delta V_T = 2\Gamma \cdot \Theta \left\{ 1 + \sqrt{1 - \frac{\chi_1(\psi_{bi}, y_j) \chi_1(\psi_{bi} + V_{ds}, y_j)}{[\chi_1(\psi_{bi}, y_j) + \chi_1(\psi_{bi} + V_{ds}, y_j)] \Gamma \cdot \Theta}} \right\}$$

$$\Theta = \frac{[\chi_1(\psi_{bi}, y_j) + \chi_1(\psi_{bi} + V_{ds}, y_j)] \exp(-\lambda_1 L/2)}{\kappa_1 - 2 \exp(-\lambda_1 L/2)}$$

$$\chi(V, y_j) = A_1(V) + B_1(V, y_j)$$

$$A_1(V) = V + V_{fb} - V_{TL} - \frac{qN_A}{\epsilon_{Si} \lambda_1^2}$$

$$\Gamma = \frac{\exp(-\lambda_1 L/2)}{\kappa_1 + 2 \exp(-\lambda_1 L/2)}; \quad \psi_{bi} = \frac{kT}{q} \ln \left(\frac{N_A N_{D_{source/drain}}}{n_i^2} \right)$$

$$\kappa_1 = \frac{1}{2} \left[1 + \frac{C_{ox} d}{\epsilon_{Si}} \left(1 + \left(\frac{\lambda_1 \epsilon_{Si}}{C_{ox}} \right)^2 \right) \right]$$

$$d = \sqrt{\frac{2\epsilon_{Si}}{qN_A} 2\phi_F}; \quad \phi_F = \frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right)$$

$$V_{TL} = V_{fb} + 2\phi_F + \frac{\sqrt{2q\epsilon_{Si}N_A \cdot 2\phi_F}}{C_{ox}}$$

$$B_1(V, y_j) = \left[V - V_{bs} + \frac{qN_A}{\epsilon_{Si} \lambda_1^2} \right] \left[\frac{\epsilon_{Si} \lambda_1}{C_{ox}} \sin(\lambda_1 d) - \cos(\lambda_1 d) \right]$$

Compact Model for Delay Variance

$$\sigma_{T_{PD}} = \sigma_L \cdot \mu_{T_{PD}} \left[\frac{\alpha \cdot \Delta V_t}{V_{DD} - V_t} \cdot \frac{\lambda}{2} \cdot \left(\frac{\theta}{\theta - e^{-\lambda \cdot L_{eff}/2}} \right) + \frac{\kappa}{L_{eff}} \right] \quad (5)$$

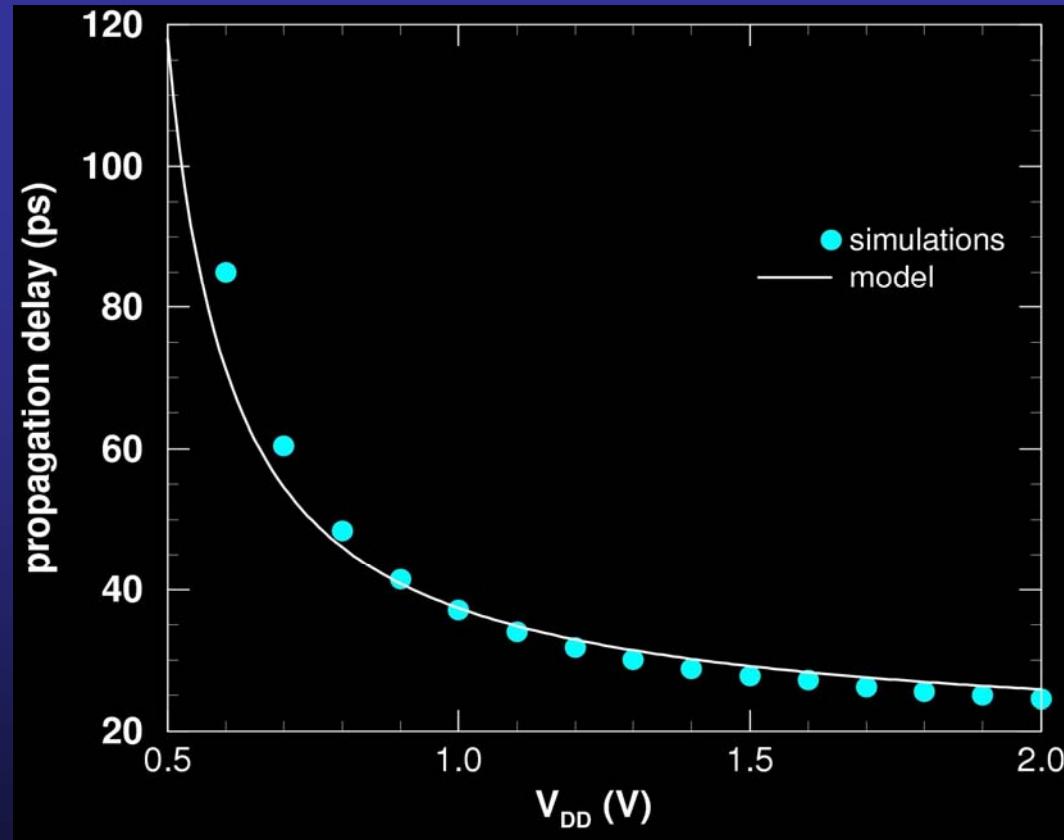
κ is a process-dependent parameter

$$\theta = \frac{1}{2} \left[1 + \frac{C_{ox} d}{\epsilon_{Si}} \left(1 + \left(\frac{\lambda \epsilon_{Si}}{C_{ox}} \right)^2 \right) \right]$$

Verification of Model

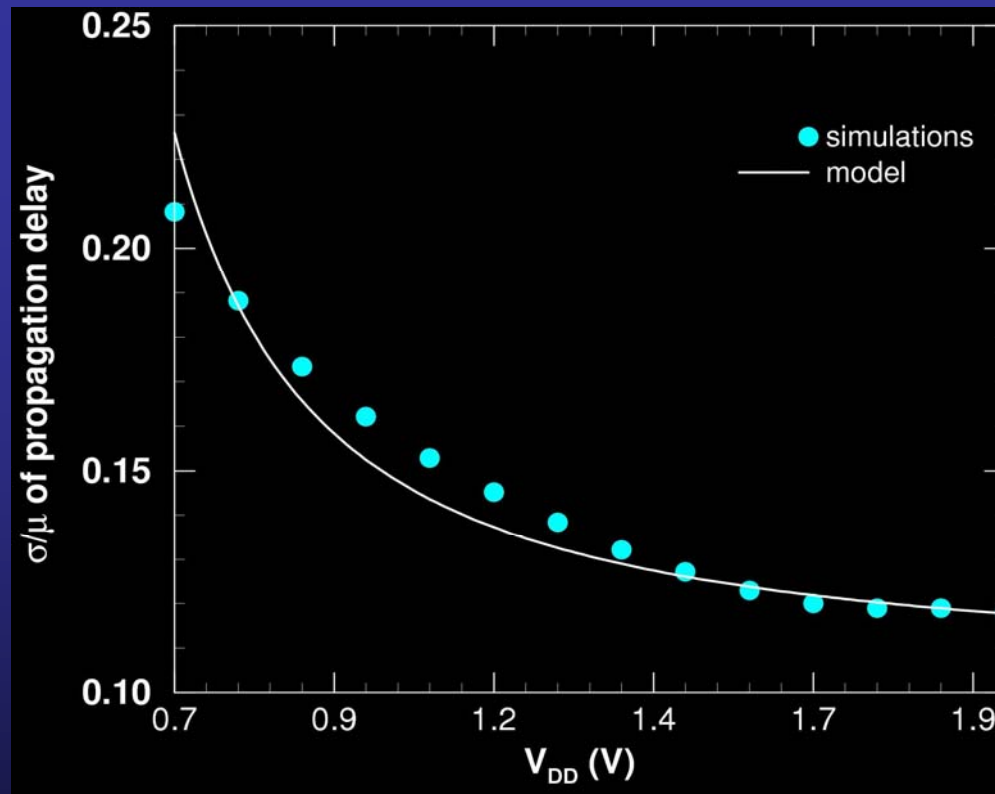
- 130nm technology with 70nm gate-length transistors
- K and α (Sakurai I-V model) extracted from I-V curves
- κ extracted from transient simulations

Propagation Delay



NAND3 gate with a step input

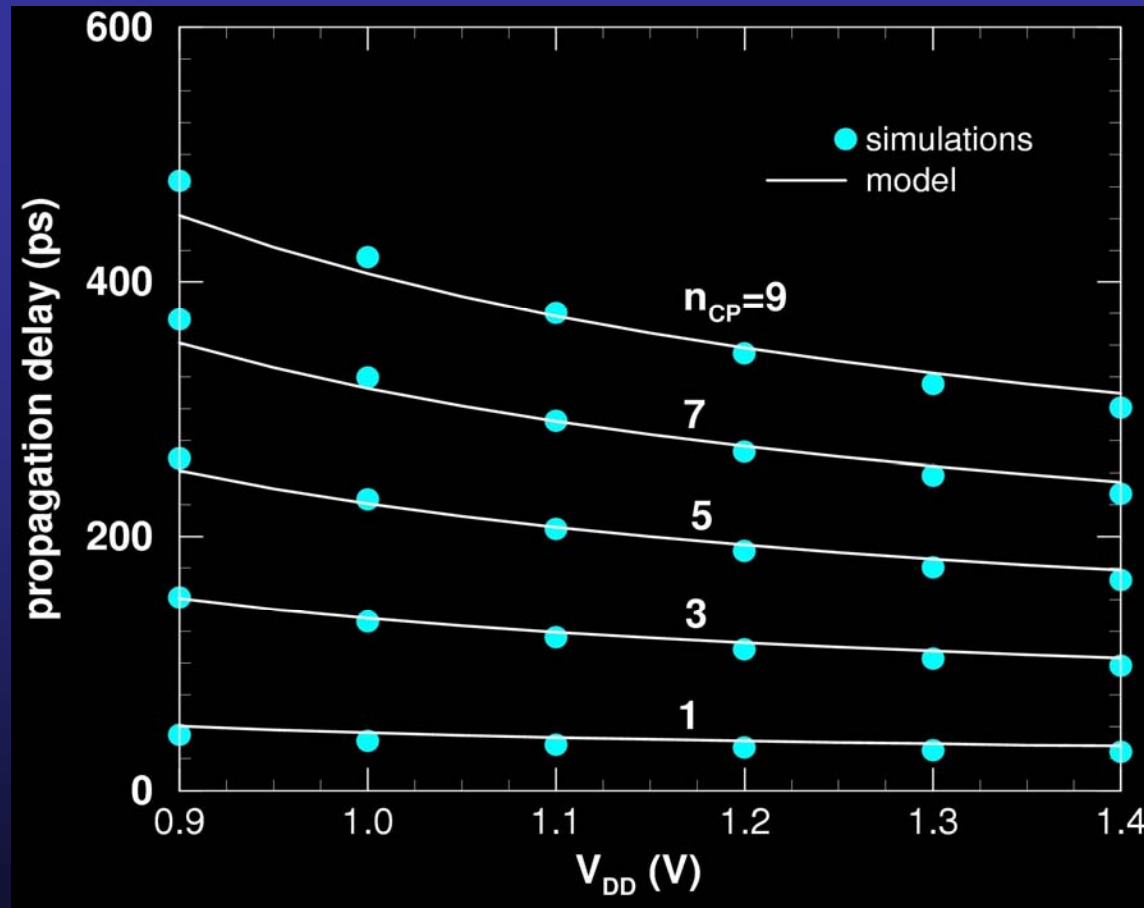
Delay Variation



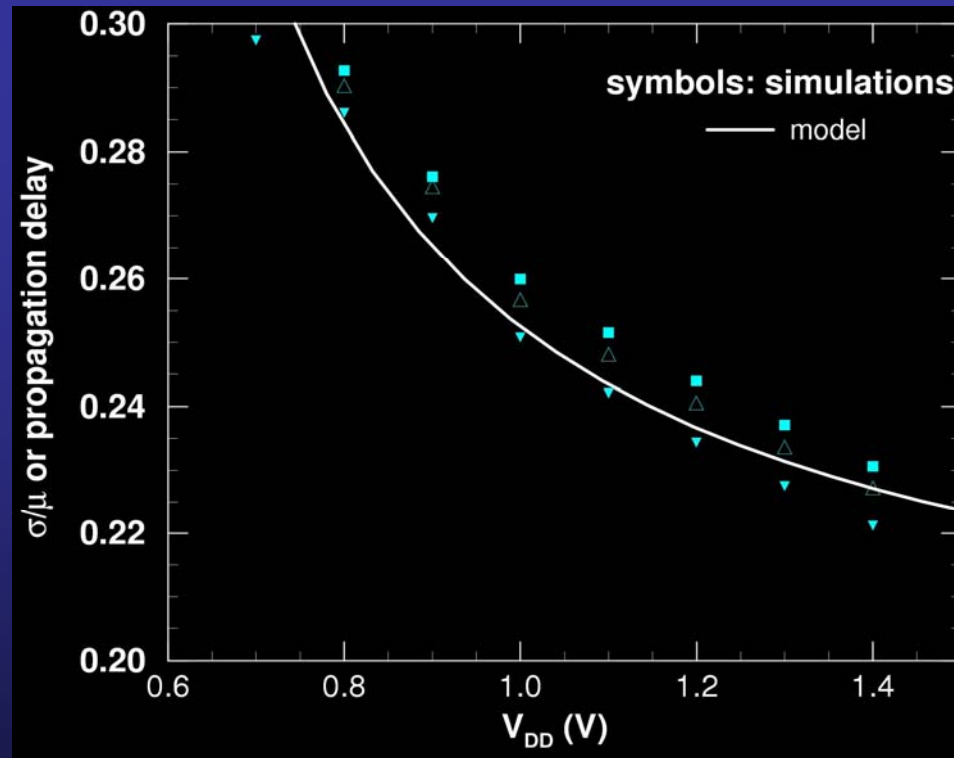
NAND3 gate with a step input

$\sigma_L = 20\%$ of L

Chain of NAND3 Gates



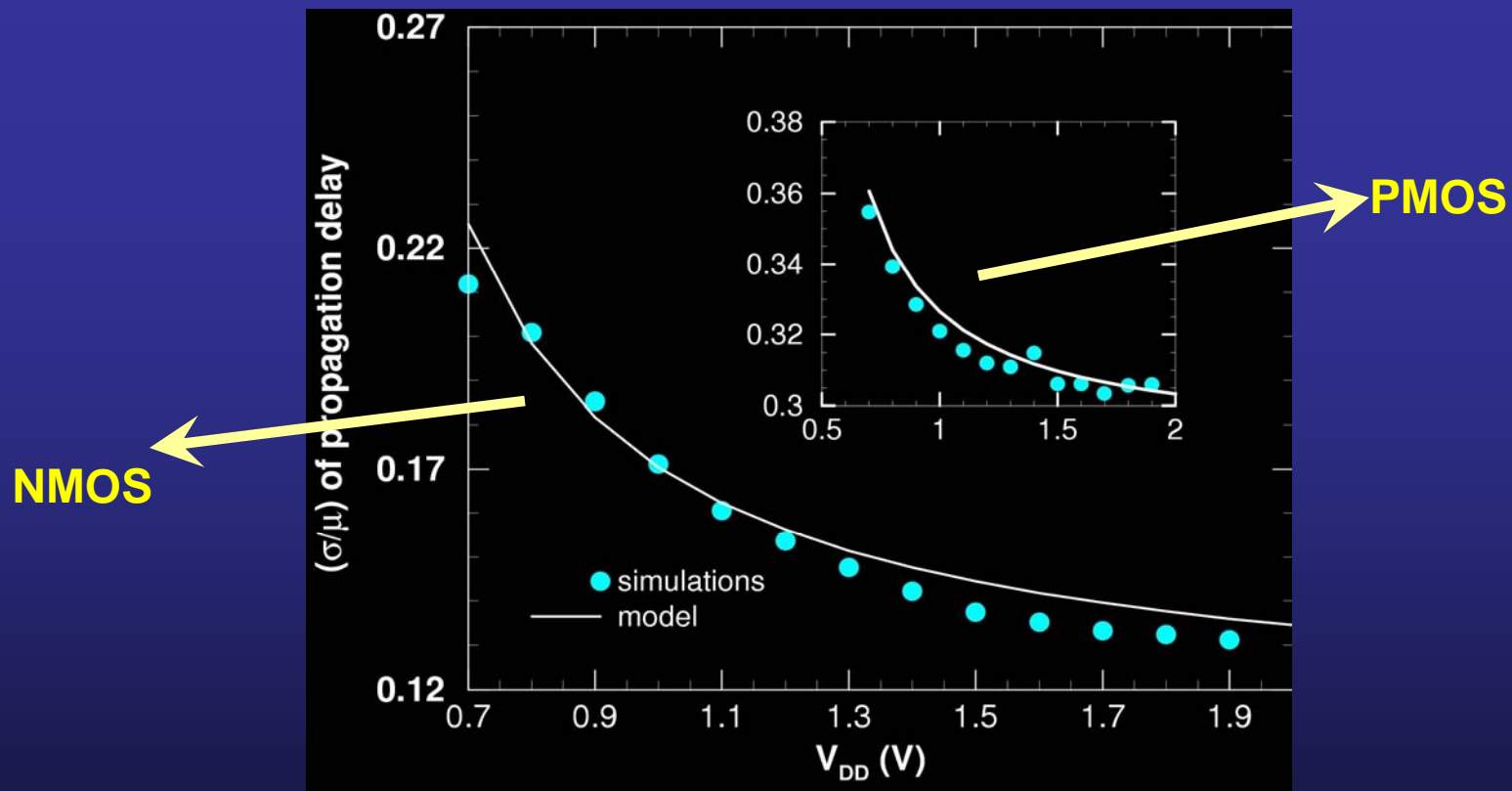
Delay Variation for Gate Chain



Chain of NAND3 gates

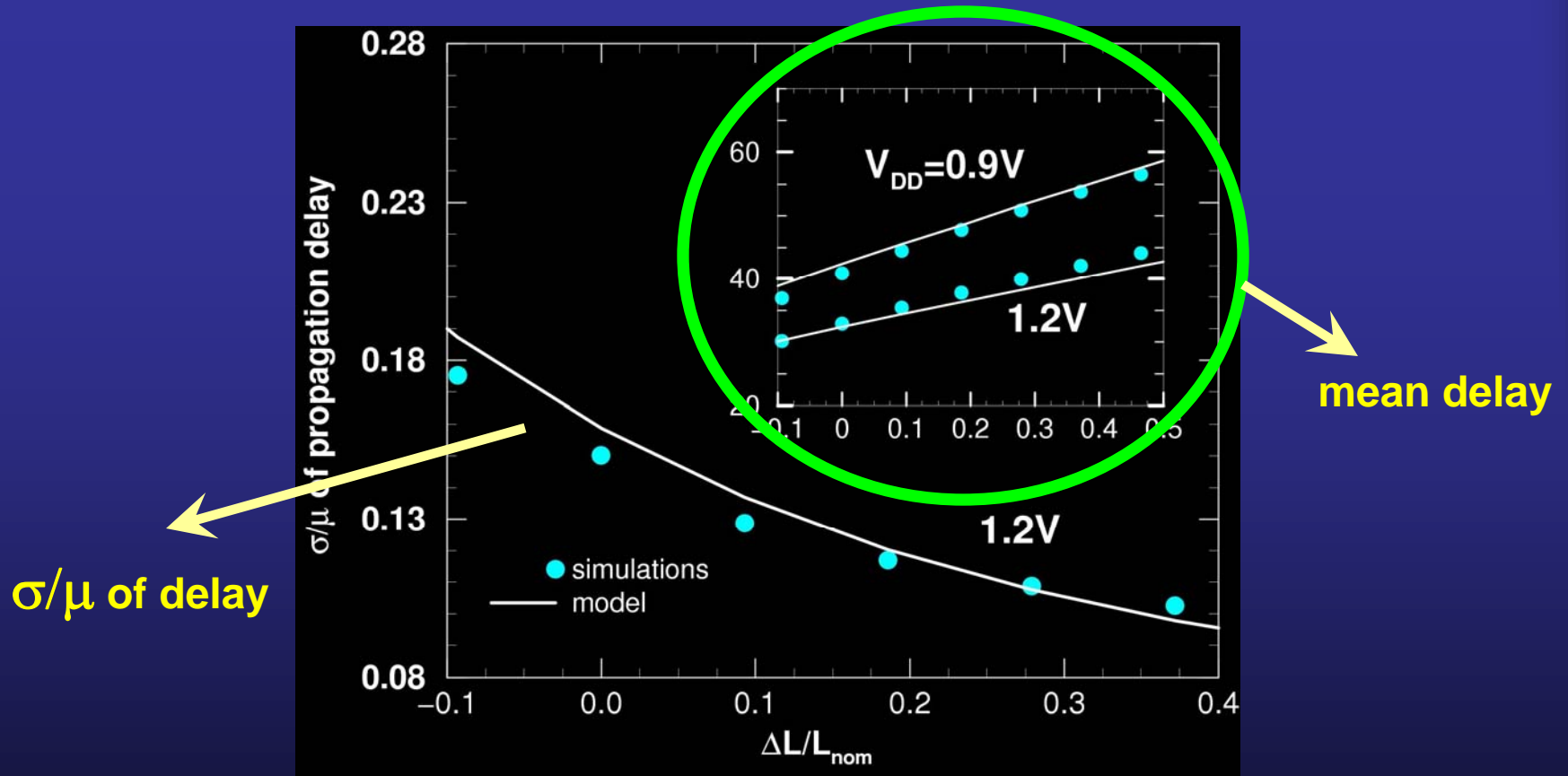
σ_L is higher than that for a single gate

PMOS vs NMOS Variation



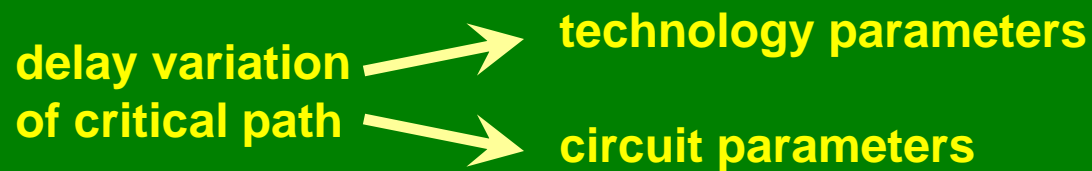
For this technology, PMOS devices have worse short-channel effect σ_L is higher for PMOS – gate shows worse variance for falling input

Gate Length Variation



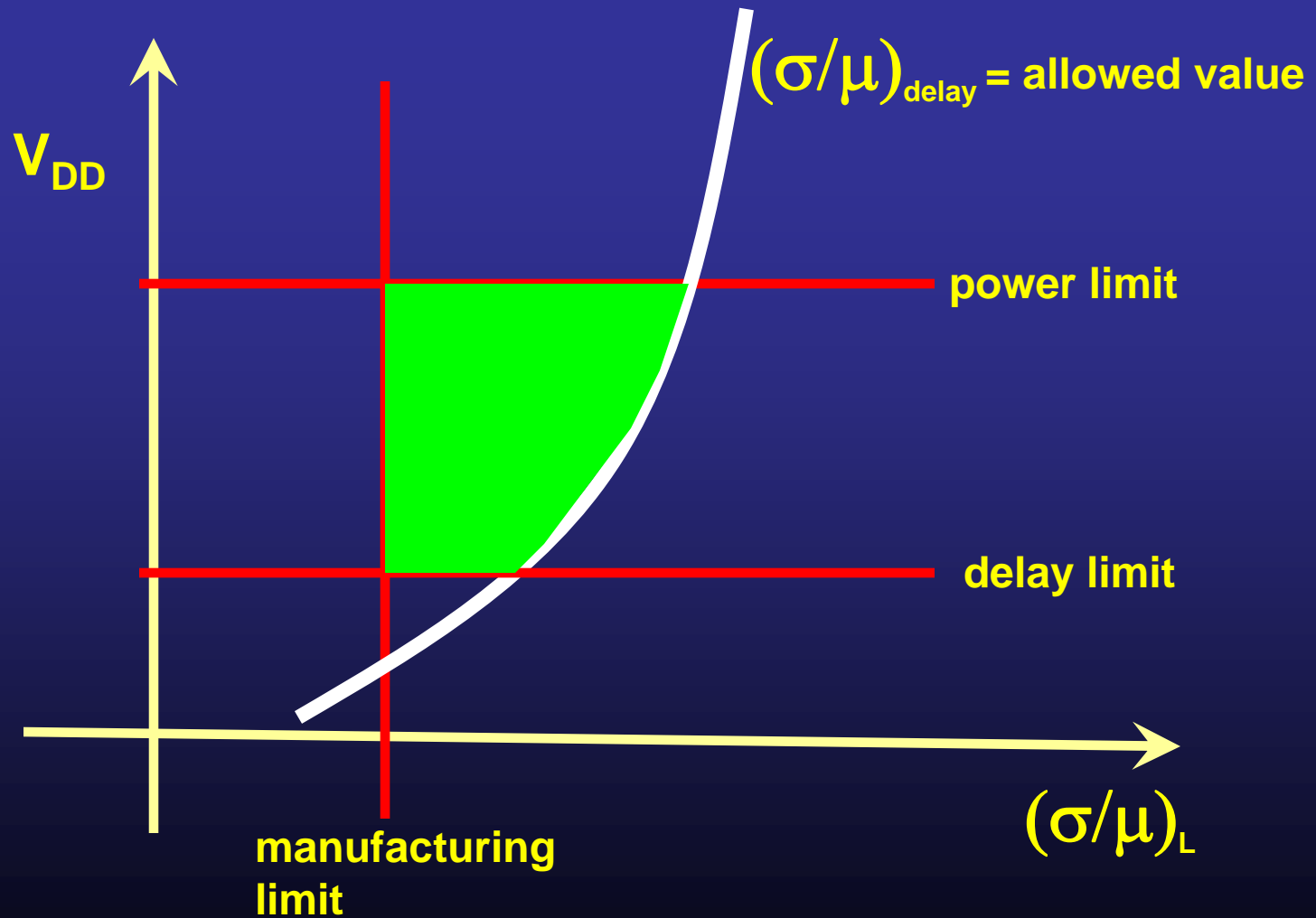
→ Gate-length variation is captured well by the model

Applications

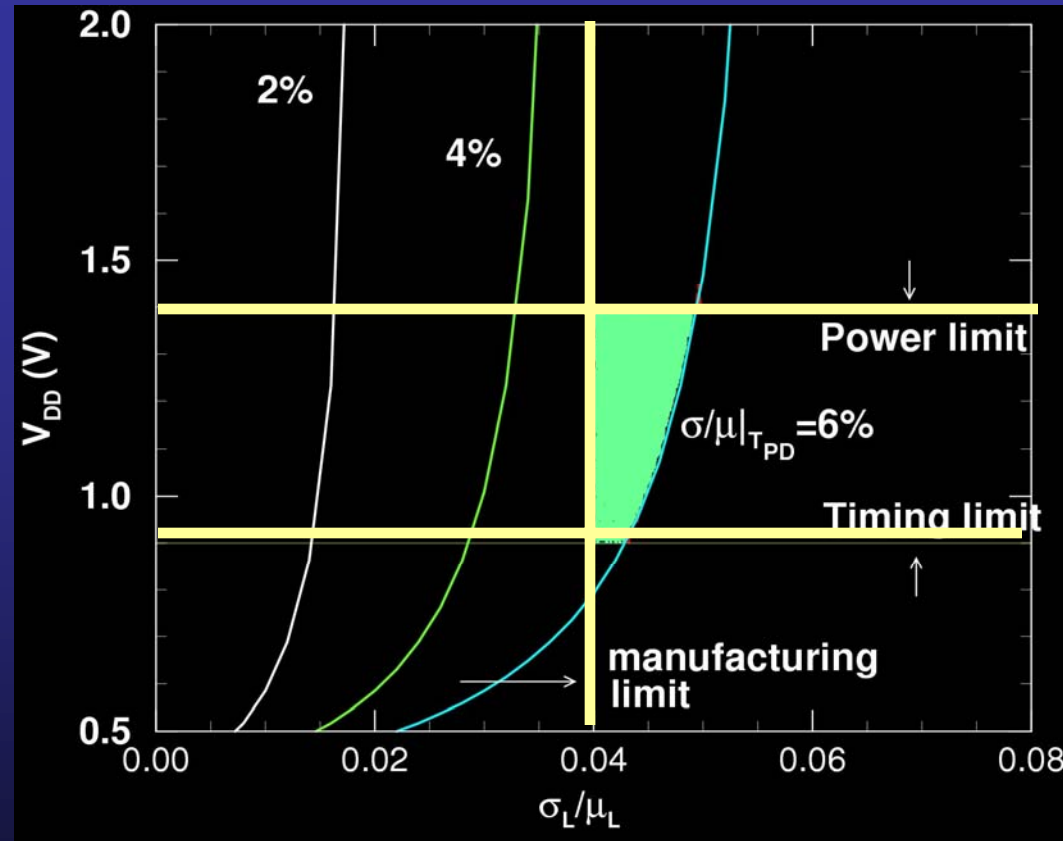


- D2D variations – sum of individual σ_{delay}
- un-correlated WID variations – RMS sum of individual σ_{delay}
- correlated WID variations – use correlation matrix to compute total σ_{delay}

Design Space

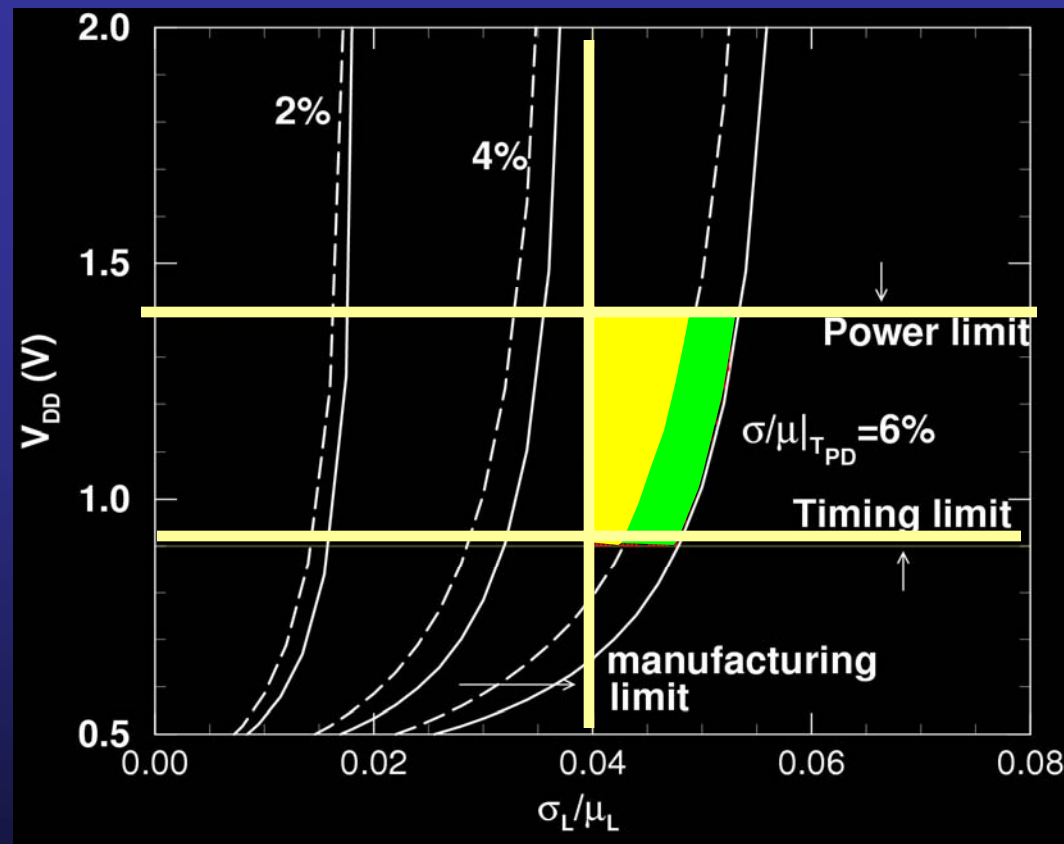


130nm Technology Design Space



→ Depending on power and timing limits, a small design-window exists

Design Space with Gate-length Bias



→ by adding a 10nm gate-length bias, design window is expanded

Conclusions

- Compact model verifies well with simulations – mean delay, delay variance, and gate-length effect on delay
- WID, D2D and correlated variations can be handled
- Design-space allows for early circuit-design and circuit/technology optimization