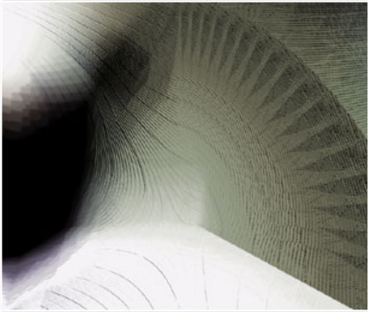
Modeling of

Multi-Fin MOSFET Parasitic Effects



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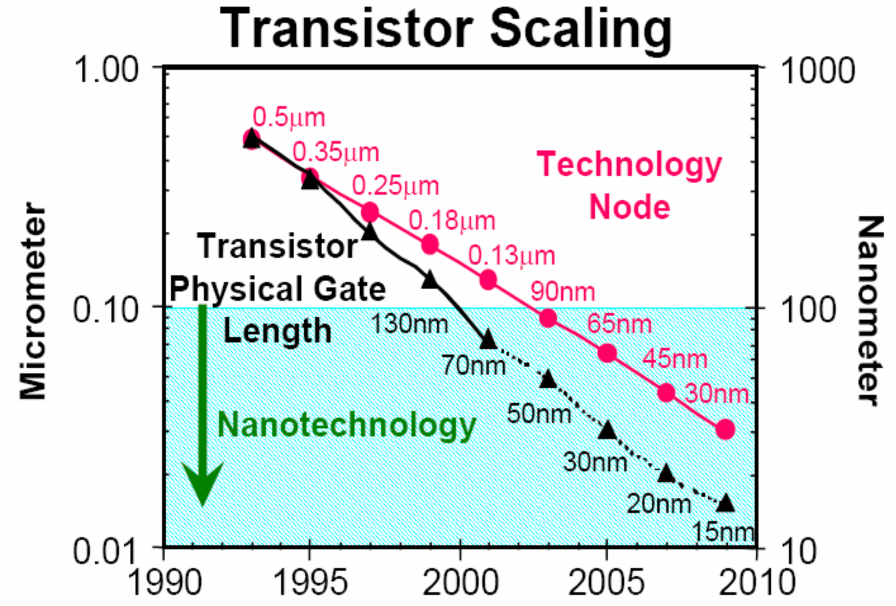
Acknowledgement

- The work is supported by a grant from the Research Grant Council of Hong Kong and a grant from the 2006 New Energy and Industrial Technology Development Organization (NEDO) International Joint Research Program

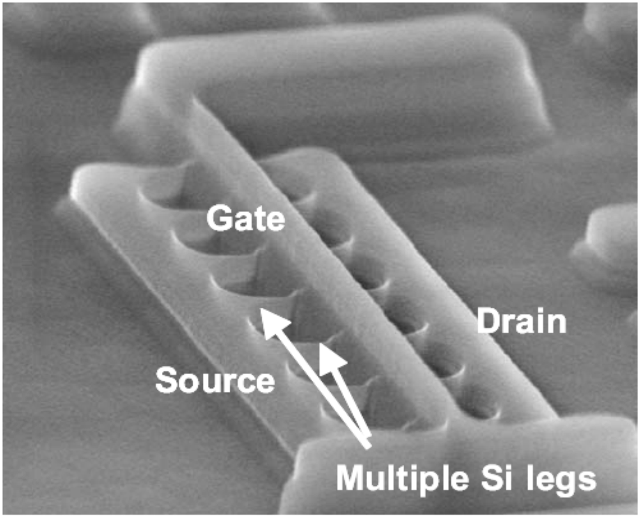
- The contribution from the following researchers
  - Wen WU
  - Wai-Kit LEE
  - Prof. Jin HE of Peking University

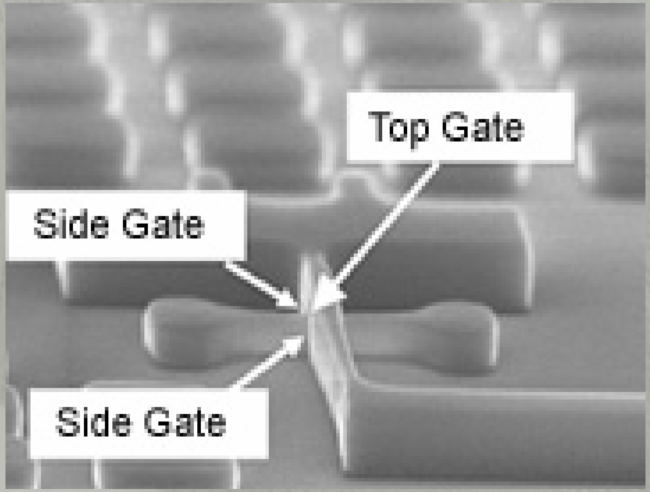
The Multi-Fin Technology

The Scaling Trend



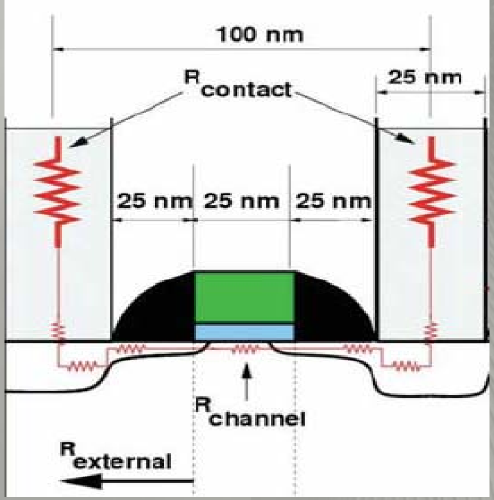
Source: Intel





- It is time to study the performance of non-traditional devices for future scaling

Device Performance

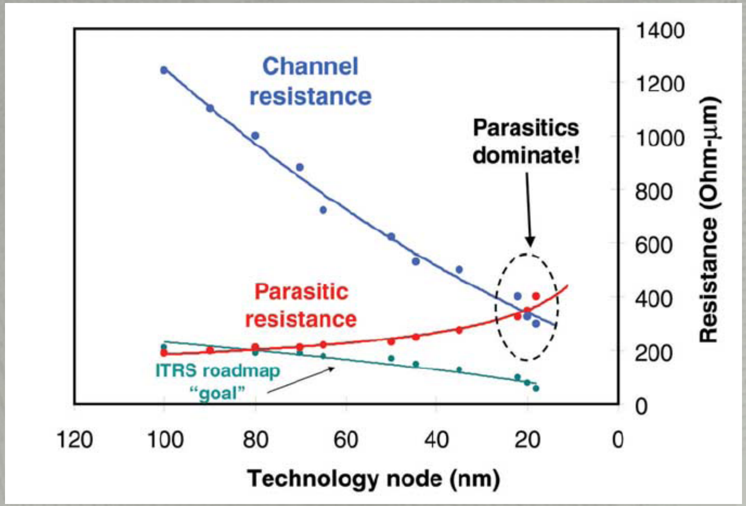


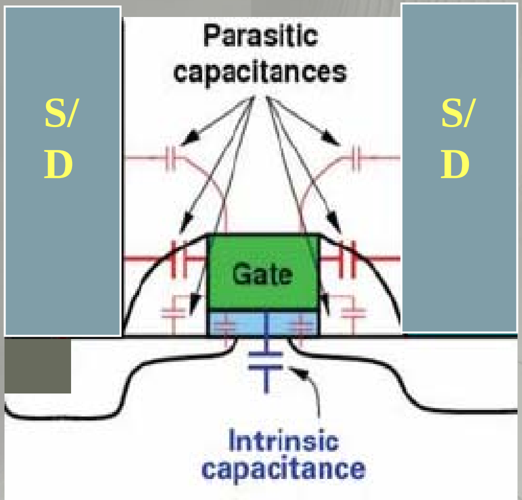
Intrinsic Resistance

- o Channel resistance

Extrinsic Resistance

- o Contact resistance
- o S/D Series resistance
- o Gate resistance



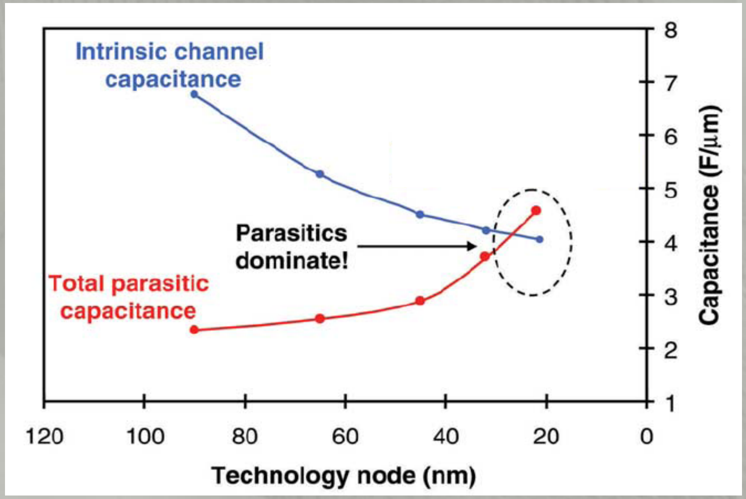


Intrinsic Capacitance

- o Gate capacitance

Extrinsic Capacitance

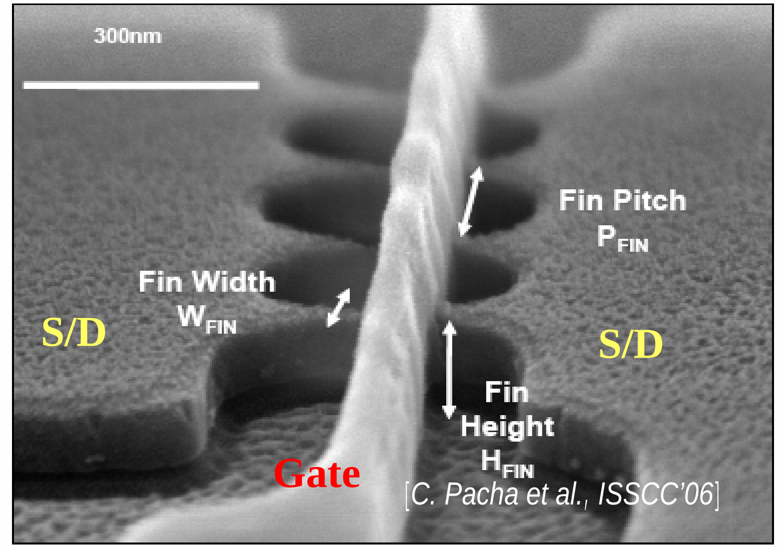
- o Junction capacitance
- o fringing capacitance
- o overlap capacitance



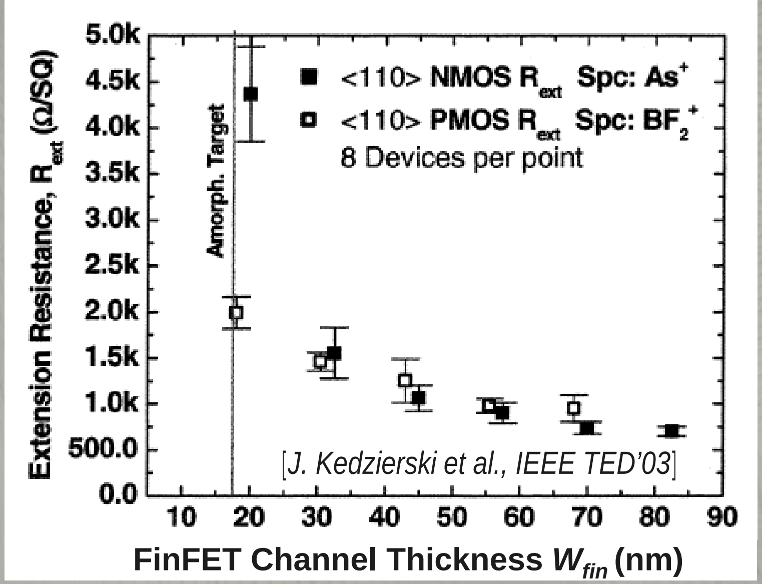
[S. E. Thompson *et al.*, *Materials Today'06*]

Nature of Parasitics

Strongly geometry dependent



[C. Pacha et al., ISSCC'06]

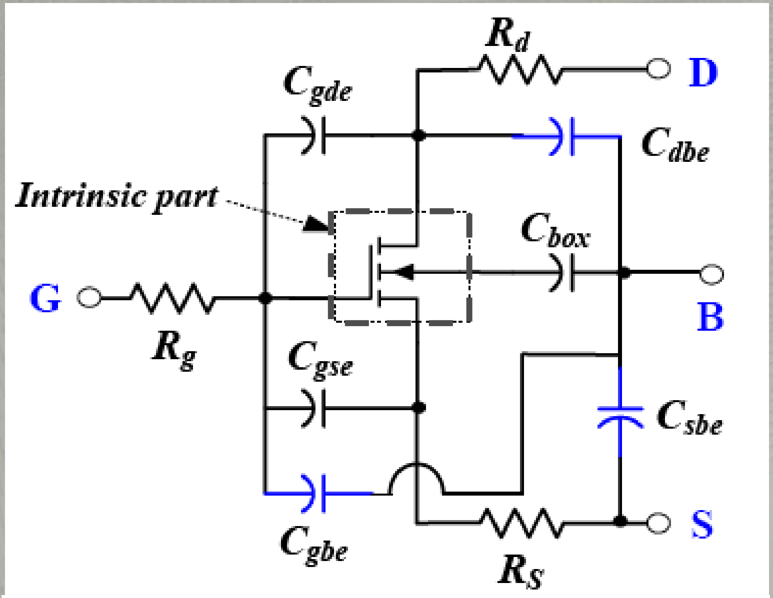


[J. Kedzierski et al., IEEE TED'03]

- Require a lot of structural related parameters such as H_{Fin}, W_{fin}, P_{Fin}, L_{ext} etc.
- Challenge: some of these parameters should be supplied by the layout extractor

Modeling Approach

- The parasitic components are added to an independently from the intrinsic model
- The model is supposed to work with different intrinsic models (surface potential, charge based, carrier based etc.)



Non-planar multi-gate SOI Model
((*G*, *D*, *S*, *B*) four-terminal model: separate gate devices are not considered)

- Based on distributed network and s-parameters

Impedance Matrix

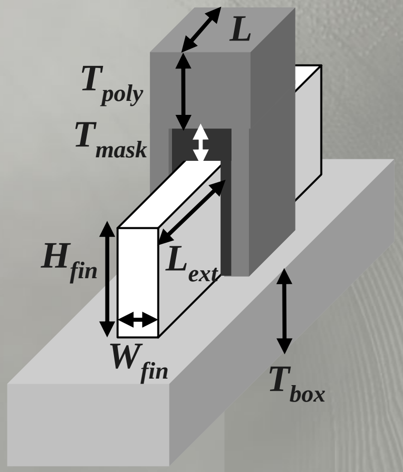
$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \Rightarrow \begin{cases} \mathrm{Re}(Z_{11}) = R_g + R_s \\ \mathrm{Re}(Z_{12}) = \mathrm{Re}(Z_{21}) = R_s \\ \mathrm{Re}(Z_{22}) = R_d + R_s \end{cases}$$

DC: R_d, and R_s
RF: R_g, R_d, and R_s

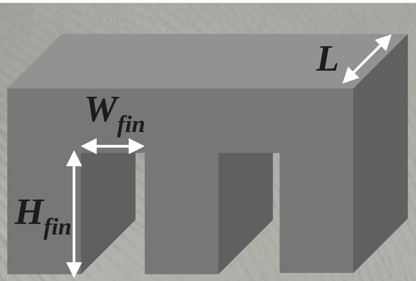
Outline

- Gate Resistance Model
- Fringing Capacitance Model
- Overlap Capacitance Model
- Verification of the Models
- Extensions and Summary

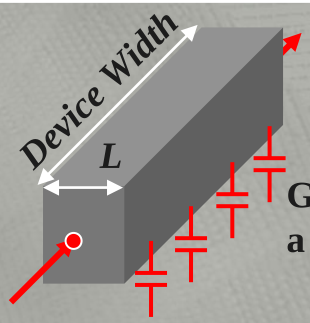
Gate Resistance Modeling (1)



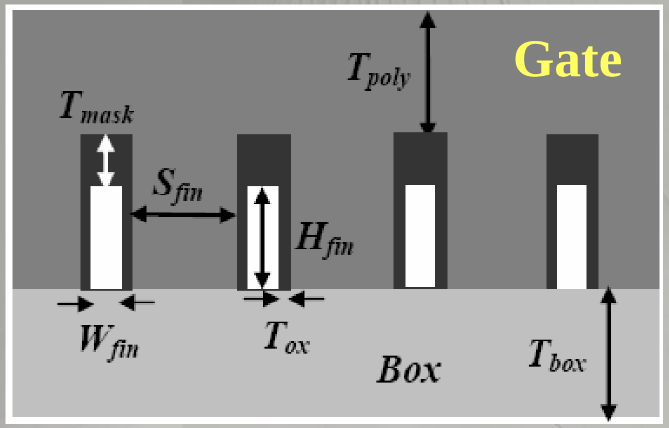
3-D nature: Complicated Resistances & Capacitances



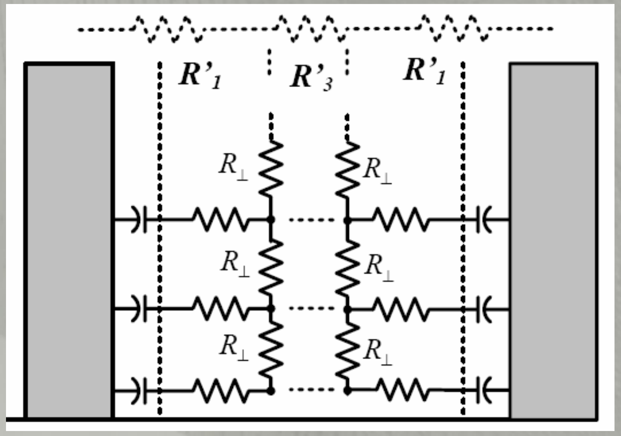
Gate Geometry of a 2-fin FinFET



Gate Geometry of a bulk MOSFET

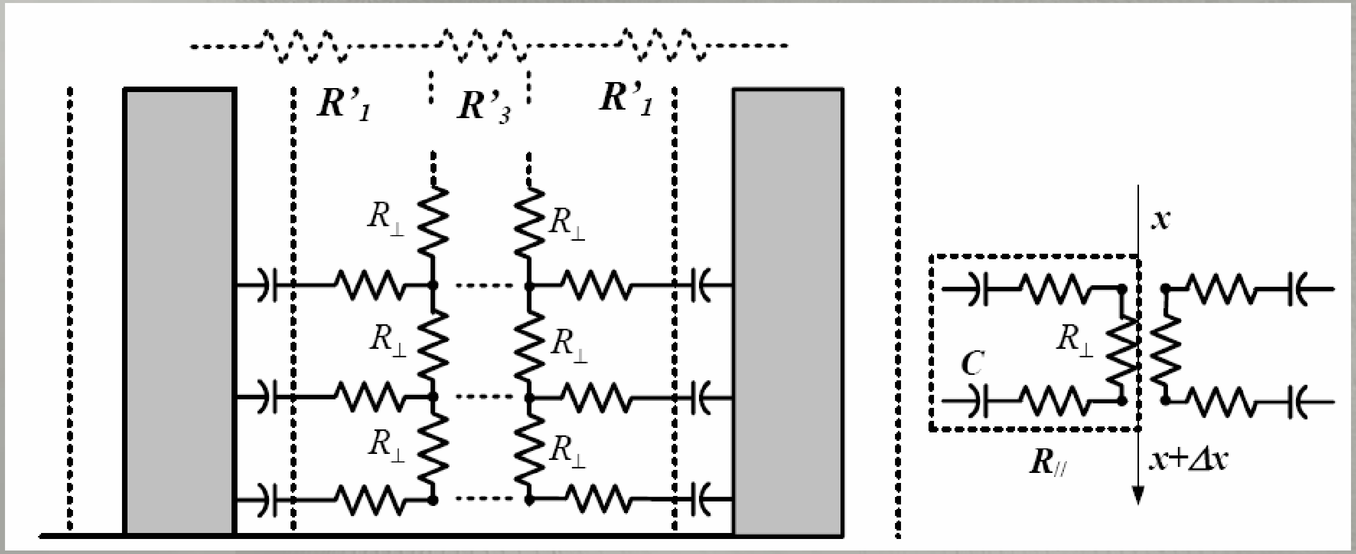


Cross section of a four-fin DG MOSFETs



Equivalent Resistance Network

Gate Resistance Modeling (2)



$$R_{//} = \frac{\rho S_{fin}}{2\Delta x}$$

$$R_{\perp} = \frac{2\rho \Delta x}{S_{fin}}$$

$$C = \frac{C_g}{H_{fin}}\Delta x = C_{OX}\Delta x$$

$$I_D \approx g_m \frac{V_{in}(s)}{1+\left(sC_{OX}H_{fin}\right)\left(\frac{2\rho H_{fin}}{3S_{fin}}\right)} = \frac{g_m V_{in}(s)}{1+\left(sC_g\right)R_C}$$

$$R_C = \frac{2\rho H_{fin}}{3S_{fin}}$$

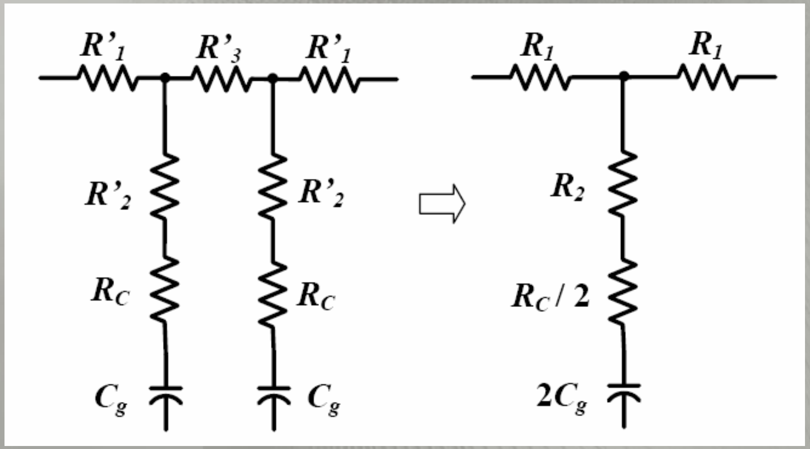
Assumption: thick buried oxide; no gate inductive components

$$-\frac{\partial I(x,s)}{\partial x} = \frac{sC_{OX}}{1+\rho S_{fin} sC_{OX} / 2} V(x,s)$$

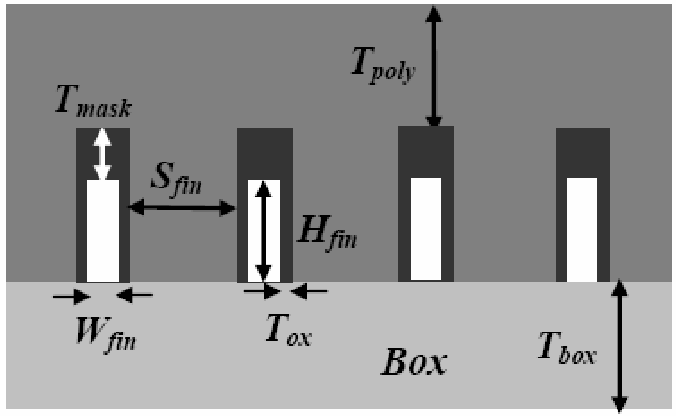
$$-\frac{\partial V(x,s)}{\partial x} = \frac{2\rho}{S_{fin}} I(x,s)$$

$$\begin{cases} v(x=0, s) = V_{in}(s) \\ i(x=H_{fin}, s) = 0 \end{cases}$$

Gate Resistance Modeling (3)



from π-network to *T*-network



$$R_1 = k_1\left(S_{fin} + 2T_{OX} + W_{fin}\right)/T_{poly}$$

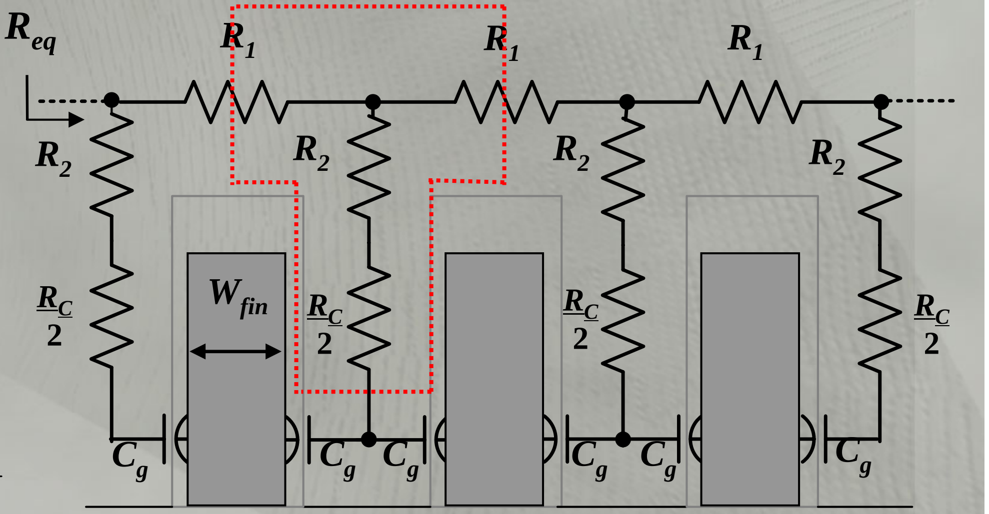
$$R_2 = k_2\left(T_{poly}/2 + T_{mask}\right)/S_{fin}$$

$$R_{eq,n} = \frac{(n-1)(R_2 + R_C/2)}{2n^2} + \frac{(n+1)(2n+1)R_1}{6n} + R_{eq,1}$$

$$C_{eq,n} = 2nC_g$$

⇩

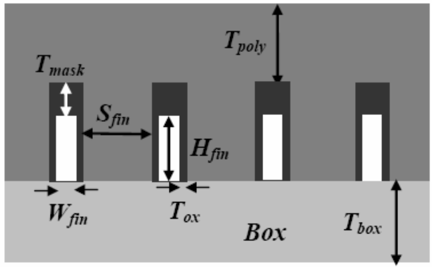
$$S_{finopt} = \sqrt{\frac{3(n-1)T_{poly}\left(k_2 T_{poly}/2 + k_2 T_{mask} + \rho H_{fin}/3\right)}{n(n+1)(2n+1)k_1}}$$



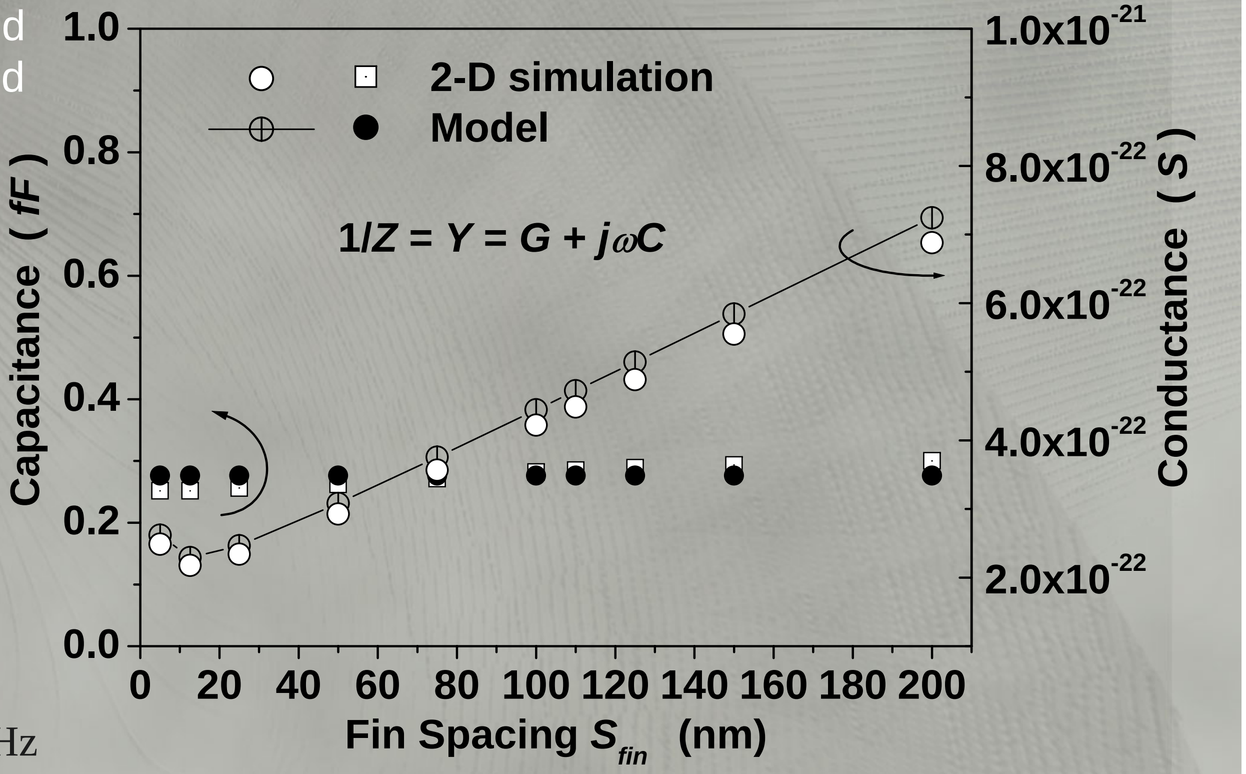
A RC network to model gate resistance

Gate Resistance Modeling (4)

Comparison of capacitances and conductances between modelled data and *2-D* AC small-signal simulation results.



W_{fin} = 20 nm; H_{fin} = 80 nm
T_{OX} = 2 nm; L = 50 nm;
T_{mask} = 10 nm
The frequency (ω/2π) is 1000 Hz



$$Y = G + j\omega C = \frac{1}{R_{eq,n} + \frac{1}{j\omega C_{eq,n}}}$$

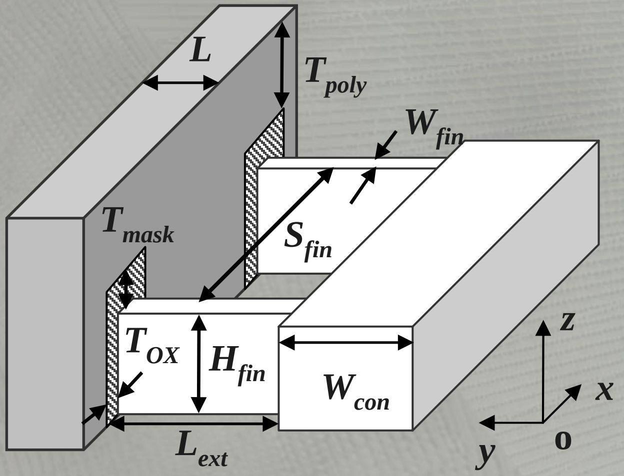
⇨

$$\omega = 2\pi f \quad ; \quad C = C_{eq,n}$$

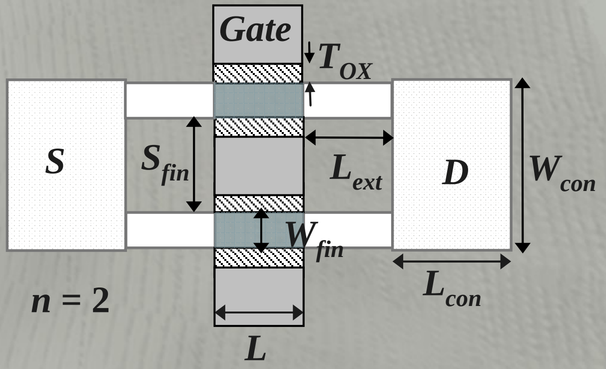
$$G = \omega^2 C_{eq,n}{}^2 R_{eq,n}$$

Parasitic Capacitance

- Consists of overlap (C_{ov}) and fringing (C_{fr}) capacitance
- Fringing capacitance can be further decomposed into outer fringing (C_{of}) and inner fringing (C_{if}) capacitance
- C_{if} capacitance is relative small in accumulation and strong inversion
- As a MOSFET always operate at strong inversion at high frequency, C_{if} is ignored

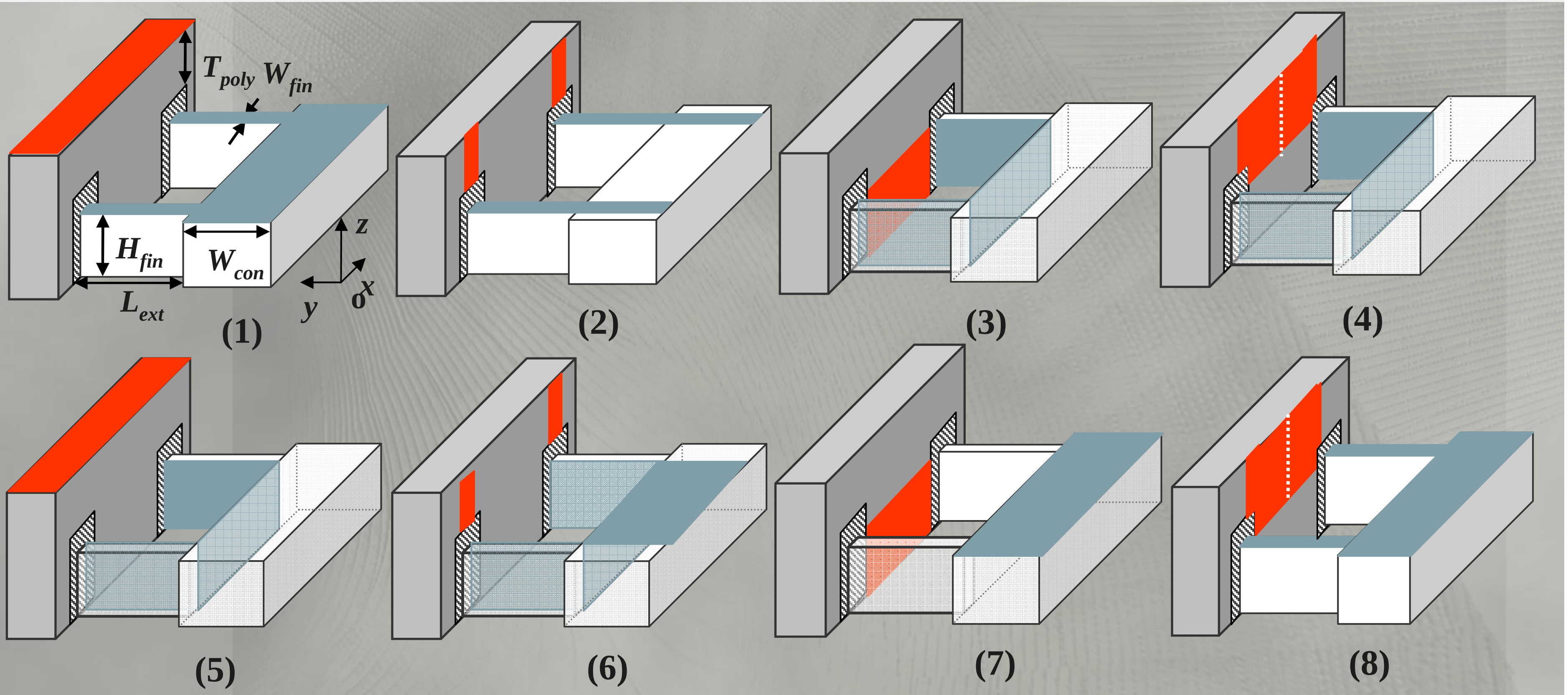


Three dimensional diagram of a two-fin double-gate MOSFET



The top view of the 2-fin double-gate MOSFET

Fringing Components



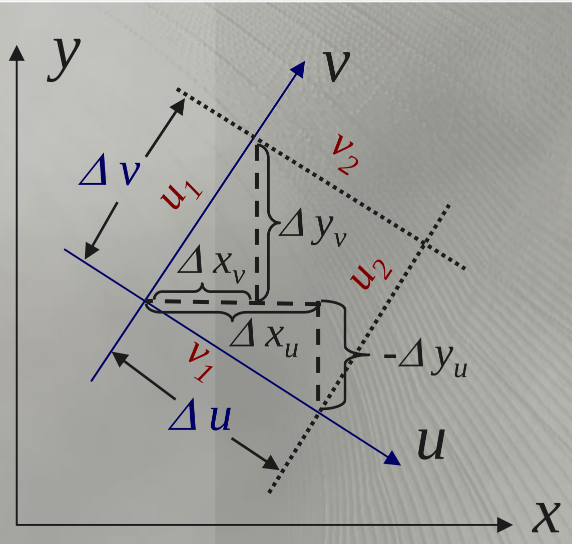
Red: Anode *Blue: Cathode*

- From 3-D simulation, (1),(2), (3) contribute more than 99% of the capacitive components and (3) alone contribute around 80-98% depends on geometry

Formulation

Conformal mapping

- Deal with orthogonal field lines (potential and flux)
- A configuration in the complex *z*-plane
- Map it into a simpler and more readily analyzable configuration in the complex *w*-plane by a function *f* (*z*)
- “Conformal”: all properties are preserved at microscopic level during transformation



$$\frac{\Delta u}{\Delta x_u} = \frac{\Delta v}{\Delta y_v} \qquad \frac{\Delta v}{\Delta x_v} = -\frac{\Delta u}{\Delta y_u}$$

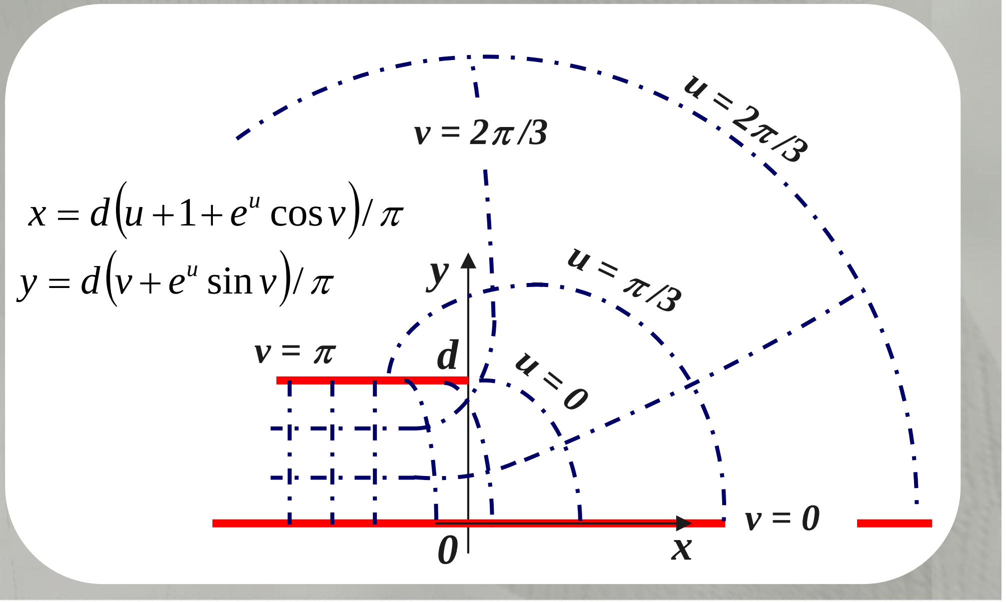
$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} = \frac{\partial^2 x}{\partial u^2} + \frac{\partial^2 x}{\partial v^2} = \frac{\partial^2 y}{\partial u^2} + \frac{\partial^2 y}{\partial v^2} = 0$$

$$z = x + iy \qquad w = u + iv$$

$$\Downarrow$$

$$w = f(z)$$

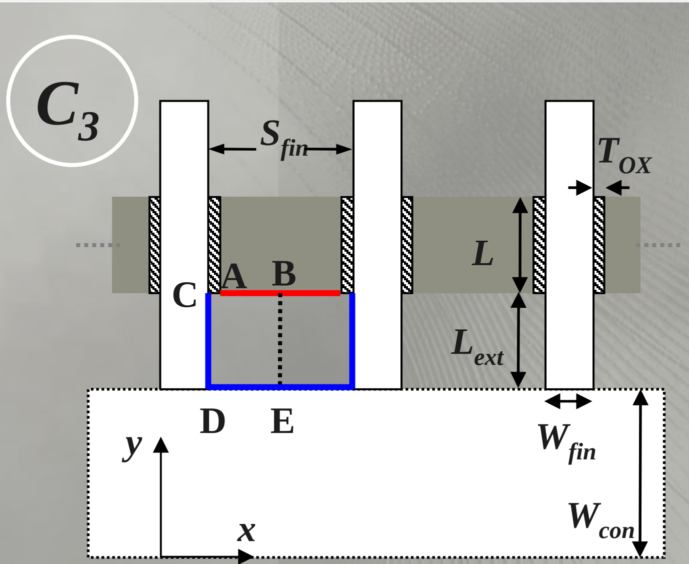
The form of f (z) depends on the specific boundaries

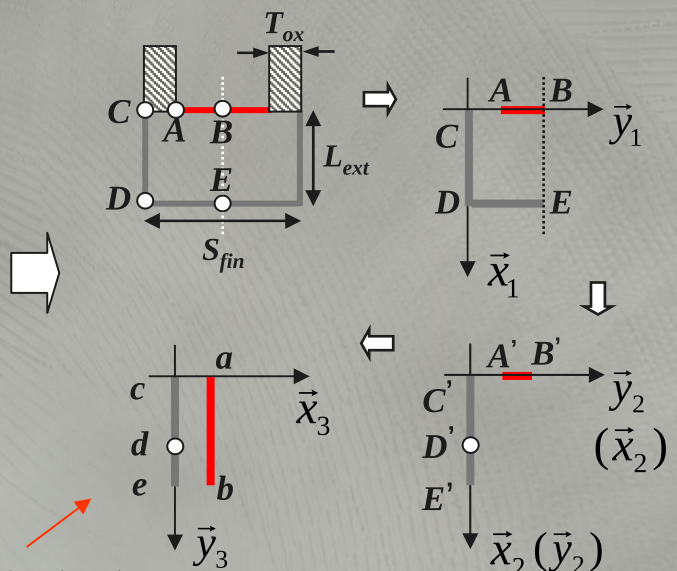


$$x = d\left(u + 1 + e^u \cos v\right)/\pi$$

$$y = d\left(v + e^u \sin v\right)/\pi$$

Fringing Capacitance Model (1)



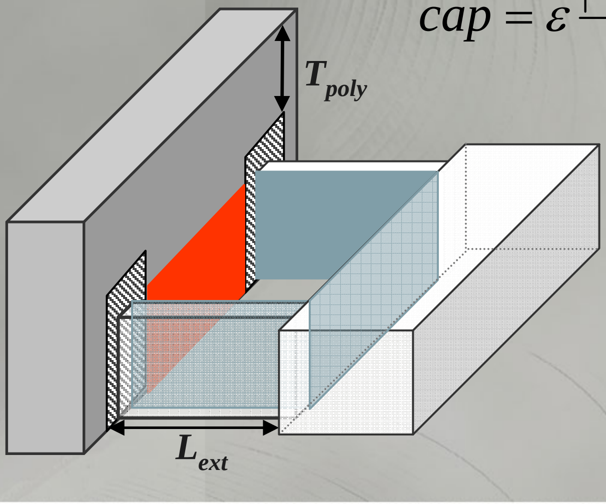


(x_1-y_1) -> (x_2-y_2)
(x_2-y_2) -> (x_3-y_3)

Transformation function

$$w = f(z)$$

$$cap = \varepsilon \frac{|cd| + |de|}{|ac|}$$

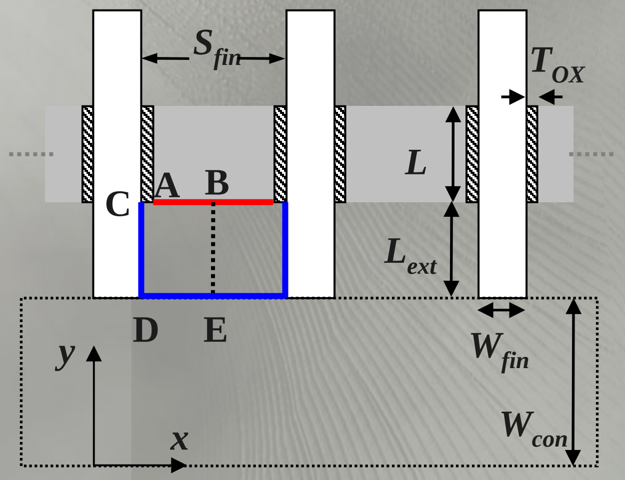


$$nx\vec{X} + y\vec{Y} = k_1 \sin\left(u\vec{U} + v\vec{V}\right)$$

$$nx + iy = k_2 \sin(u)\cosh(v) + ik_2 \cos(u)\sinh(v)$$

Fringing Capacitance Model (2)

C_3

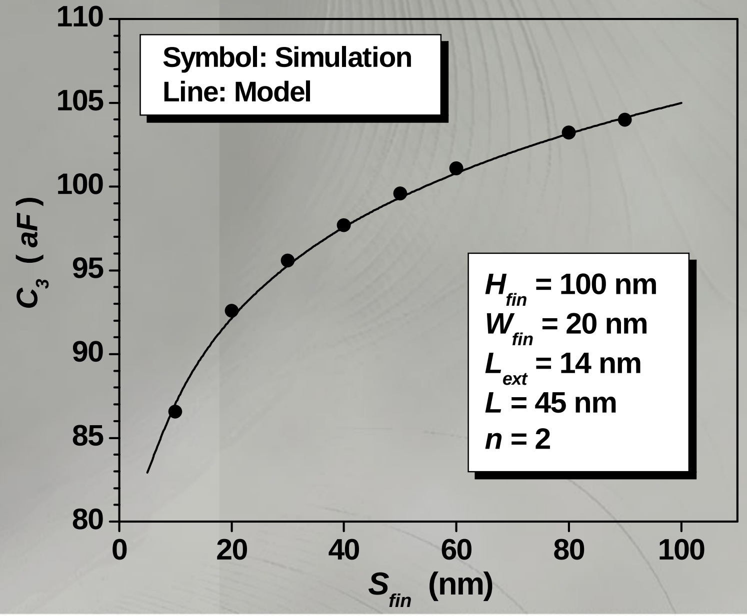


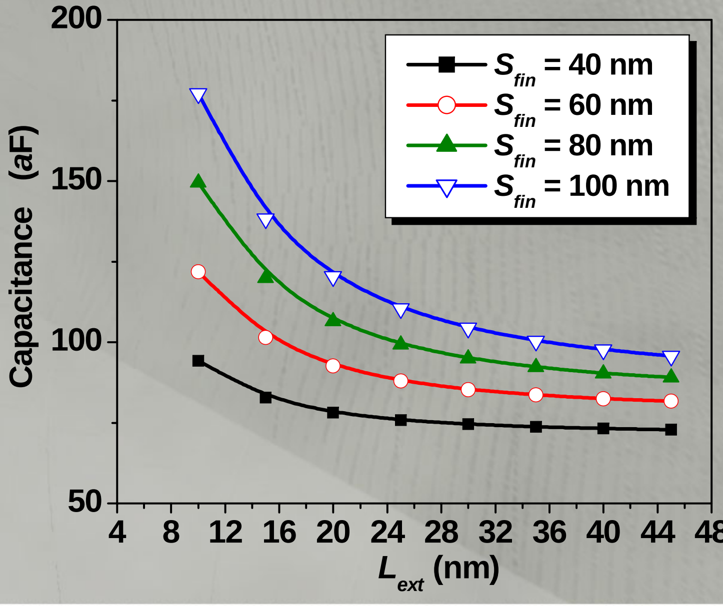
$$C_{unit} = \varepsilon \frac{|cd|+|de|}{|ac|} = \frac{2\varepsilon}{\pi}\sinh^{-1}\left(\sqrt{\frac{\sinh^{2}\left(\frac{\pi}{2}\cdot\frac{|BC|}{|DC|}\right)}{\sinh^{2}\left(\frac{\pi}{2}\cdot\frac{|AC|}{|DC|}\right)}-1}\right)$$

⇩

$$C_3 = (C_{unit} + C_{fitting})\cdot H_{fin}$$

account for corner effects ~ 11aF/µm

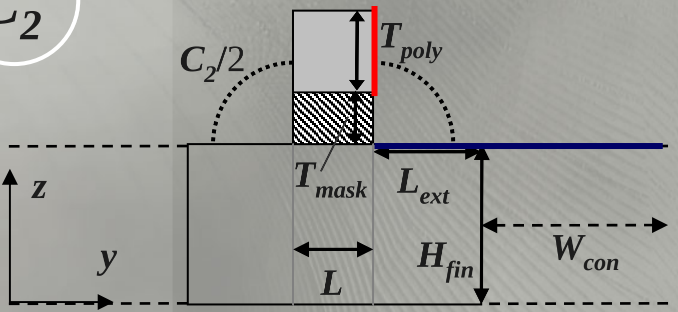




n = 2
H_{fin}=100nm
W_{fin}=20nm

Fringing Capacitance Model (3)

C_2



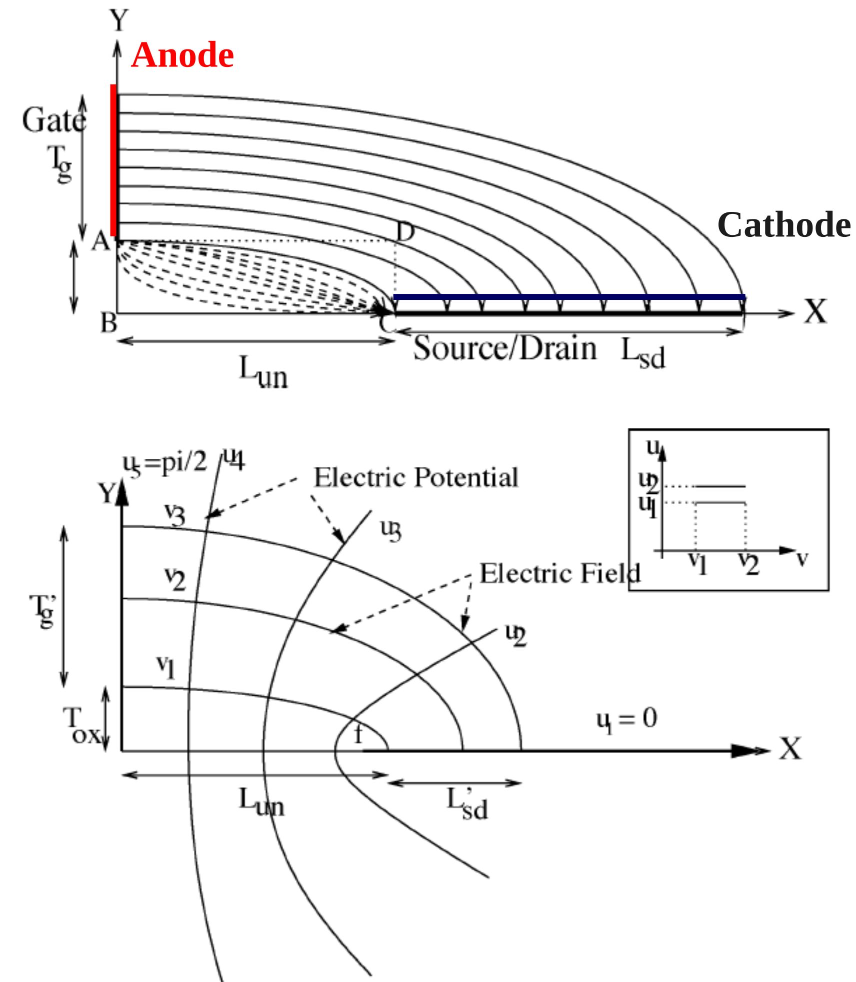
$$L_{un} = 0 \;\; \& \;\; L_{sd} = L_{ext} + W_{con}$$

$$C_2 = \frac{2\varepsilon_{OX} W_{C2}}{\pi} \ln\left(\frac{T_{mask} + \eta_1 T_{poly} + \sqrt{(\eta_1 T_{poly})^2 + 2T_{mask}\eta_1 T_{poly}}}{T_{mask}} \right)$$

$$+ \frac{\eta_2 e^{-1} \varepsilon_{OX} W_{C2}}{\pi} \ln\left(\frac{\pi W_{C2}}{T_{mask}} \right)$$

$$\eta_1 = \exp\left(\frac{L_{sd} - \sqrt{T_{poly}^{\;2} + 2T_{mask}T_{poly}}}{\tau_1 L_{sd}} \right)$$

η_1 is geometry-dependent parameter;
η_2 and τ_1 are geometry-independent

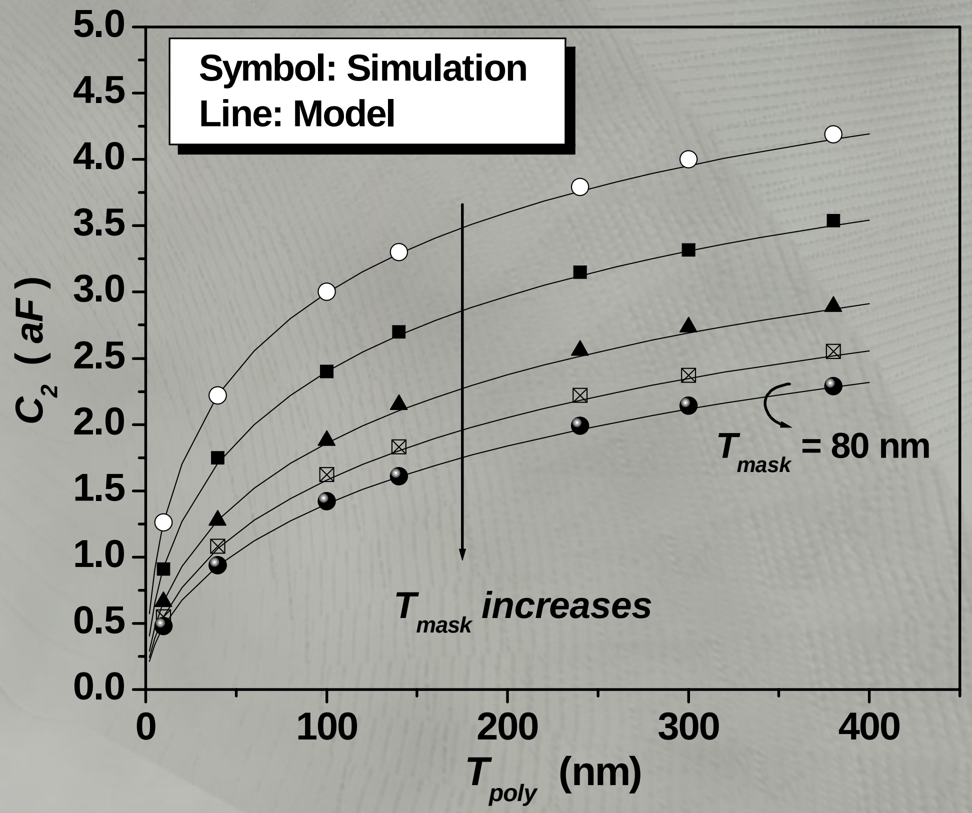


A. Bansal et al., *IEEE TED*, pp. 256, Feb. 2005

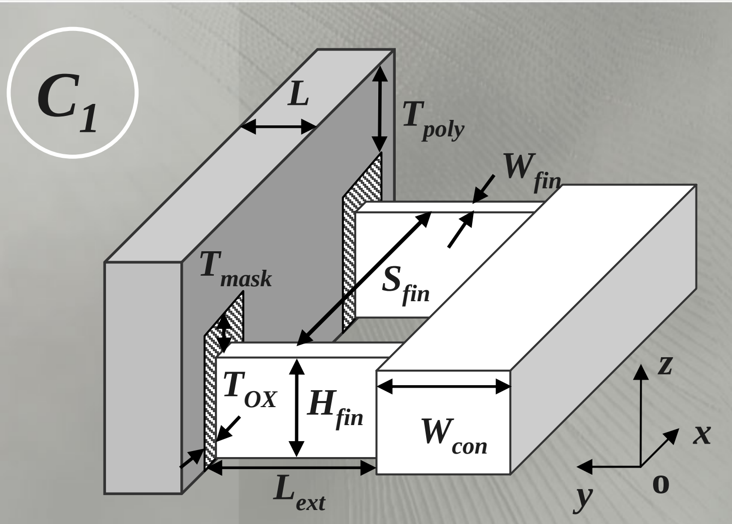
Fringing Capacitance Model (4)

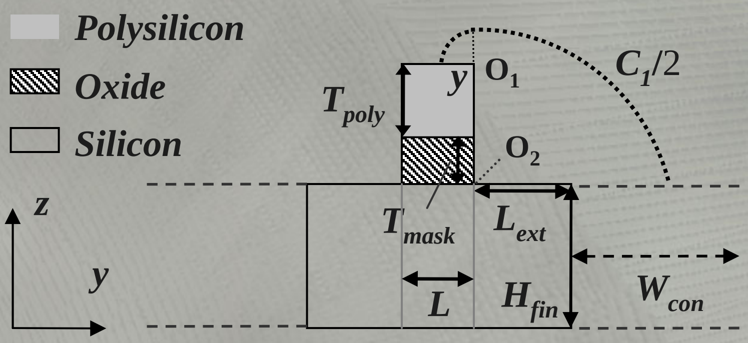
C_2

Model verification by numerical simulator



Fringing Capacitance Model (5)





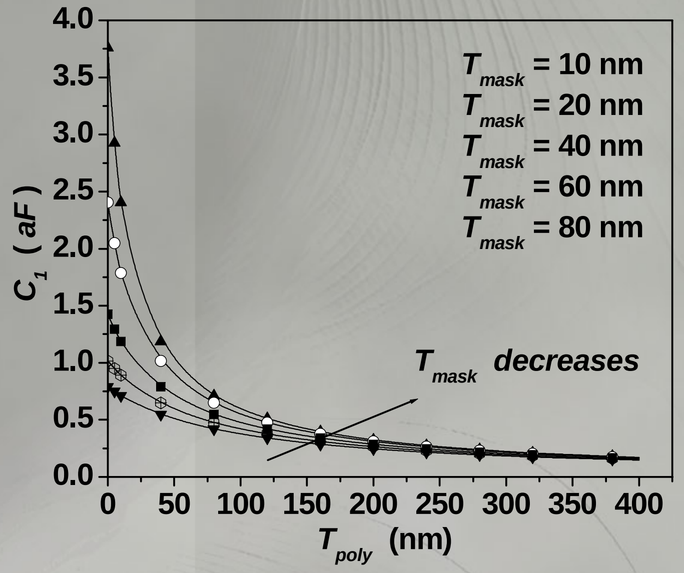
- Assume $(T_{mask}+T_{poly}) >> L_{ext}$ and W_{con} is quasi-infinite
- The length of electric field is given by

$$\frac{2\pi y}{4}+\frac{2\pi\left(y+T_{poly}+T_{mask}\right)}{4}$$

- Therefore

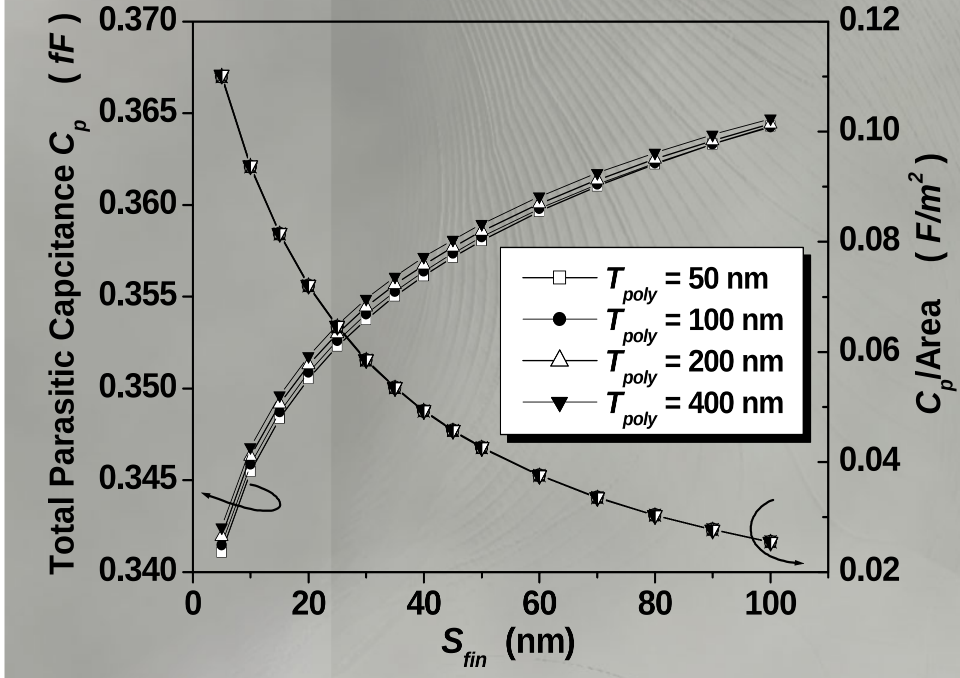
$$C_1 = 2n\left(W_{fin}+S_{fin}\right)\int_0^{L/2}\frac{\varepsilon_{OX}\,dy}{\left\{2\pi y+2\pi\left(y+T_{poly}+T_{mask}\right)\right\}}$$

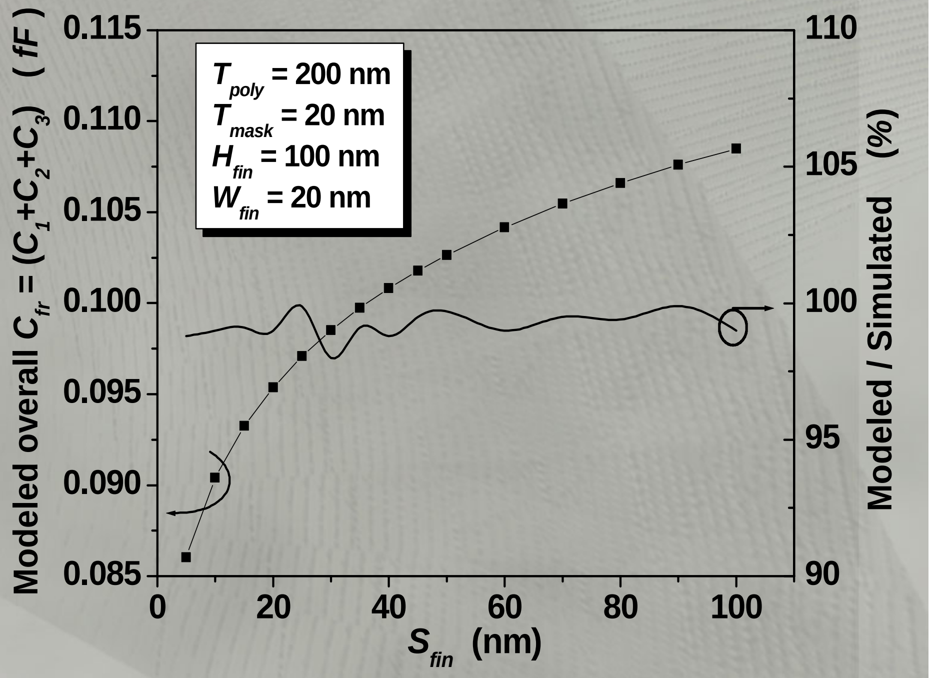
$$=\frac{2n\left(W_{fin}+S_{fin}\right)\varepsilon_{OX}}{\pi}\ln\left(1+\frac{L}{T_{poly}+T_{mask}}\right)$$



Fringing Capacitance Model (6)

- Comparison between model and 3-D numerical simulator



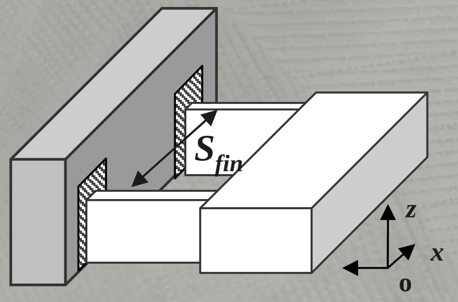


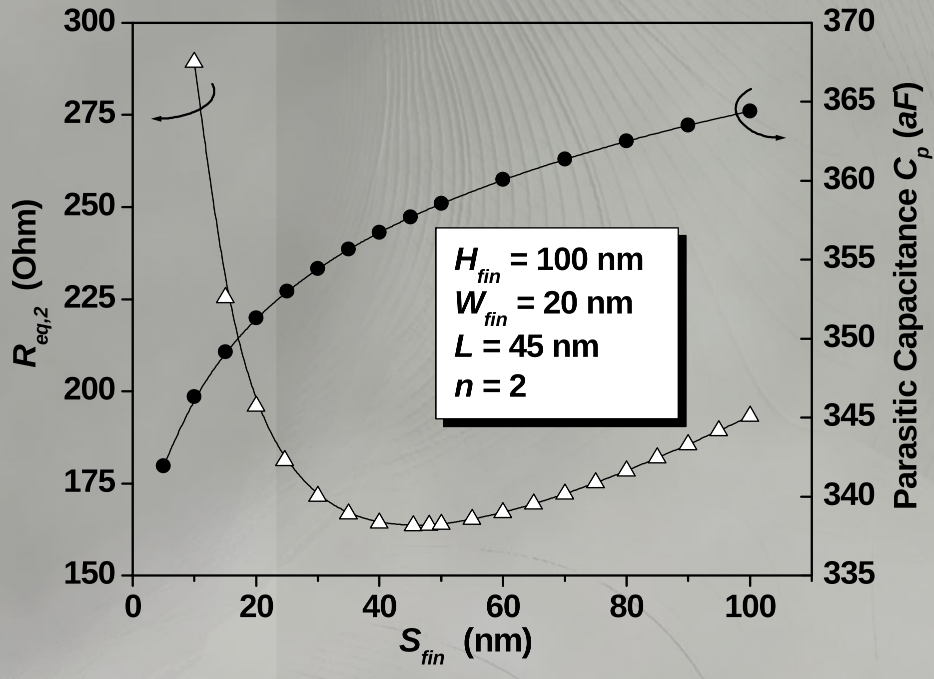
$$C_P = (C_1 + C_2 + C_2)$$

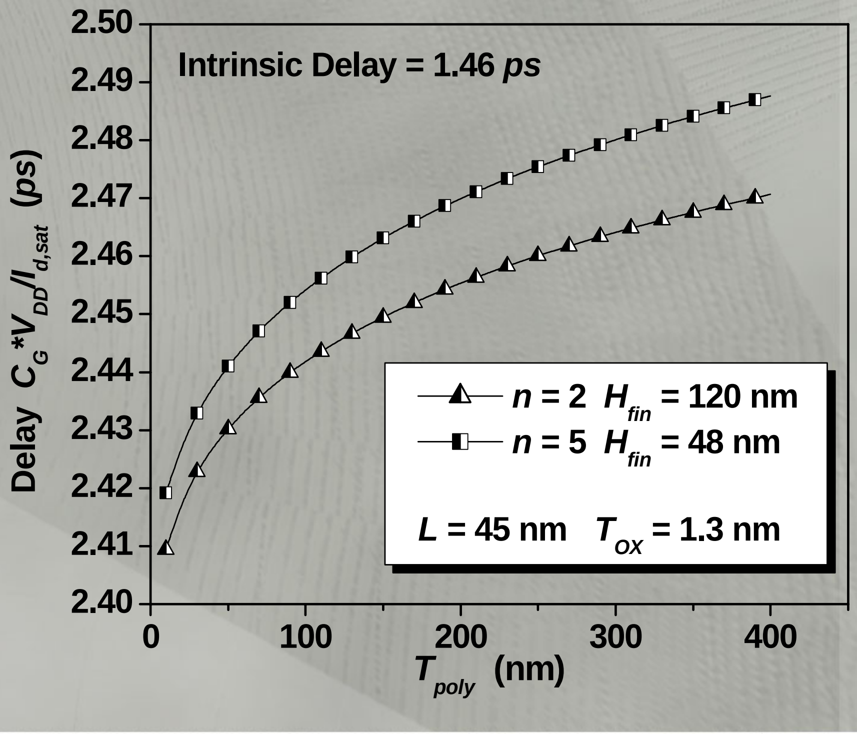
Preliminary Simulation Result

- The selection of Fin Spacing

$$f_T = \frac{g_m}{2\pi C_{in}} \qquad f_{\max} = \sqrt{\frac{f_T}{8\pi C_{GD} r_G}}$$

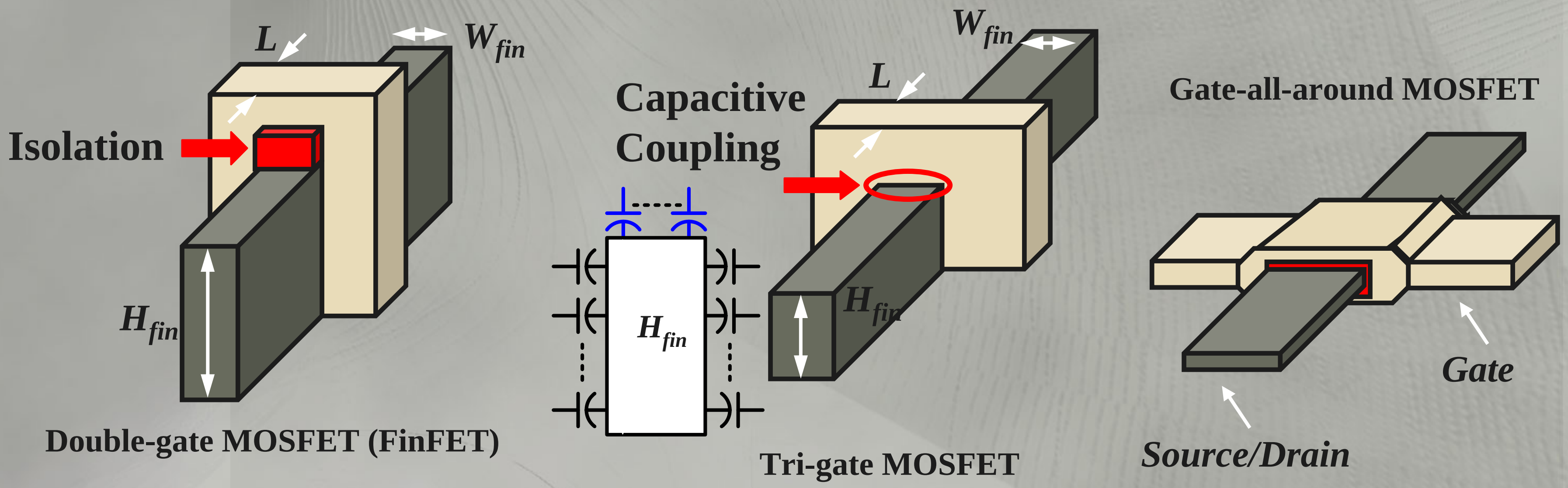




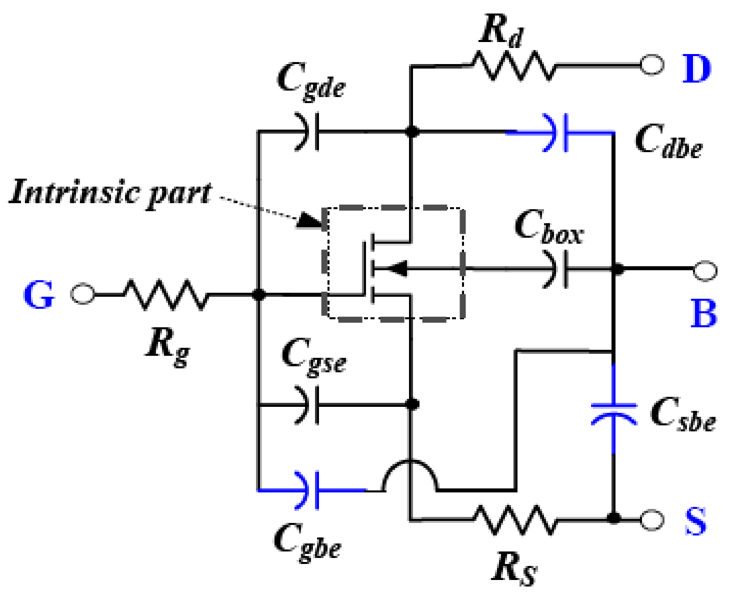


Extending to Multi-gate FETs

- **Same methodology for Tri-gate and Gate-all-around (GAA) MOSFETs**
  - Isolation → C_{OX} coupling



Model Implementation

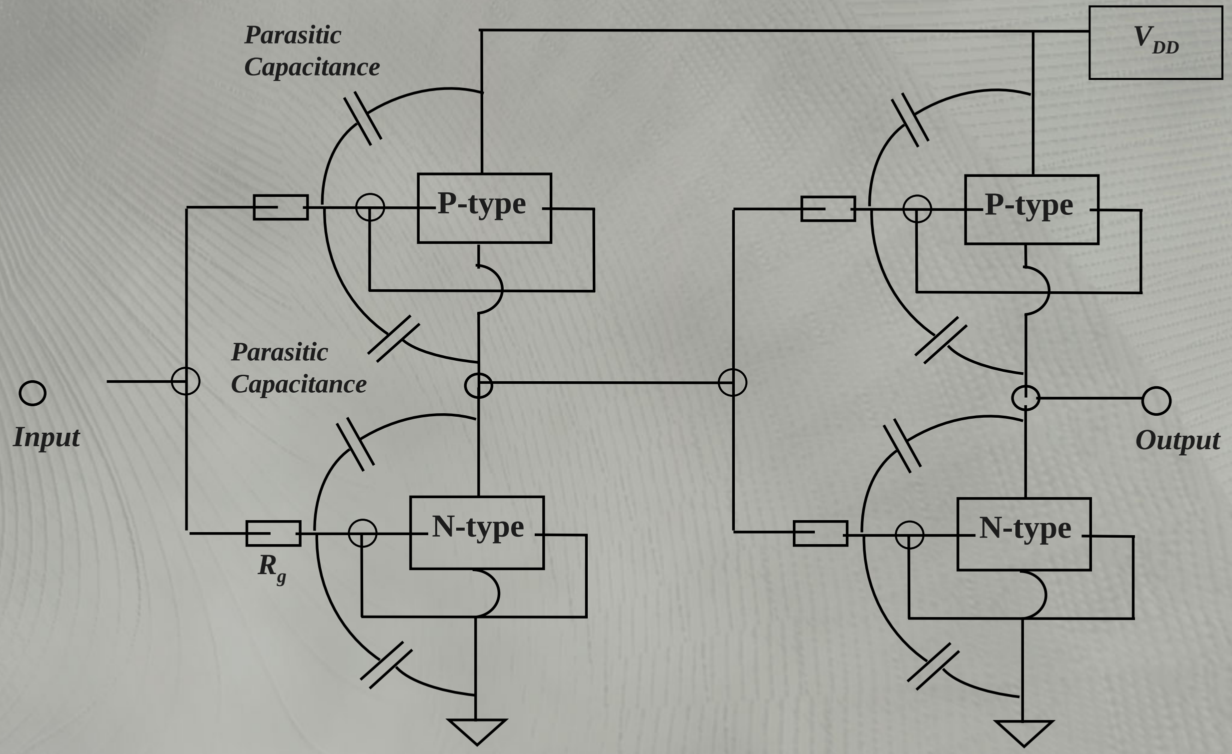


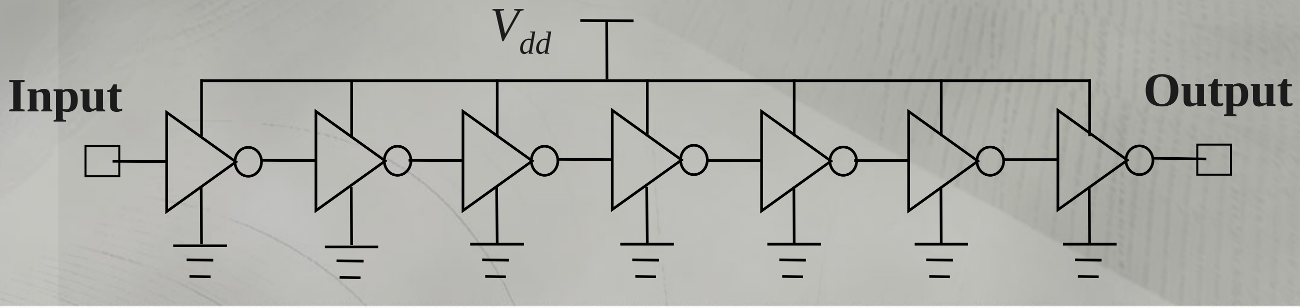
Non-planar multi-gate SOI Model
((*G*, *D*, *S*, *B*) four-terminal model: separate gate devices are not considered)

- The parasitic model has been implemented in Verilog-A platform
- Core model based on BSIM4 with parameters extracted to fit numerical data
- Parasitic components will be implemented as external elements at this stage

Circuit Examples [1]

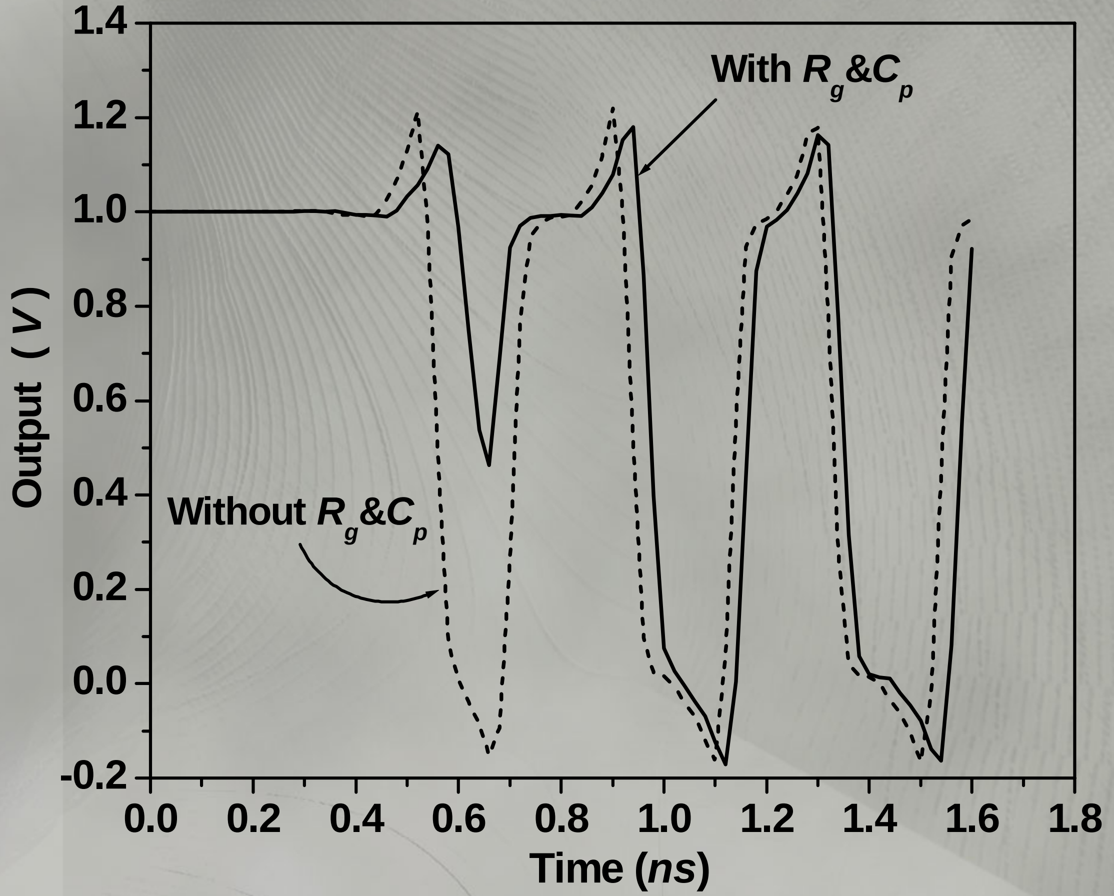
- **7-stage inverter**





Circuit Examples [2]

- **Output of the 7-stage inverter circuit**



Geometrical Parameters

20-nm T_{Si} (W_{fin})

T_{OX} = 1.3 nm,

L = 45 nm

H_{fin}=120nm

Number of Fins:

NMOSFET: 2

PMOSFET: 4

Summary

- Parasitic components become more significant in the process of CMOS devices scaling
- 3-D nature makes the modeling of parasitic components more difficult
- A geometry dependent gate resistance has been developed
- Parasitic capacitance between the gate and source/drain has been developed and preliminary result has been obtained
- Still a lot of work to need be done