



Semiconductor Research & Development Center

A Simple Yet Accurate Mismatch Model For Circuit Simulation

Zhenrong Jin, Yoo-mi Lee, Josef Watts,
Tony Bonaccio, Greg Schroer, and Neelesh Pai

IBM Microelectronics, Essex Junction, VT 05452



Outline

- **Motivation**
- **Mismatch Model**
- **Circuit Simulation Results**
- **Summary**

Motivation

- **Mismatch Is Getting Worse as Technology Scales**
- **Mismatch Model Is Critical for Some Circuit Design**
- **Sophisticated Model Is Often Required**
 - Correlation between all electrical parameters from a FET
 - Geometry dependences
 - Example: our previous work*
 - Disadvantage: slow down simulation
- **Balance Between Simulation Accuracy and Model Complexity**
 - A simple mismatch model is proposed
 - The model is accurate enough to predict circuit performance
 - The model reduces simulation time significantly

* Y.M. Lee et al., “SPICE Modeling of Multiple Correlated Electrical Effects of Dopant Fluctuations”, WCM 2005.

Model

- **Electrical Variation can be Obtained from Model Sensitivity Analysis**

- Threshold variation

$$\delta V_{th} = \frac{\delta V_{th}}{\delta v_{th0}} \delta v_{th0} + \frac{\delta V_{th}}{\delta k2} \delta k2 + \frac{\delta V_{th}}{\delta eta0} \delta eta0 + E(V_{th})$$

- Drain current variation

$$I_{DS} = \alpha u0 f(V_{th})$$

$$\frac{\delta I_D}{I_D} = \frac{\delta u0}{u0} + \frac{\delta f(V_{th})}{f(V_{th})} + E(I_D)$$

- Mismatch model parameters

$$\delta v_{th0}, k2, eta0, u0 = \frac{m_{v_{th0}, k2, eta0, u0}}{\sqrt{WL}}$$

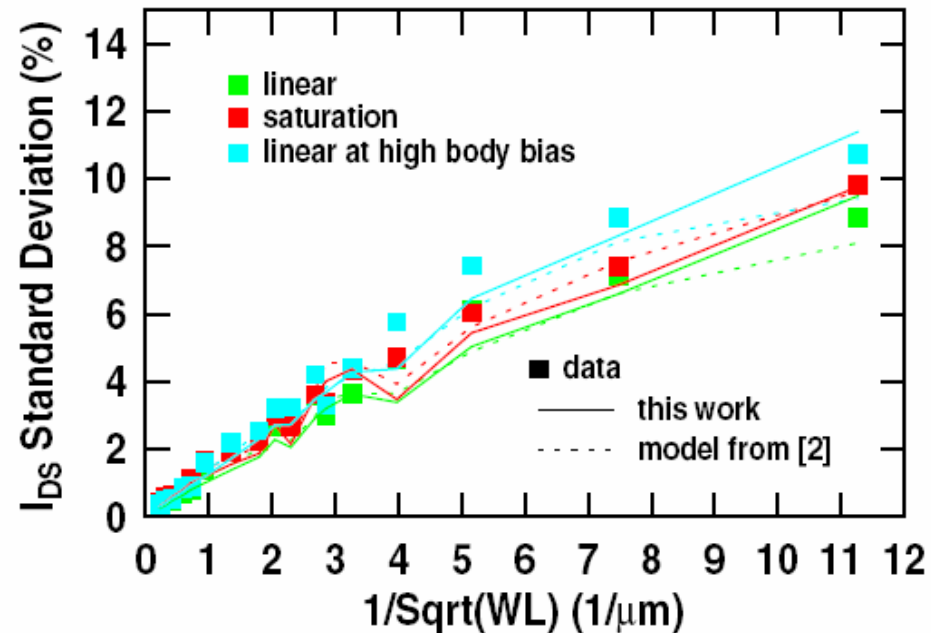
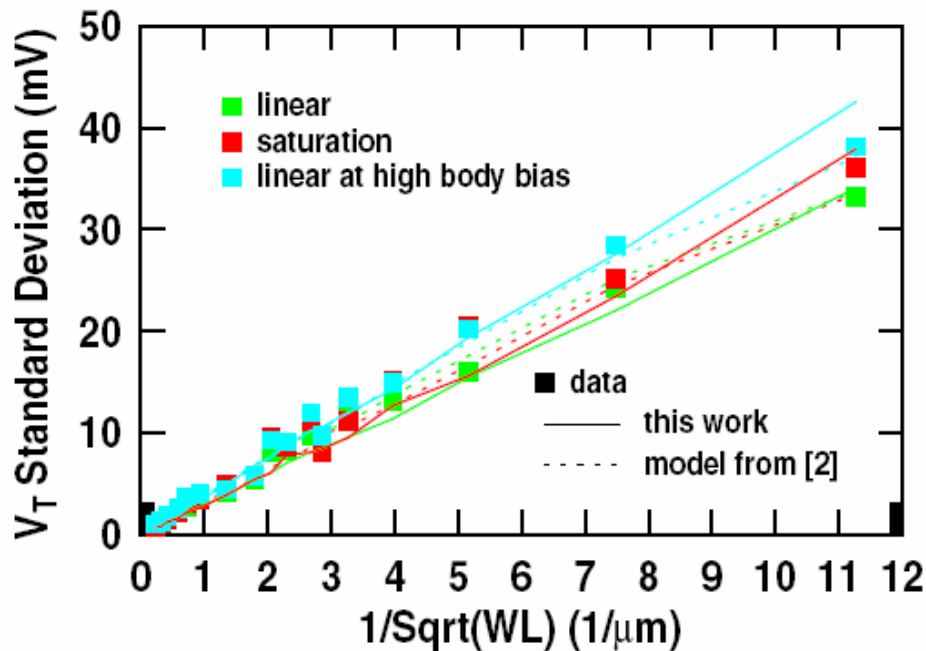
Model from Our Previous Work

- **“SPICE Modeling of Multiple Correlated Electrical Effects of Dopant Fluctuations”, WCM 2005.**
- **Model Is Based on Principle Factor Analysis**
 - Sensitivity matrix for each device size
 - PFA using correlation matrix for each size
 - Linear regression to extract model parameters across geometry
- **Pros: Model can Accurately Capture Mismatch Variation**
 - Electrical parameter correlation
 - Fractional power scaling of device size dependence
- **Cons: Complexity of the Model Significantly Increases Simulation Time**

Model-Hardware Correlation

■ Threshold Voltage and Drain Current Variation

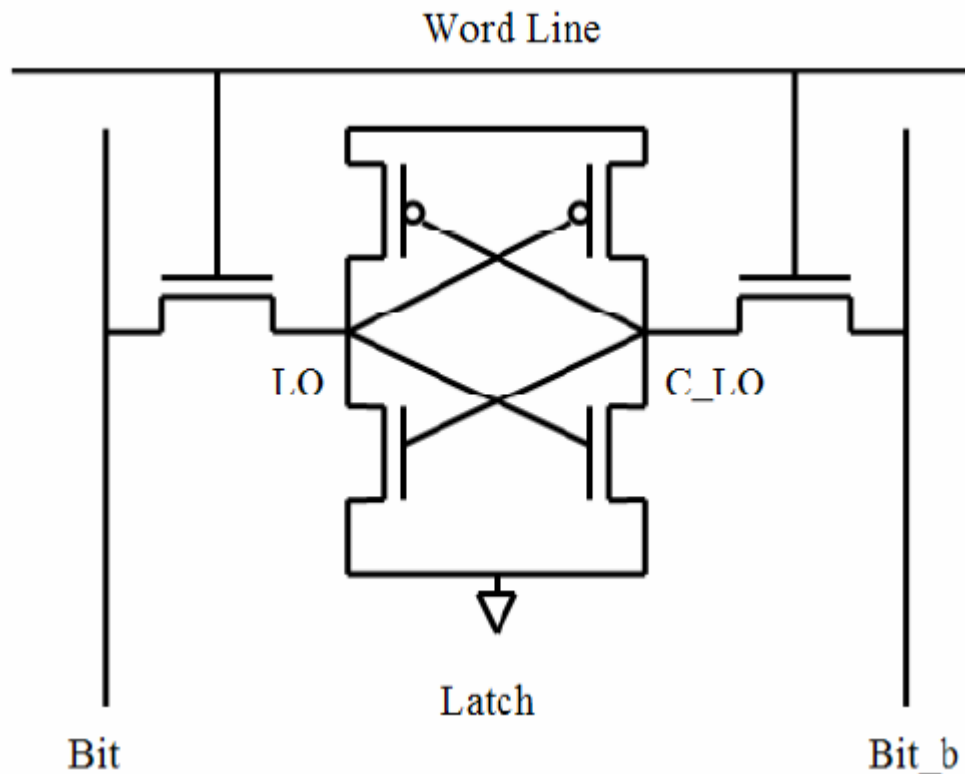
- three bias conditions: linear, saturation, and linear at high body bias
- The model matches the data well
- Small discrepancy from the model from our previous work*



* Y.-M. Lee et al., WCM 2005.

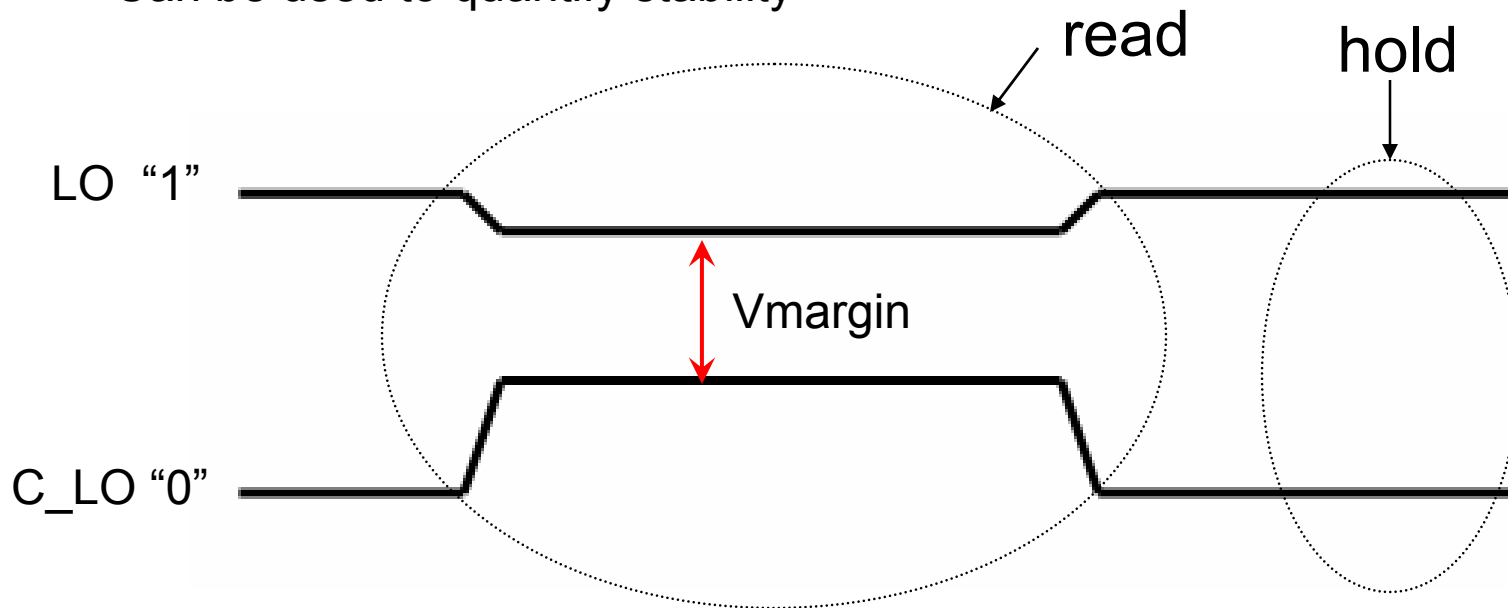
6-Transistor SRAM Cell

- Symmetrical Topology
- Mismatch Can Flip the State of a Cell
- IBM 90nm ASIC Library



Cell Read Stability

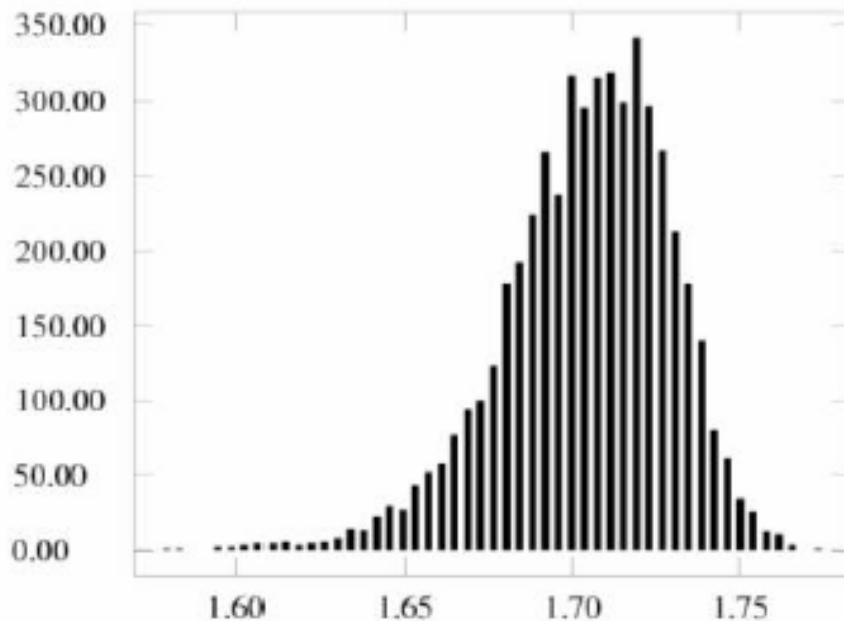
- Usually the Worst Constraint in Cell Design
- Latch Keeps the State of a Cell While Holding a Value
- Vmargin, the Node Voltage Difference During Read
 - Positive Vmargin ensures that latch return from meta-stable to original state
 - Can be used to quantify stability



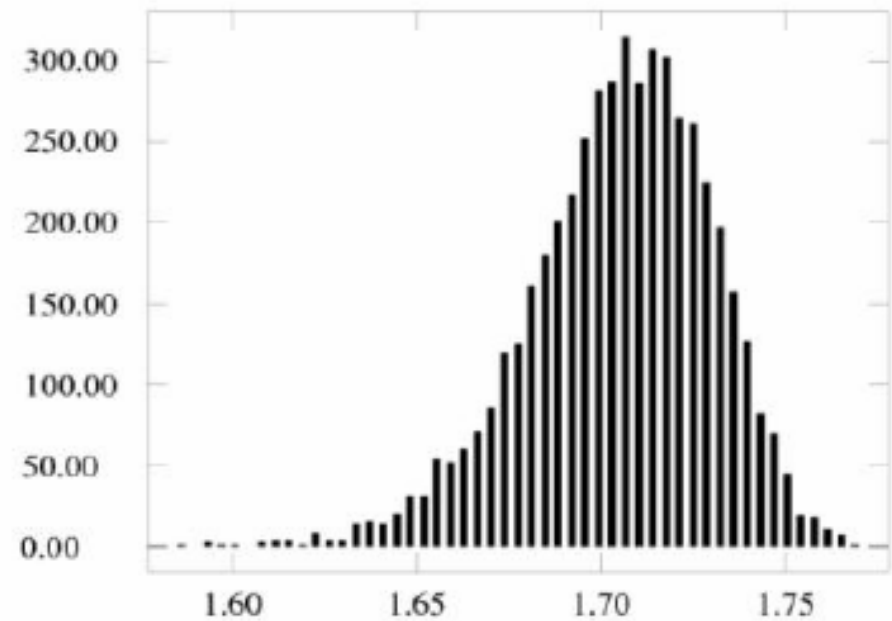
Results

- Histogram of 5000 Monte Carlo Runs from a Cell
- Simple Model Result is Similar to that Using the Previous Model

Model in This Work
 $V_{margin} \sigma = 24.3\text{mV}$

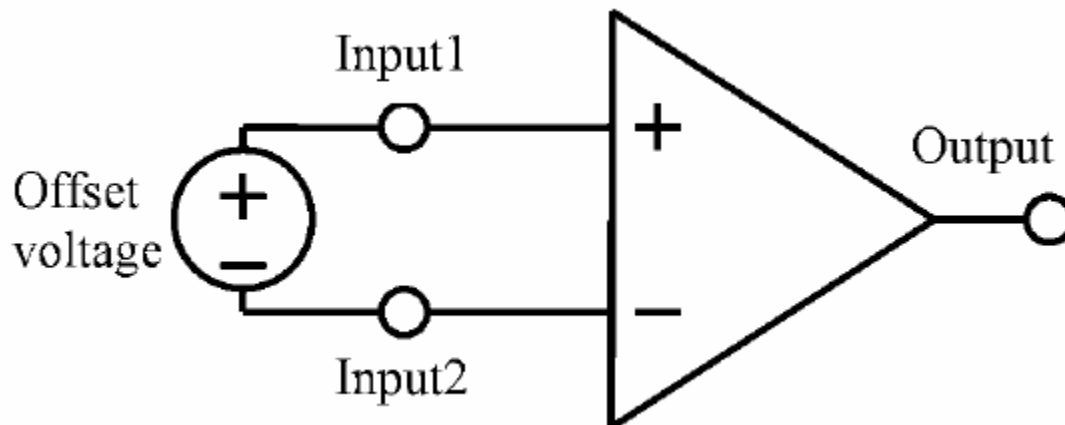


Model from Previous Work
 $V_{margin} \sigma = 23.1\text{mV}$



Operational Amplifier

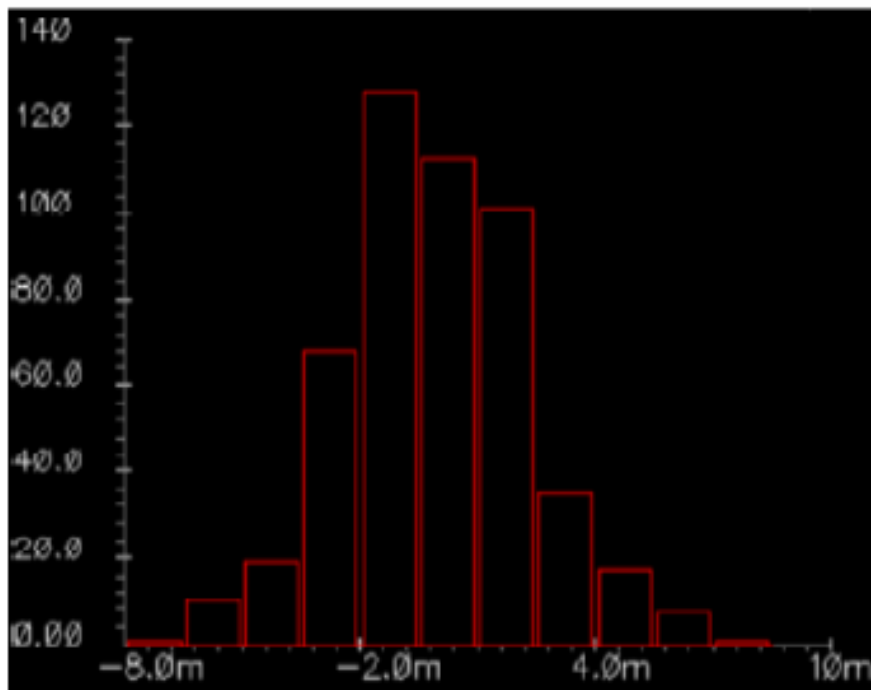
- Symmetrical Differential Amplifier Topology
- Mismatch Degrades Sensitivity, CMRR, and SNR etc.
- IBM 90nm ASIC Library



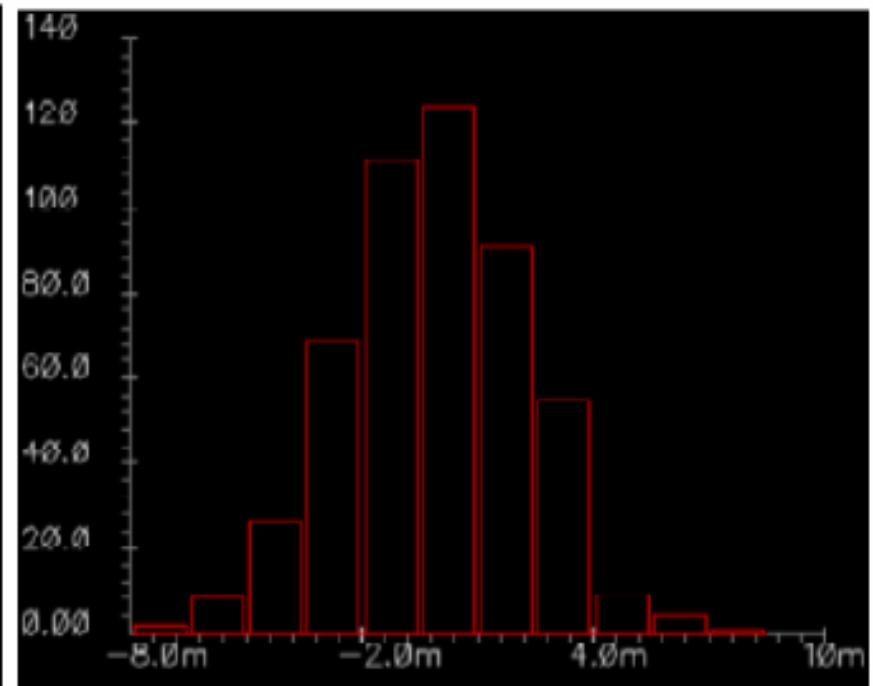
Results

- Histogram of 500 Monte Carlo Runs from a Cell
- Simple Model Result is Similar to that Using the Previous Model

Model in This Work
Input Offset Voltage $\sigma = 2.3\text{mV}$



Model from Previous Work
Input Offset Voltage $\sigma = 2.32\text{mV}$



Summary

- **A Simple Mismatch Model Is Proposed**
 - Based on BSIM model sensitivity analysis
 - Match hardware well
 - Reduce model extraction time
 - Reduce circuit simulation time by about 35%
- **The Model Is Accurate Enough to Predict Circuit Performance**