



Capacitance Model for Four-Terminal DG MOSFETs

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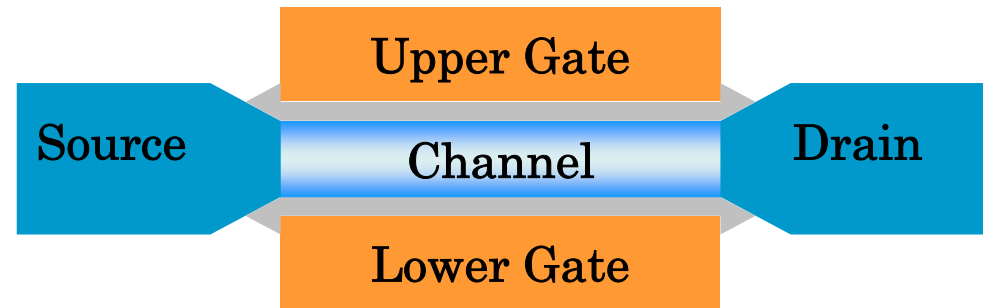
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1. Introduction: background and what has been achieved
2. Intrinsic capacitance: definition, derivation and results
3. Charge-sheet position: spurious capacitance and its remedy
4. Summary:



DG MOSFET

In ITRS2005,
 DG MOSFETs are **not**
 emerging devices;
 they are now on the road.



Year	'05	'06	'07	'08	'09	'10	'11	'12	'13	'14	'15	'16	'17	'18	'19	'20
MPU M1 HP	90	78	65	57	50	45	40	36	32	28	25	22	20	18	16	14
<i>EOT: High Performance MPU/ASIC</i>																
Conv. MOS	12	11	11	9	7.5	6.5	5	5								
DG							8	7	6	6	6	5	5	5	5	5
<i>EOT: Low Standby Power MPU/ASIC</i>																
Conv. MOS	21	20	19	16	15	14	14	13	12							
DG								13	12	11	11	11	10	10	9	9

Red bricks mean “manufacturable solutions are NOT known.”
 So, “DG MOSFETs will enter marketplace as early as 2011,
 but manufacturable solutions are NOT known.”



3- vs. 4-terminals

Usually DG MOSFETs are told as 3-terminal devices, because they achieve

- minimum short-channel effect
- high current drivability, or less severe EOT requirement
- no need for channel doping, no worry about its fluctuation
- ideal S factor

Alternative 4-terminal structure keeps advantages of

- minimum short-channel effect
- no need for channel doping, no worry about its fluctuation

but abandons

- high current drivability, or less severe EOT requirement
- ideal S factor

while adding

- 'body bias' by the gate, including aggressive forward body bias
- signal mixing by two gates



Transport modeling summary

1. Double charge-sheet model
2. Source-end charge calculated 1-D Poisson equation
3. Gradual channel approximation
4. No current mixing between two charge-sheets
5. Proportional charge profile for the other charge-sheet

Transport of two charge sheets are then solved independently.

Transport equation for one charge-sheet

$$I_i = q \left(\mu_i q \left(\frac{1}{C_{ii}} + \frac{n_j(0)/n_i(0)}{C_{ij}} \right) \frac{\partial n_i(y)}{\partial y} n_i(y) + D_i \frac{\partial n_i(y)}{\partial y} \right)$$

$$C_{11} = C_{OX1} + \left(C_{Si}^{-1} + C_{OX2}^{-1} \right)^{-1}$$

$$C_{22} = \left(C_{OX1}^{-1} + C_{Si}^{-1} \right)^{-1} + C_{OX2}$$

$$C_{12} = C_{OX1} + C_{OX2} + C_{OX1} C_{OX2} C_{Si}^{-1}$$



Mobility modeling

Bulk mobility μ_0



Surface mobility μ

$$\mu^{-1} = \mu_0^{-1} + \mu_{\text{PH}}^{-1} + \mu_{\text{SR}}^{-1}$$

$$\mu_{\text{PH}} = 5.85 \times 10^4 \times E_{\text{tr}}^{-1/3}$$

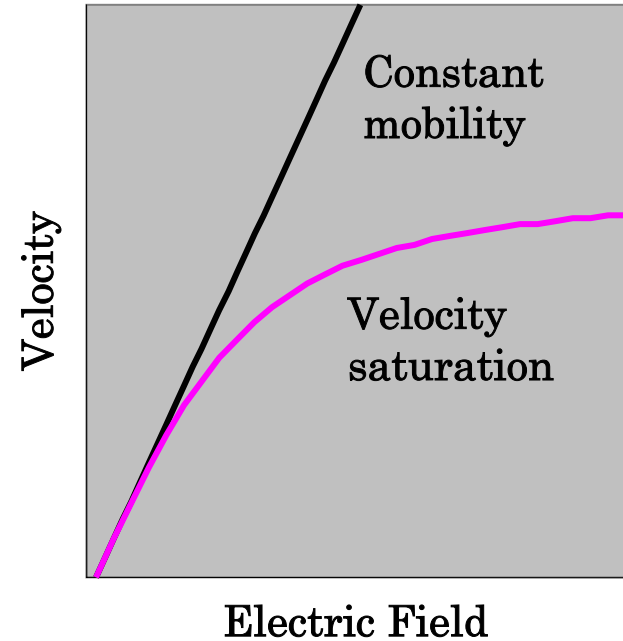
$$\mu_{\text{SR}} = 4 \times 10^{15} (E_{\text{tr}} + kT/qT_{\text{Si}})^{-2}$$



Velocity saturation

$$\mu \rightarrow \left(1 + |E(y) / E_c|^2\right)^{-1/2} \mu$$

Critical electric field E_c is for drift current.



Transport equation with velocity saturation

Transport equation

$$-q\mu \left(\frac{q}{C} \frac{dn}{dy} n + \frac{kT}{q} \frac{dn}{dy} \right) = I_i$$

Velocity saturation

$$\mu \rightarrow \left(1 + \left| \frac{E}{E_c} \right|^2 \right)^{-1/2} \mu$$

Transport equation with velocity saturation

$$= -q\mu \left(\frac{q}{C} \frac{dn}{dy} n + \frac{kT}{q} \frac{dn}{dy} \right) = I_i \left(1 + \left| \frac{E}{E_c} \right|^2 \right)^{1/2}$$

Solution

$$-\beta E_c n_b L_{tr} = \frac{1}{2} \left(n_{aL} \sqrt{n_{aL}^2 - n_b^2} - n_{a0} \sqrt{n_{a0}^2 - n_b^2} \right) - \frac{1}{2} n_b^2 \log \left(\frac{n_{aL} + \sqrt{n_{aL}^2 - n_b^2}}{n_{a0} + \sqrt{n_{a0}^2 - n_b^2}} \right)$$

$$n_{aL} = n_a(L_{tr})$$

$$n_{a0} = n_a(0)$$

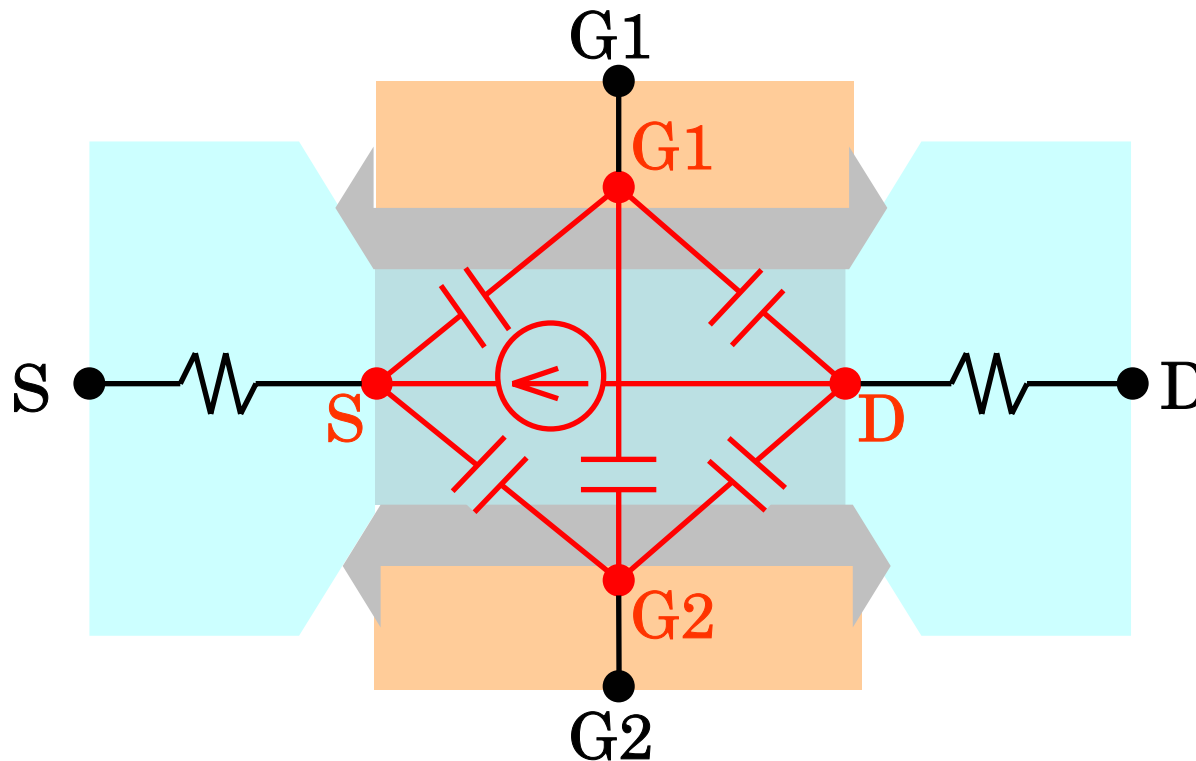
$$n_a = n / (CkT/q^2) + 1$$

$$n_b = (I_i / q\mu E_c) / (CkT/q^2)$$



Capacitance model

Intrinsic part (red) is modeled



Charges in the gates

Charges in the charge-sheets

$$Q_i = -\frac{CkT}{q} \int_0^{L_{\text{eff}}} (n_a - 1) dy = \frac{CkT}{q} \left(\frac{1}{\beta E_c n_b} \int_{n_{a0}}^{n_{aL}} n_a \sqrt{n_a^2 - n_b^2} dn_a + L_{\text{eff}} \right) \\ \left[+ \frac{n_{L_{\text{eff}}} + n_{L_g}}{2} (L_G - L_{\text{eff}}) \quad (\text{when } L_G > L_{\text{eff}}) \right]$$

Charges in the gates

$$Q_{G1} = C_{\text{tot}} (V_{G1} - V_{G2}) - \frac{C_{\text{OX1}}}{C_{11}} Q_1 - \left(1 - \frac{C_{\text{OX2}}}{C_{22}} \right) Q_2$$

$$Q_{G2} = C_{\text{tot}} (V_{G2} - V_{G1}) - \left(1 - \frac{C_{\text{OX1}}}{C_{11}} \right) Q_1 - \frac{C_{\text{OX2}}}{C_{22}} Q_2$$

$$C_{\text{tot}} = \left(C_{\text{OX1}}^{-1} + C_{\text{Si}}^{-1} + C_{\text{OX2}}^{-1} \right)^{-1}$$



Capacitances

Capacitances among **S**, **D**, **G1** and **G2**.

$$\frac{\partial Q_{G1}}{\partial V_{G1}} = C_{G1S} + C_{G1G2} + C_{G1D}$$

$$\frac{\partial Q_{G2}}{\partial V_{G2}} = C_{G2S} + C_{G2G1} + C_{G2D}$$

$$\frac{\partial Q_{G1}}{\partial V_D} = -C_{G1D}, \quad \frac{\partial Q_{G2}}{\partial V_D} = -C_{G2D}$$

$$\frac{\partial Q_{G1}}{\partial V_{G2}} = -C_{G1G2}, \quad \frac{\partial Q_{G2}}{\partial V_{G1}} = -C_{G2G1}$$



$$C_{G1S} = -\frac{\partial Q_{G1}}{\partial V_{G1}} + \frac{\partial Q_{G1}}{\partial V_{G2}} + \frac{\partial Q_{G1}}{\partial V_D}$$

$$C_{G2S} = -\frac{\partial Q_{G2}}{\partial V_{G2}} + \frac{\partial Q_{G2}}{\partial V_{G1}} + \frac{\partial Q_{G2}}{\partial V_D}$$

$$C_{G1D} = -\frac{\partial Q_{G1}}{\partial V_D}, \quad C_{G2D} = -\frac{\partial Q_{G2}}{\partial V_D}$$

$$C_{G1G2} = -\frac{\partial Q_{G1}}{\partial V_{G2}}, \quad C_{G2G1} = -\frac{\partial Q_{G2}}{\partial V_{G1}}$$

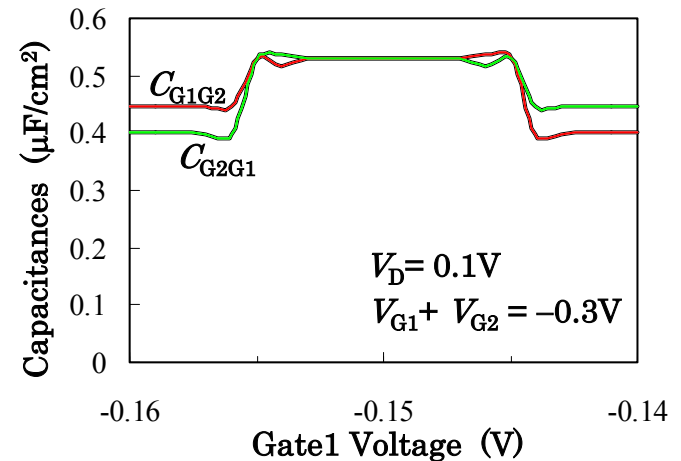
Capacitance between **G1** and **G2** is defined in two ways:

C_{G1G2} and C_{G2G1} .



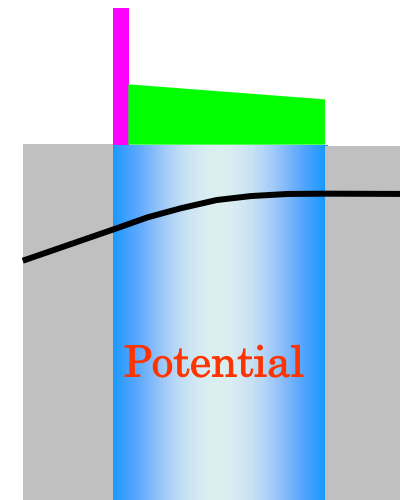
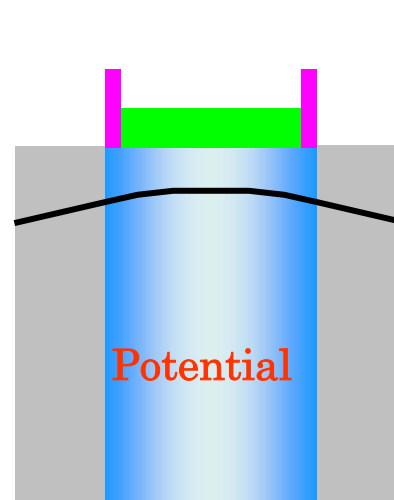
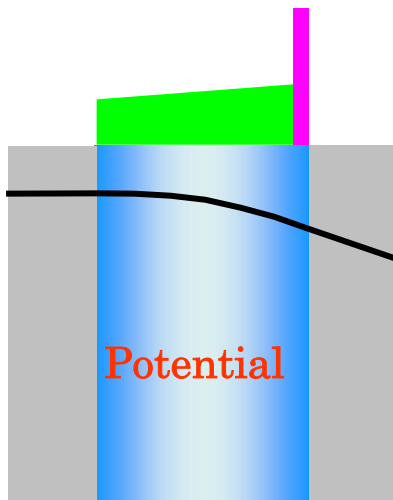
Charge-sheet position

Large spurious charge shift is produced when two gate voltages are see-sawed in the double charge-sheet region. It does not diminish even when the gate voltages are in the deep subthreshold region, resulting in overwhelming jump in the capacitance between gates.

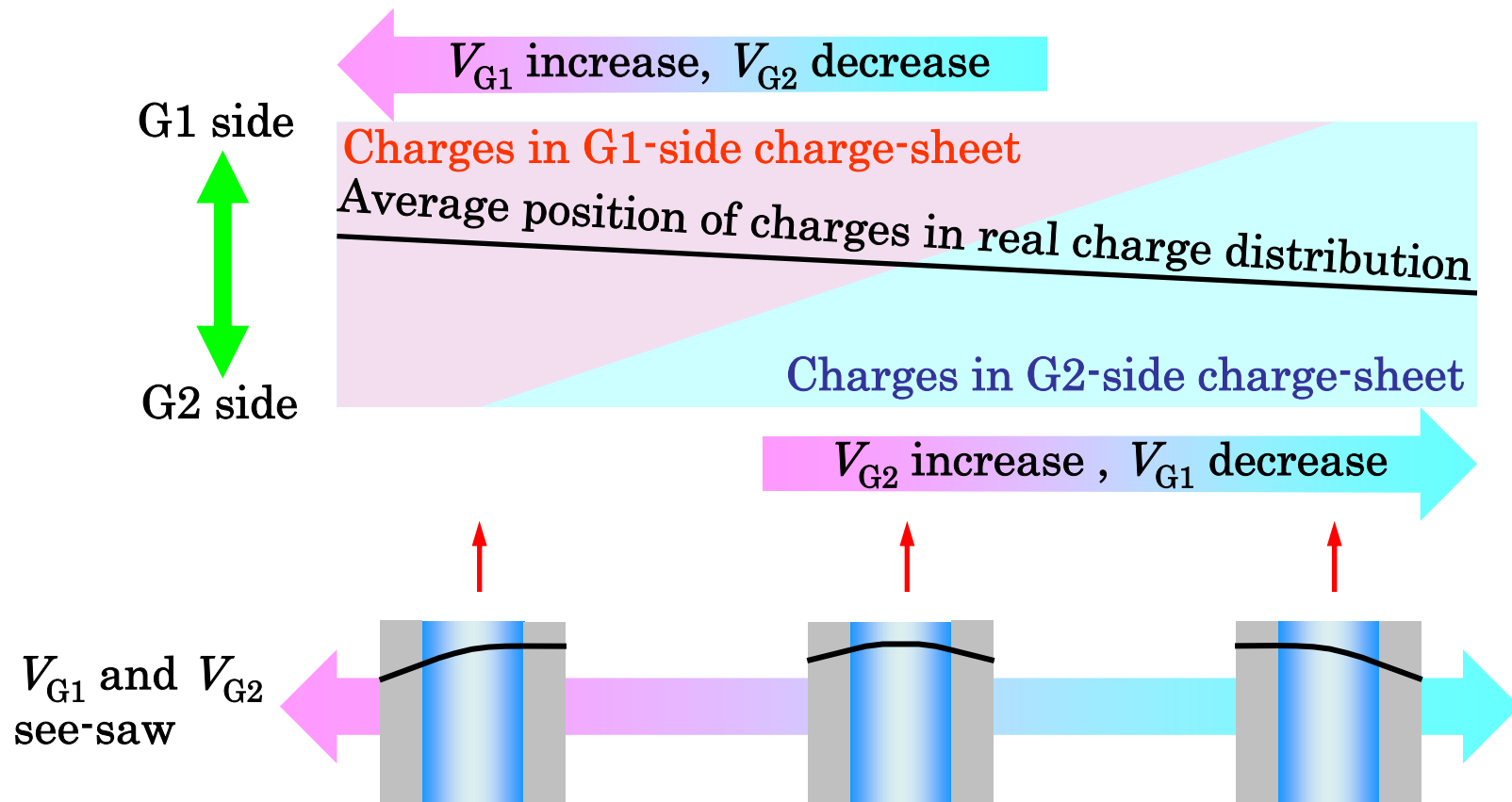


■ Real charge density

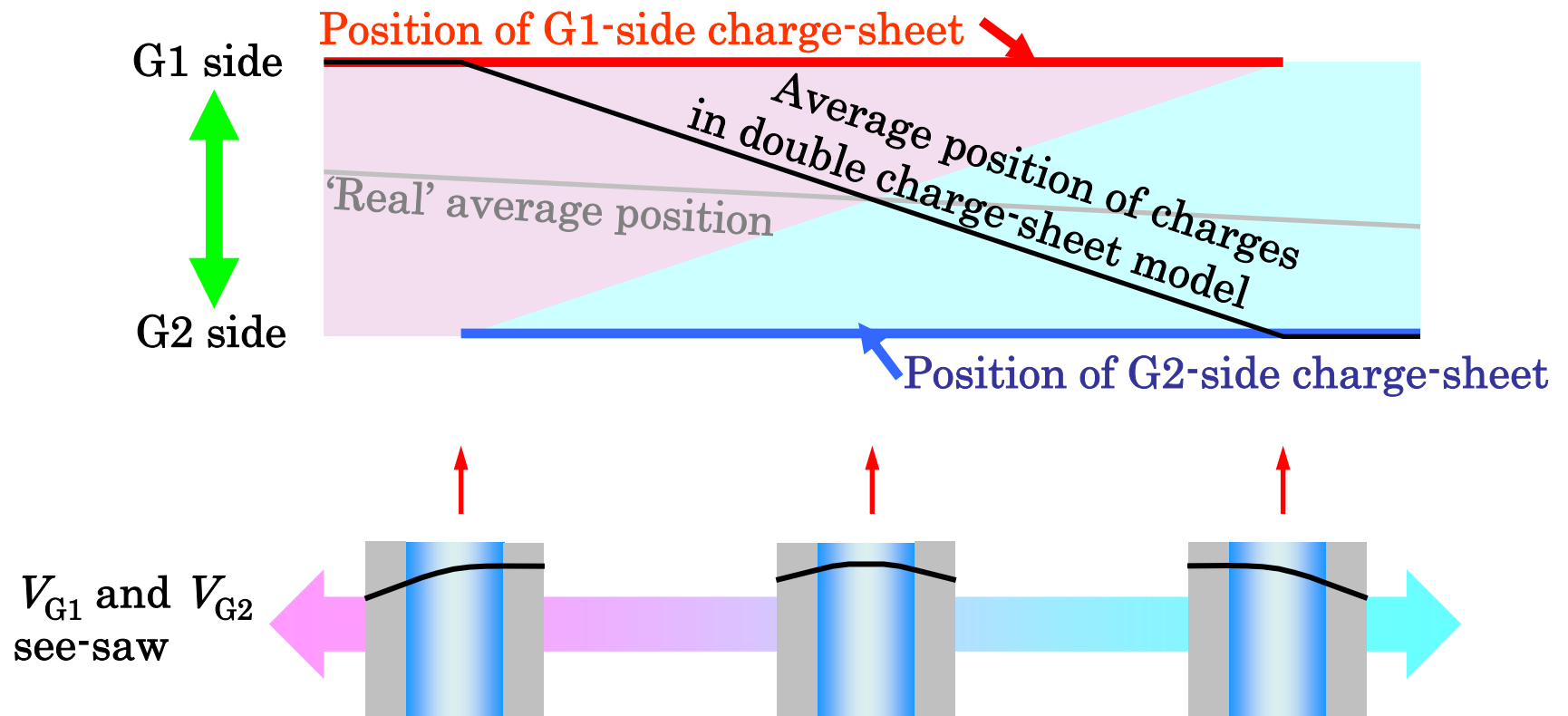
■ Modeled charge density



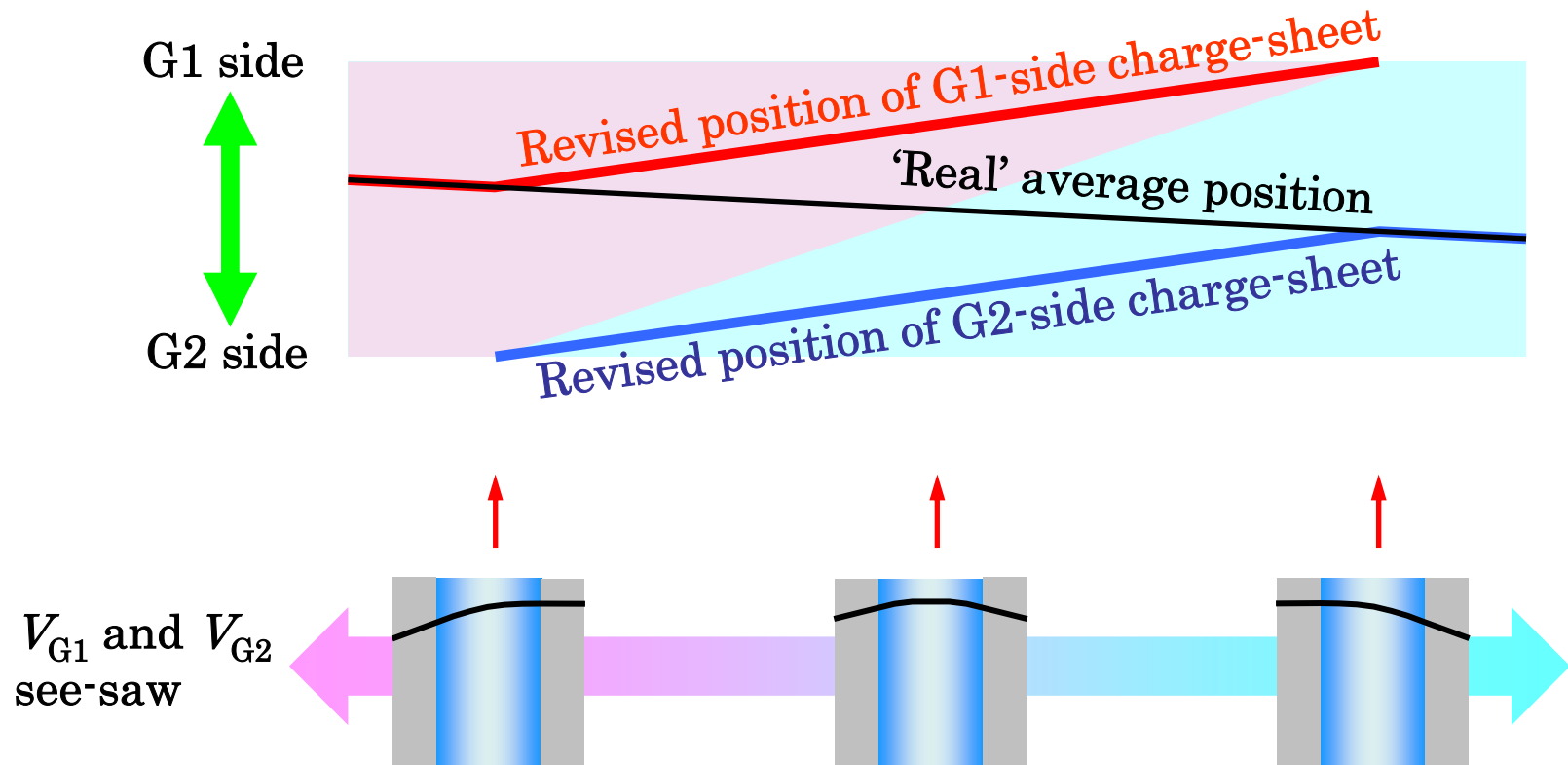
Average charge position - divide charge in two sheets



Average charge position - in double charge-sheet model



Charge-sheets in the averaged position



Variable charge-sheet position

Average charge-position

$$V_{G1} + V_{G2} = -0.3V \quad V_D = 0.1V$$

Single charge-sheet

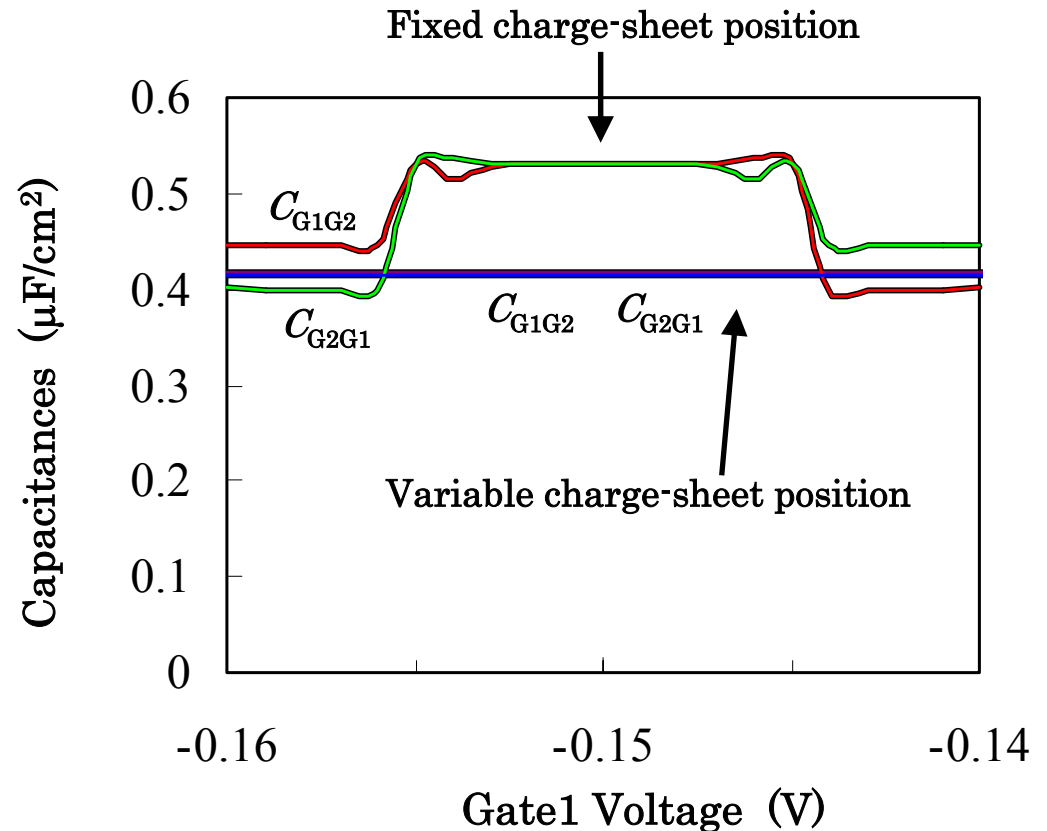
$$x_{ch1} = \frac{(\psi_{S1} - \psi_{S2}) - t_{Si} E_{\perp S2}}{E_{\perp S1} - E_{\perp S2}}$$

Double charge-sheet

$$x_{ch1, ch2} = \frac{\psi_{S1, S2} - \psi_M}{E_{\perp S1, S2}}$$

Positions are calculated by using source carrier density profile.

They are assumed to be constant in the entire channel.

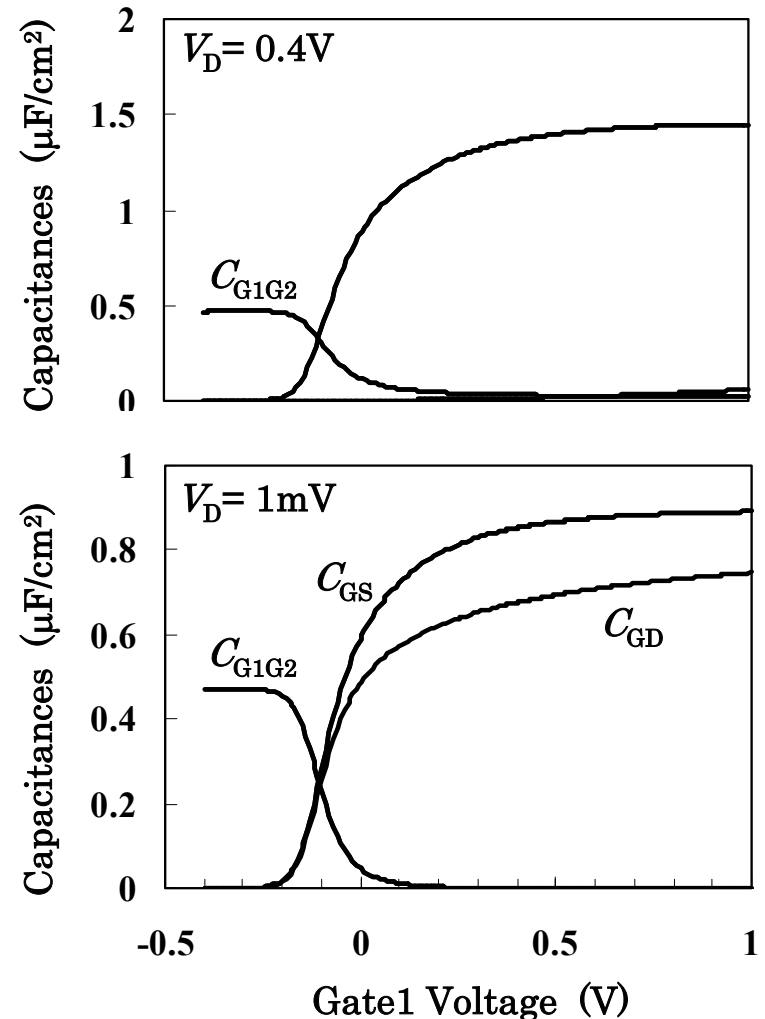


Capacitances of DG MOSFET

Three-terminal case

$$\begin{aligned}L_G &= 50\text{nm} \\ T_{\text{OX1}} &= 2\text{nm} \\ T_{\text{OX2}} &= 2\text{nm} \\ T_{\text{Si}} &= 10\text{nm}\end{aligned}$$

Even when V_D approaches 0V, C_{GD} does not approach C_{GS} . This asymmetry is caused by the device modeling not symmetrical with respect to the source and the drain.



Capacitances of DG MOSFET

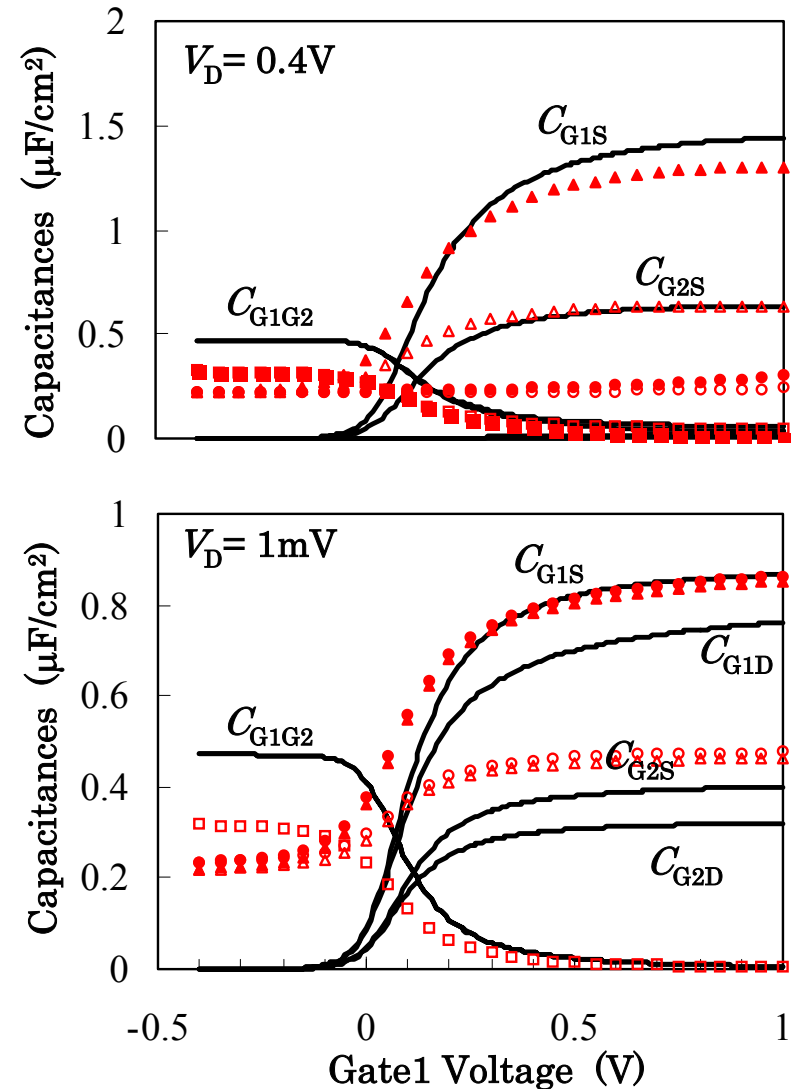
Four-terminal case

$L_G = 50\text{nm}$
 $T_{\text{OX1}} = 2\text{nm}$
 $T_{\text{OX2}} = 2\text{nm}$
 $T_{\text{Si}} = 10\text{nm}$

$V_{G2} = -0.4\text{V}$

Red marks are for
ATLAS device
simulator results.

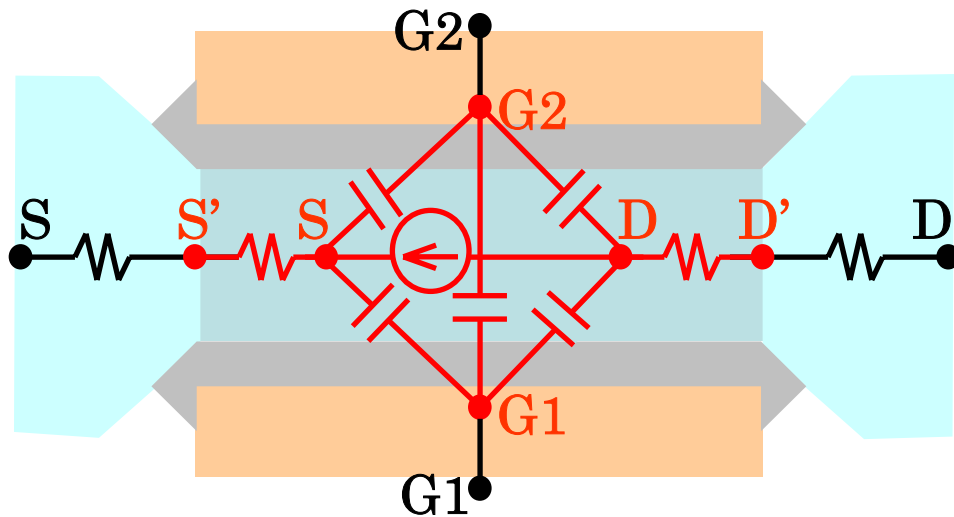
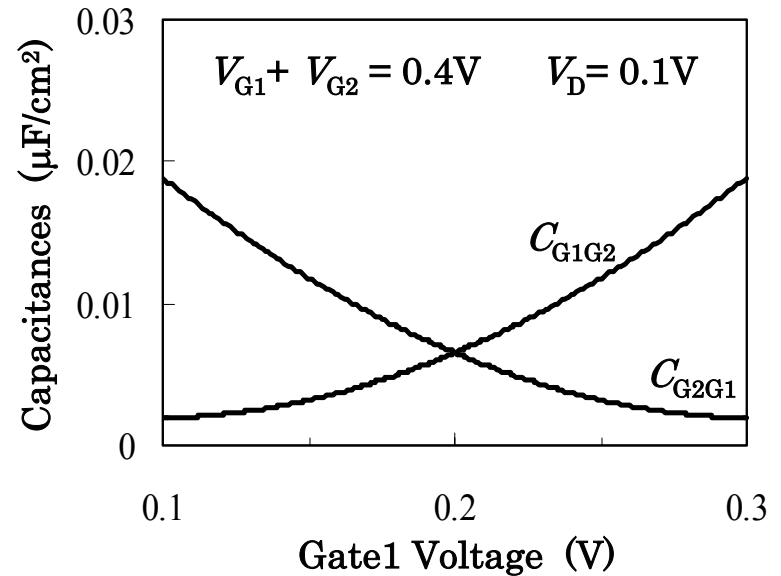
Discrepancy from the device simulator in the subthreshold region is caused by the lack of fringe capacitances, which increases C_{G1S} , C_{G2S} , C_{G1D} and C_{G2D} , while it decreases C_{G1G2} and C_{G2G1} because of the screening effect by the source and the drain region.



Capacitance model

C_{G1G2} and C_{G2G1} do not match.

To make C_{G1G2} and C_{G2G1} identical, Intrinsic circuit should include part of channel resistance.



$$L_G = 50\text{nm}$$

$$T_{\text{OX1}} = T_{\text{OX2}} = 2\text{nm}$$

$$T_{\text{Si}} = 10\text{nm}$$

Summary

An intrinsic-capacitance model is proposed.

Capacitances are derived from the derivatives of the gate charges.

When the channel is in the sub-threshold region, capacitance anomaly was observed.

Fixed charge-sheet position was found to be the cause of the anomaly.

The model was modified such that the position of charge-sheets are at the mean position of the carrier.

This remedy removed the anomaly.

It was found that $C_{G_1G_2}$ and $C_{G_2G_1}$ do not match, as far as the modeled circuit does not include part of the channel resistance explicitly.

