

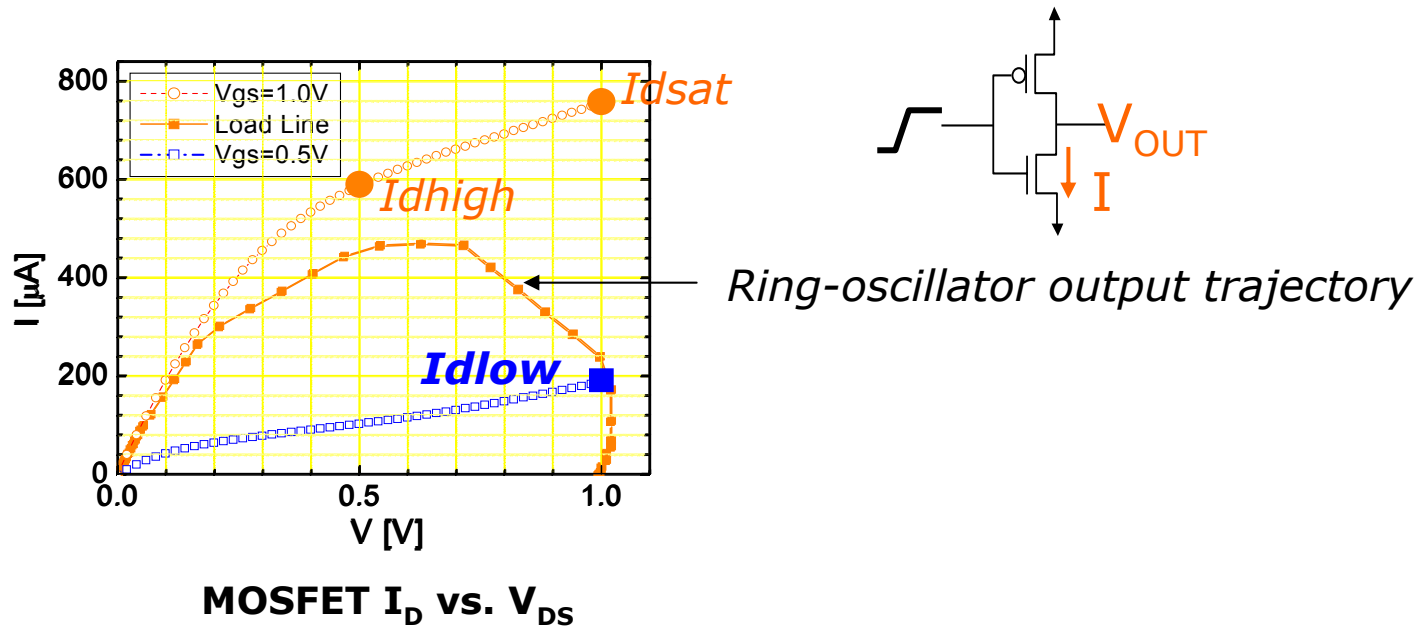
On Idlow with Emphasis on Speculative SPICE Modeling

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What & Why is Idlow?



- Idlow – drain current at low V_{GS} & high V_{DS} ($V_{GS}=V_{DD}/2$, $V_{DS}=V_{DD}$)
- Idlow & Idhigh – more relevant to transient analysis than Idsat*
 - Closer to the node output trajectory in ring oscillators than Idsat
 - $(Idlow+Idhigh)/2$ well approximates Ideff which directly relates to inverter delay
- Idlow & Idhi used together to gauge FET performance

*M. H. Na, et al., "The effective drive current in CMOS inverters," IEDM, 2002

Speculative SPICE Modeling

- Speculative modeling
 - Model extraction using only a few key electrical parameters (“*targets*”) of MOSFETs instead of full I-V curves
 - Necessitated by parallel technology development and circuit/system design
- Cross-device targets
 - Targets of different W/L devices provided to ensure W/L scalability and proper corner models
- Cross-voltage targets
 - Driven by performance per watt optimization
 - Targets at different supply voltages provided to project performance and power requirement

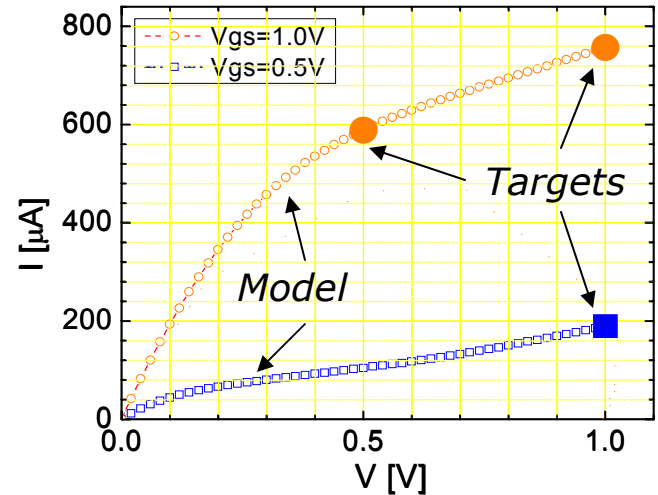


Illustration of speculative modeling

Challenges with Idlow

- Model vs. target accuracy
 - Frequent observation of sub-optimal fit between models and targets, particularly cross-W/L and cross- V_{DD}
- Challenges in analyzing Idlow
 - Strong dependence on threshold voltage
 - Isolated Idlow analysis does not yield clear guidelines
- Consequences
 - Prolonged model extraction time
 - Uncertain trade-off in matching threshold voltage and Id targets
- Further understanding and improved analysis of Idlow is thus required

Holistic Approach to Idlow Analysis

- Idlow analysis in conjunction with Idsat, Vt, and V_{DD}
- Alpha-power law model for the saturation region *
 - α - indicator of velocity saturation

$$I_{DS} \propto (V_{GS} - V_T)^\alpha$$

- Seeking correlation between Idlow/Idsat and

$$\left[1 - \frac{1}{2} \left(1 - \frac{V_{tsat}}{V_{DD}} \right)^{-1} \right]^\alpha$$

- Or,

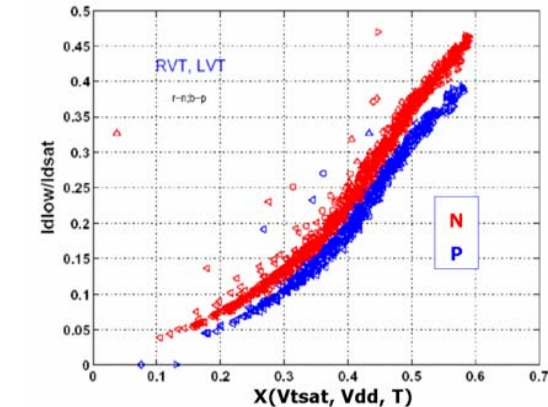
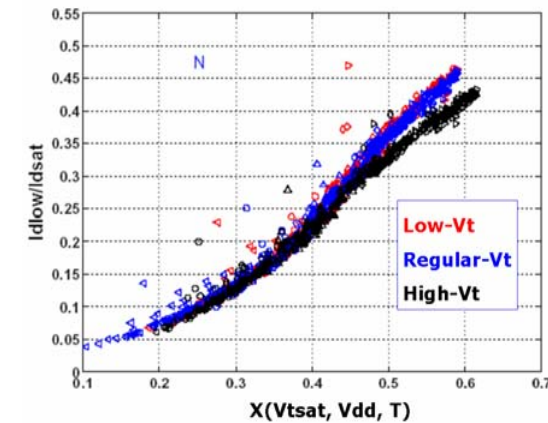
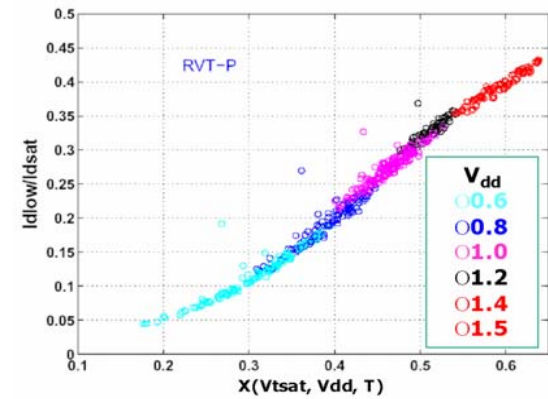
$$X = \left[1 + A(T - 25) \right] \left[1 + B(V_{DD} - 1) \right] \left[1 - \frac{1}{2} \left(1 - \frac{V_{tsat}}{V_{DD}} \right)^{-1} \right]^\alpha$$

- using A & B to account for other factors..

*T. Sakurai, et al., "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," JSSC, 1990

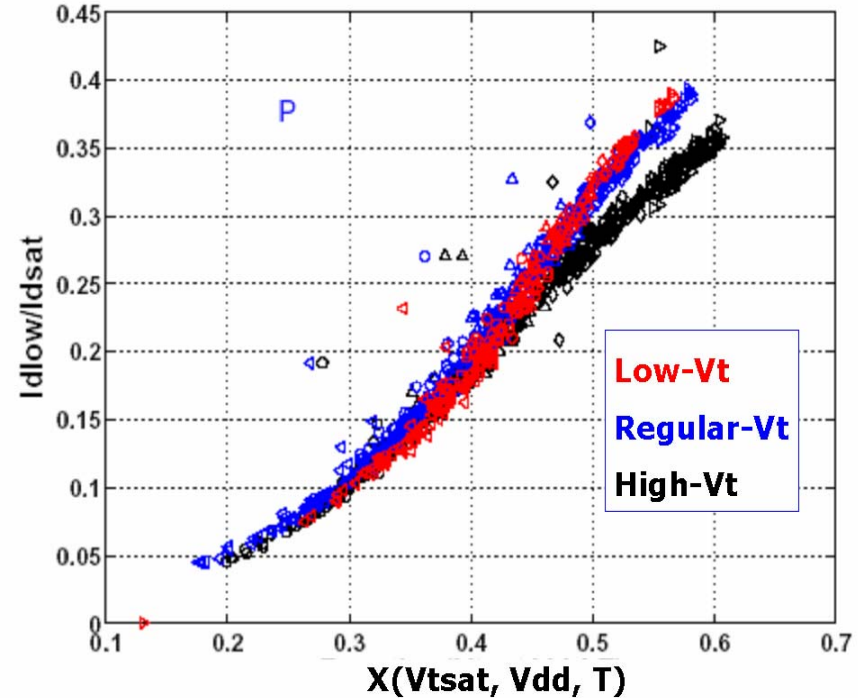
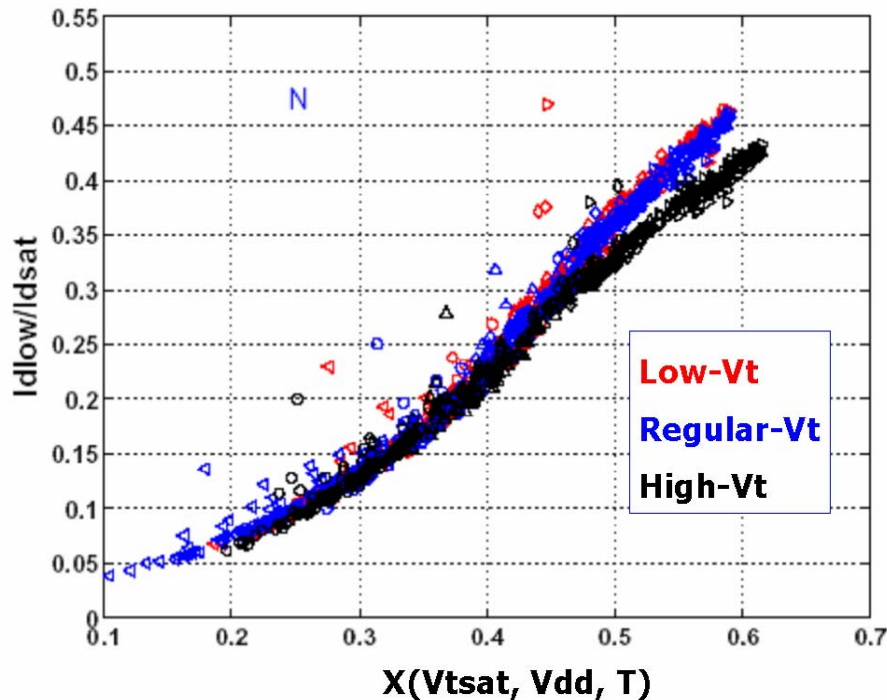
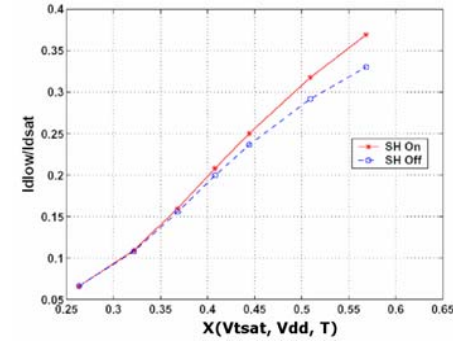
Results

- Unique I_{dlow}/I_{dsat} vs. $X(V_{tsat}, V_{DD}, T)$ correlation obtained
- In multi-Vt technologies different correlation curves are observed among different Vt's
 - May be caused by the self-heating effect and different current levels
- Different correlation curves are observed between N- and P-type devices
 - Possibly caused by different impact ionization rates of electrons and holes
- Applications of the new I_{dlow} analysis methodology
 - Holistic analysis of measured electrical test data
 - I_{dlow} target projection & iteration



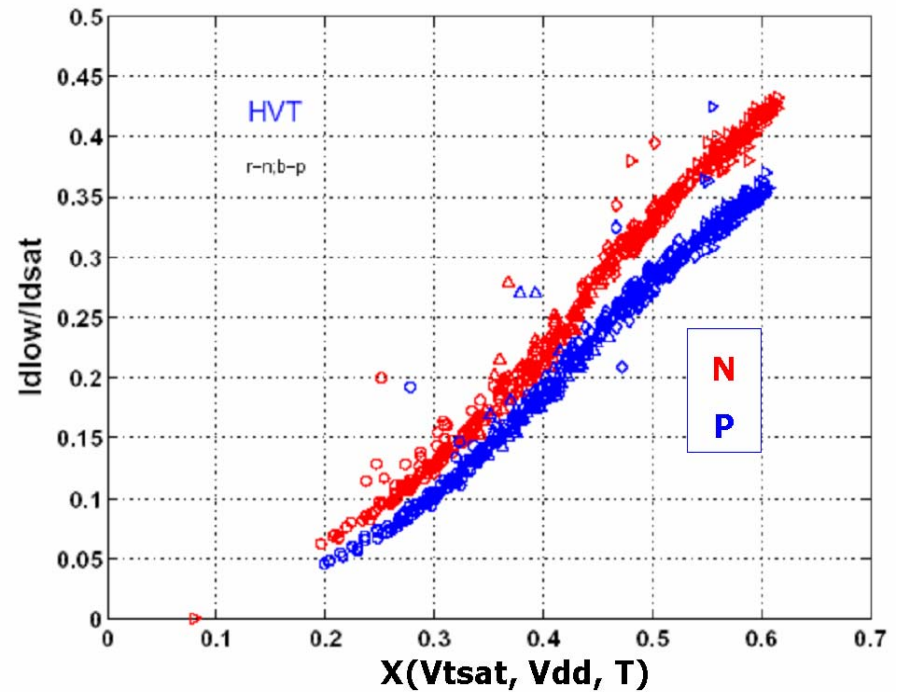
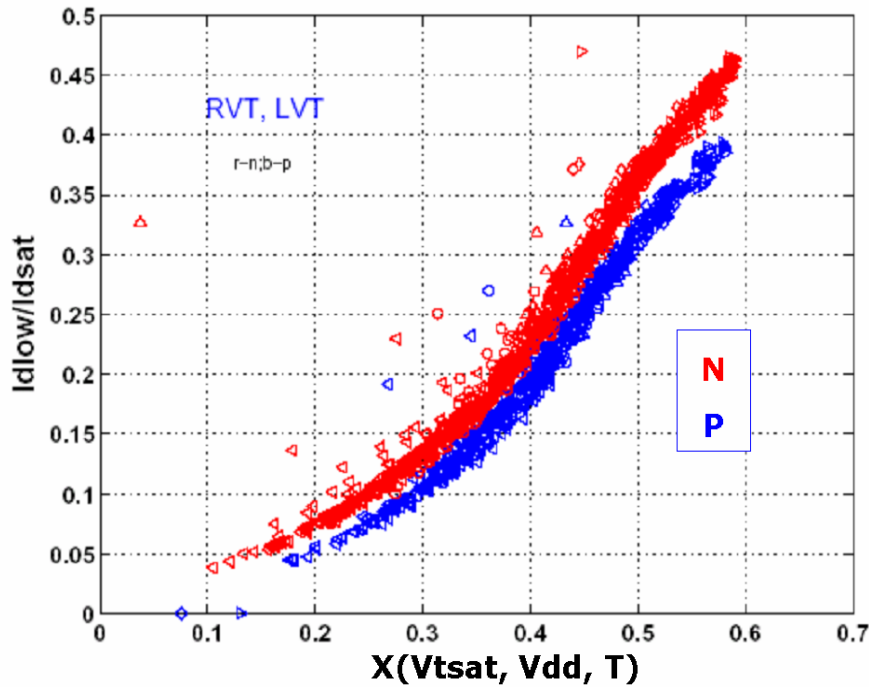
Cross-Vt Comparison

- All Vt devices show \sim identical trends for up to $\sim 1.0V$
- HVT shows lower I_{dlow}/I_{dsat} than RVT/LVT at large V_{DD}
- Self-heating mainly degrades $I_{dsat} \rightarrow$ higher I_{dlow}/I_{dsat} ratio in N than P
 - Same LVT/RVT trends may result from close current levels

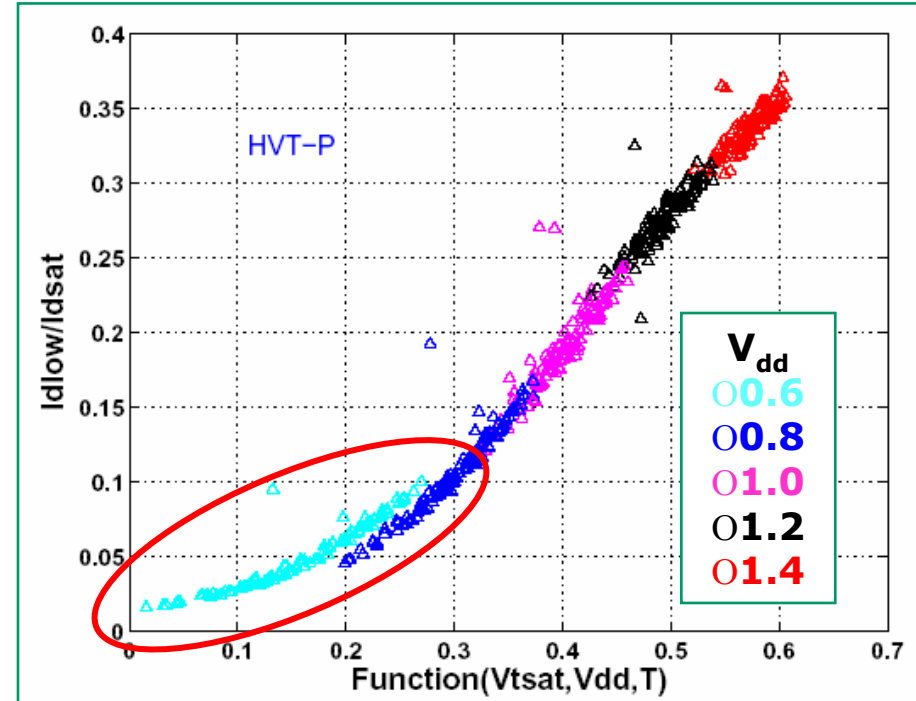
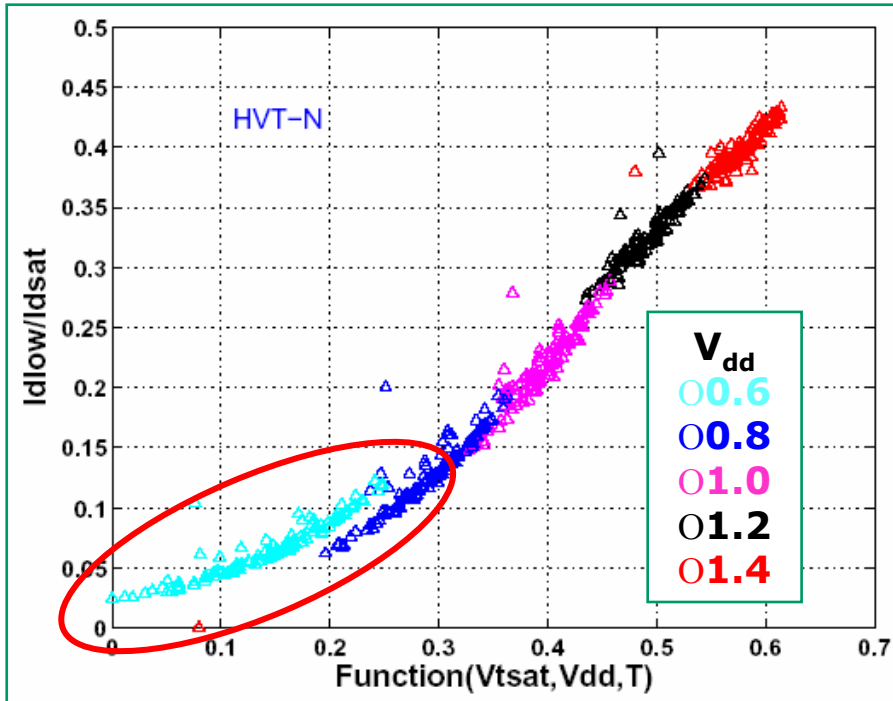


N vs. P Comparison

- N-MOS shows consistently higher I_{dlow}/I_{dsat} than P-MOS
- Possibly caused by impact ionization rate difference of electrons and holes
 - II increases I_{dlow} → higher I_{dlow}/I_{dsat} in N than P



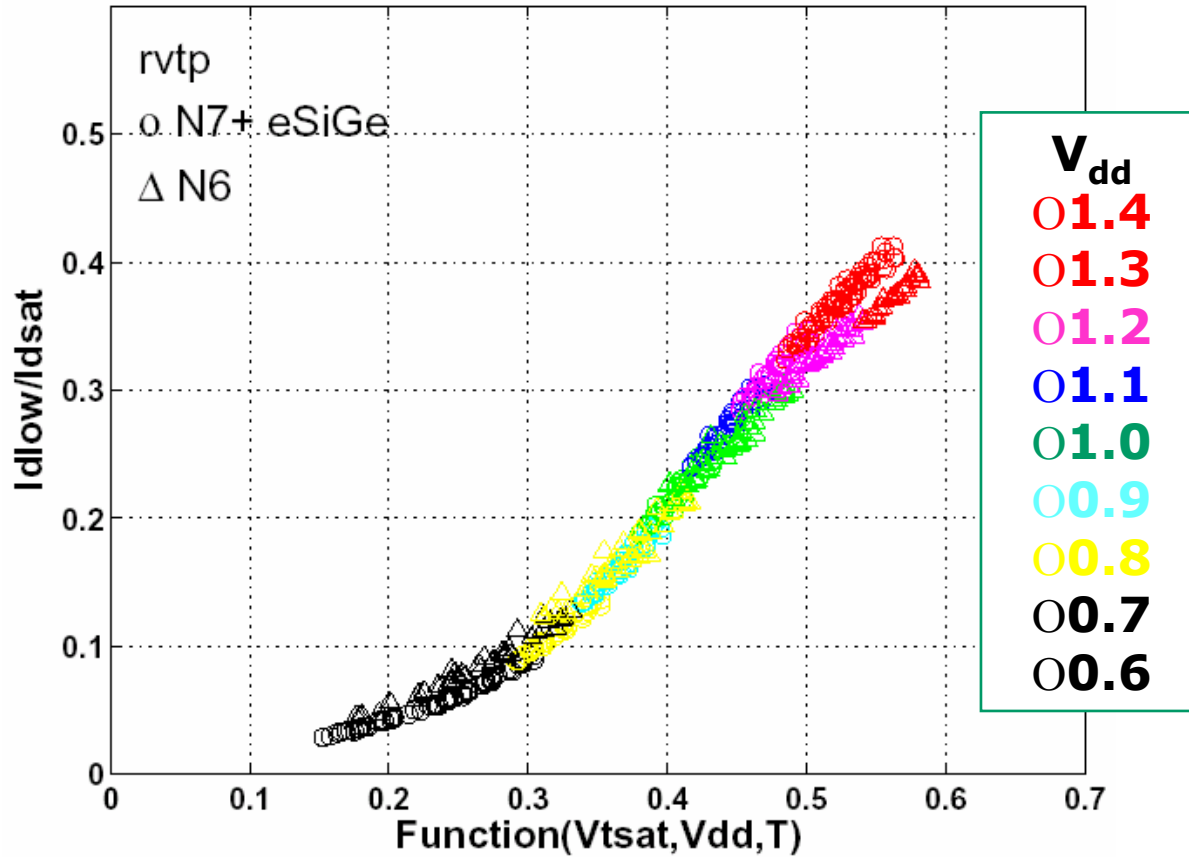
Near- vs. Super-Threshold Idlow



- For $V_{DD}=0.6V$, I_{dlow} measured @ $V_{gs}=0.3V$
- For HVT N/P: $V_{gs}=0.3V$ is barely above V_{tsat} @ $V_{dd}=0.6V$ → near-threshold region!
- I_{dlow} vs. $(V_{gs}-V_{tsat})$ becomes exponential (instead of \sim linear in the super-threshold region) → a higher line results

Cross-Technology Comparison

- Slight increase at the higher end with embedded SiGe



Applications

- One of the tools to assist in target iteration for speculative SPICE modeling

